Solid State Electronics 168 (2020) 107719

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Post-process porous silicon for 5G applications

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ARTICLE INFO

The review of this paper was arranged by "Joris Lacord"

Keywords:
Effective permittivity
Effective resistivity
Microwave losses
Porous silicon (PSi)
CMOS compatibility
RF substrate
Silicon-on-insulator (SOI) technology

ABSTRACT

The interest of 5G in centimeter and millimeter waves relies on large blocks of available spectra and thus increased bandwidth. At these frequencies, the dielectric and conductive losses of the substrate can greatly degrade the performances of RF circuits. With high electrical resistivity and low relative permittivity, porous silicon is an ideal candidate as a high-quality RF substrate. This paper presents an innovative technique of post device fabrication integration of porous silicon (POST-PSi) with the substrate. The frontside is not involved in porous layer growth and therefore the integrity of the RF circuitry is not impacted by the POST-PSi process. A comparison of the RF performances with benchmark trap-rich (TR) RF silicon substrate is presented. In addition to its compatibility with standard microfabrication processes and stable final structure, POST-PSi provides characteristics of low losses, high isolation and very high linearity, unmatched by any other silicon-based substrate. Finally, the substrate's RF performance is evaluated at high temperature, and POST-PSi substrate linearity is shown to remain sufficiently high for RF and 5G applications up to 175 °C.

1. Introduction

5G is the next generation of mobile networks and will achieve speeds of several Gb/s. 5G is therefore designed to support large amounts of data, but also to enable a very large number of connections and multiply the types of uses. It will be versatile, to adapt to the needs of each use: performance, energy savings, critical uses (e.g. autonomous cars), etc. For 5G, centimeter and millimeter waves are considered because they have wide ranges of available spectra (3.5–6 and 24–86 GHz) and will also bring new features such as beam forming and Multiple Input Multiple Output (MIMO) antenna arrays.

The choice of 5G technology blocks is critical to ensure the required performance. Despite the excellent performance of emerging materials, silicon-based technologies remain a strategic choice for RF applications. The co-integration of high-speed digital circuits alongside analog and RF front-end modules on the same chip, the excellent control of the silicon process and the low production cost of the substrates are some advantages of silicon technologies. A substrate technology enabling such integration and providing a platform for RF and mm-wave circuitry is desired to be low-loss, highly isolating, and highly-linear.

However, in silicon-on-insulator (SOI) substrates, standard doped silicon handle substrate suffers from high losses and poor isolation for co-integrated circuits due to its high electrical conductivity. Indeed, the so called standard-resistivity wafers (Std) have nominal resistivities in the range of 5–20 Ω cm, and this very low value makes the implementation of quality RF circuits a strong challenge, along with their co-integration alongside digital modules.

It turns out that a lower-doped silicon handle substrate with a high nominal resistivity ($\rho_{nom} > 1$ kΩ cm) has similar poor RF performances due to a parasitic surface conduction (PSC) effect beneath the buried oxide (BOX) layer, which degrades the effective resistivity of the substrate [1]. Indeed, these so called high-resistivity (HR) substrates owe their name to their low nominal doping, but due to unavoidable fixed oxide charges at the Si/SiO_2 interface, a large amount of electrons are induced at this surface, drastically lowering the effective resistivity sensed by planar technology. The effective resistivity of such HR substrates is typically in the range of 30–50 Ω cm, significantly lower than ρ_{nom}, and of little performance improvement over Std wafers.

Over the past three decades, a series of silicon-based substrate technologies have successfully mitigated this parasitic surface conduction effect to reach higher effective resistivities in the range of several kΩ cm. The introduction of a thin poly-silicon layer (typically 300 nm to 2 μm-thick) rich in defects between the BOX and the high-resistivity silicon handle substrate provides a highly resistive state at this interface. The oxide charges are no longer balanced by free carriers to define a highly conductive parasitic layer, but are instead compensated by

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https://doi.org/10.1016/j.sse.2019.107719

Available online 26 November 2019

ionized traps, that are charged, but do not participate in conduction. The Fermi-level at the interface is pinned near mid gap by the large number of traps in the polysilicon layer, and this structure defines the so called trap-rich (TR) SOI substrates. This technique has proved to be very effective while being compatible with industrial SOI CMOS thermal budgets and wafer fabrication processes [2].

As an alternative to TR-SOI, porous silicon (PSi) has been proposed for several decades. This material is formed by electrochemical dissolution (anodization) of bulk silicon. PSi achieves high resistivity, low permittivity, low losses, low crosstalk levels, and strong linearity. For all these reasons, PSi is a promising candidate for RF substrates. Substantial amounts of work have proved PSi to be a promising candidate as RF substrates [3–21], however, the incompatibility of porous silicon with high temperature annealing (cracking or bending in the substrate) makes its integration in to a full CMOS process impossible with sufficient yield.

The PSi substrates proposed in [3–21] integrated the porous layer before the deposition of the overlying insulating layer and fabrication of the RF passives. In this paper, we present an innovative technique for integrating high-quality PSi into post-process of RF circuit fabrication (POST-PSi): PSi electrochemical porosification is performed after the circuits are completely processed and before the packaging steps. This approach overcomes the incompatibility issues of the PSi presence in a standard CMOS process. POST-PSi substrates is compared with the benchmark trap-rich RF substrates technology in terms of their effective electrical parameters extracted through the direct S-parameter measurements of coplanar waveguides (CPW) over a wide frequency range from 10 MHz to 67 GHz, which covers most of the frequencies targeted by 5G. Furthermore, large-signal harmonic distortion measurements reveal POST-PSi to be of record-high linearity amongst silicon-based substrates. Finally, both small- and large-signal measurements are performed up to 175 °C.

2. Substrate description

To benchmark the newly developed POST-PSi substrate and evaluate its performance, it is compared to the two most widely used RF substrate technologies in the RF industry today: the HR-SOI and TR-SOI substrates. In this section the physical structures and fabrication processes of each substrate are described.

2.1. High resistivity substrate (HR)

The HR substrate is based on an n-type silicon wafer with a nominal resistivity above 5 kΩ cm. A 500-nm silicon dioxide (SiO_2) layer is deposited at 300 °C by plasma-enhanced chemical vapor deposition (PECVD), followed by a 1-μm-thick layer of aluminum deposited by physical vapor deposition (PVD) for the definition of the CPW line devices by standard photolithography and wet etching. A typical HR substrate structure is depicted in Fig. 1(a).

2.2. Trap-rich substrate (TR)

The TR substrate consists in an n-type HR-Si wafer with a nominal resistivity above 5 kΩ cm and a 300-nm-thick poly-Si layer rich in traps and defects deposited through low-pressure chemical vapor deposition (LPCVD). On top, a 500-nm SiO_2 layer is deposited at 300 °C by PECVD, followed by a 1-μm-thick layer of aluminum deposited by PVD for the definition of the CPW lines. A typical TR substrate structure is depicted in Fig. 1(b).

2.3. Pre-process porous silicon substrate (PRE-PSi)

The PRE-PSi substrate, is prepared from a strongly doped p-type silicon wafer (10–20 mΩ cm) porosified in an electrolyte composed of 1:1 mixture of hydrofluoric acid (HF 49%) and ethanol. A current density of 75 mA/cm^2 for 40 min is applied. Finally, the PRE-PSi substrate is annealed in oxygen at 300 °C for 2 h to strengthen the microstructure, and then in nitrogen at 420 °C for 2 h to stabilize the structure. Using this process, the top 50 μm of the silicon are porosified, yielding a PRE-PSi structure such as shown in Fig. 1(c). On top, a 500-nm SiO_2 layer is deposited at 300 °C by PECVD, followed by a 1-μm-thick layer of aluminum deposited by PVD for the definition of the CPW lines.

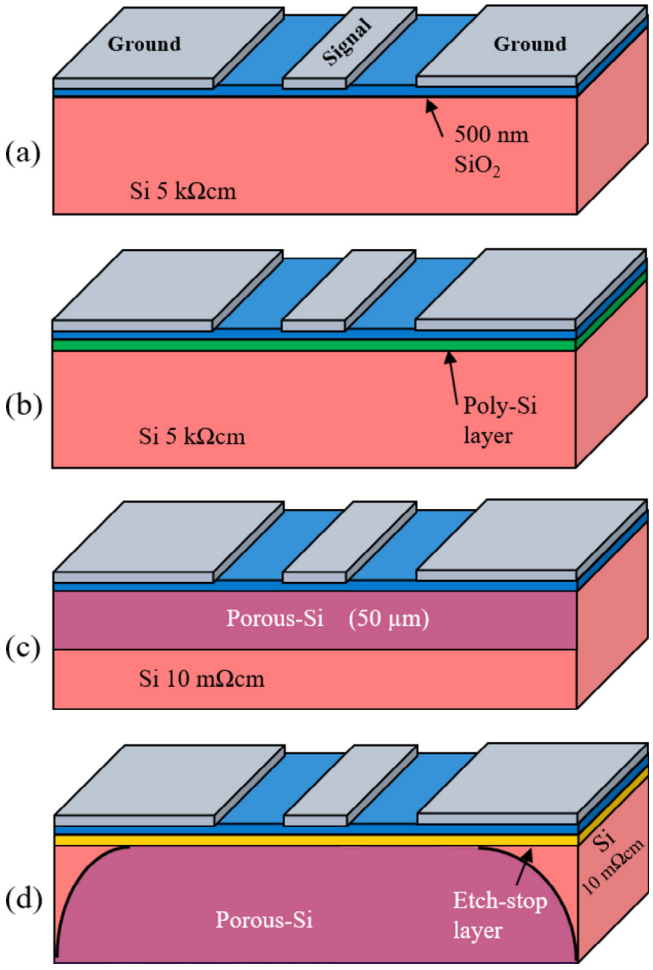

Fig. 1. Schematic of a CPW transmission line fabricated on (a) HR- substrate, (b) TR- substrate, (c) POST-PSi and (d) POST-PSi substrates.

The mesoporous PRE-PSi substrate, has an average porosity of 50% over the porosified 50 μm (evaluated by weight measurements) and with a pore size of around 15 nm in diameter, that was evaluated by images obtained from scanning electron microscopy [21].

2.4. Post-process porous silicon substrate (POST-PSi)

A 380 μm-thick doped p-type silicon wafer is used as starting substrate. Before processing, the silicon wafer is cleaned by O_2 plasma and immersed in 2% HF to remove the thin oxide. A HF-resistant etch-stop layer is deposited on the substrate frontside. A 500 nm-thick SiO_2 layer is deposited by PECVD atop the etch-stop layer, and CPW lines are then fabricated by standard photolithography and wet etching in a 1 μm-thick aluminum film.

The structure of a POST-PSi substrate is presented in Fig. 1(d). The porous layer is formed starting from the backside of the wafer to reach all the way to the frontside of the silicon handle substrate. The electrochemical porosification stops on the etch-stop layer placed between the silicon substrate and the RF circuit layers. A hard mask on the wafer

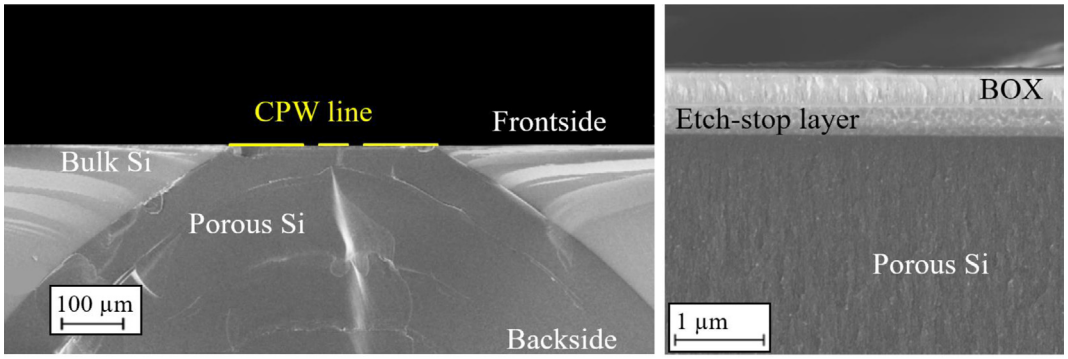

Fig. 2. Cross-sectional view of POST-PSi substrate (a) over full substrate thickness, and (b) magnified view at the frontside of the wafer. Both images obtained from scanning electron microscopy.

backside is used to define the location of the porosification. The porous layer is therefore defined locally within the substrate, and in our case is implemented under the CPW device, as can be seen from Fig. 2(a).

The starting silicon's nominal resistivity is 10–20 mΩ cm (for both PSi samples) to facilitate the porosification process. However, the porosification process has been demonstrated to be adaptable in order to yield high-performance RF substrates starting from p-type wafers with resistivities up to 10 Ω cm [21] (using a PRE-PSi type of process).

The porosification is performed in an adapted electrochemical cell from the backside. Its particularity is to not involve the frontside of the wafer and therefore not to affect the RF circuits (Fig. 3). PSi is prepared by anodization in a 3:l volume solution of HF (49%):ethanol. The result is a mesoporous silicon with pore sizes in the range of a few tens of nanometers, and a porosity close to 70%.

Fig. 2 shows a cross-sectional view of a locally realized porous silicon substrate imaged from a scanning electron microscope (SEM). PSi grows through the entire substrate thickness from the backside and reaches the frontside over a surface area similar to the openings made in the mask on the backside. An over-etching ensured that the porous layer is present under the whole RF device (CPW line). Due to the isotropy of the porous silicon growth, the porous layer is largely extended laterally at the backside over a distance that is of the order of the substrate thickness.

Fig. 2(b) is a magnified image performed at the frontside of the sample and shows the BOX at etch-stop layers above the porosified silicon. It confirms that the porosification reached all the way to the etch-stop layer, and that there is no longer any bulk silicon remaining beneath the RF devices, which would degrade the high-quality RF performances.

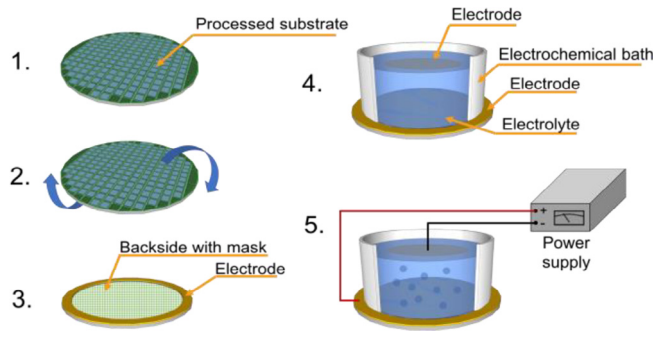

Fig. 3. Schematic of POST-PSi fabrication process: 1. The starting substrate is a processed substrate. 2. The frontside is not involved in POST-PSi fabrication process. 3. A hard mask on the backside is used for a locally porosification under interest areas. 4. Schematic of adapted electrochemical cell. 5. Post-process electrochemical porosification.

3. RF characterization at room temperature

On-wafer measurements of CPW lines were performed using an Agilent 2-port performance network analyzer (PNA)-X vector network analyzer and a pair of ground-signal-ground (GSG) Infinity probes from Cascade Microtech with 150 µm pitch. Short-Open-Thru-Load (SOLT) calibration method is used to calibrate the system at the probe tips for better accuracy of the measurement. The lines are 8 mm-long, the signal and ground widths are 38 and 208 µm-wide, respectively, and the spacing between the signal and ground lines are 18 µm-wide. The CPW electrical parameters are extracted using the methods described in [22,23].

3.1. Small-signal measurements

The RF characteristic substrate parameters, including effective resistivity and permittivity, lineic attenuation coefficient and characteristic impedance, of the fabricated CPW lines on the different substrates described above are depicted in Fig. 4. Though low-doped, the effective resistivity of the HR substrate presents a low value in the range of 35 Ω cm that is due to the parasitic surface conduction (PSC) effect that severely limits the HR sample's RF quality.

The TR substrate presents significantly improved effective resistivity with a value of between 4 and 8 kΩ cm thanks to the polysilicon layer rich in traps that captures free electrons, avoiding the creation of a highly conductive layer and preventing the PSC effect.

The porous silicon substrates both presents higher effective resistivities still are associated to a large number of trapping states present at the pore interfaces [21,24], interfaces that are in very high quantity in the fabricated mesoporous silicon samples.

These high amounts of traps pin the Fermi-level near mid-gap in both PSi-samples, making the porous regions highly-resistive despite the high nominal doping of the samples. The slightly higher effective resistivity of the POST-PSi sample is associated to a thicker PSi layer beneath the CPW line, and to a higher porosity.

The 70% porosity of the POST-PSi sample translates into an effective relative permittivity of approximately 3.6, while the 50% porosity of the PRE-PSi sample translates into an effective relative permittivity value of around 5.4.

Both the HR and TR samples present effective relative permittivities that converge to approximately 11.5, close to the value of silicon (11.7). The permittivity reduction offered by the PSi samples is desirable to reduce parasitic substrate capacitance and coupling, especially at high frequencies as the substrate capacitance will be the dominant coupling mechanism.

In terms of lineic line losses, the CPW on the HR substrate present an insertion loss of 1.1 dB/mm at 4 GHz. These losses are mainly related to the substrate's low effective resistivity. The losses on the three high

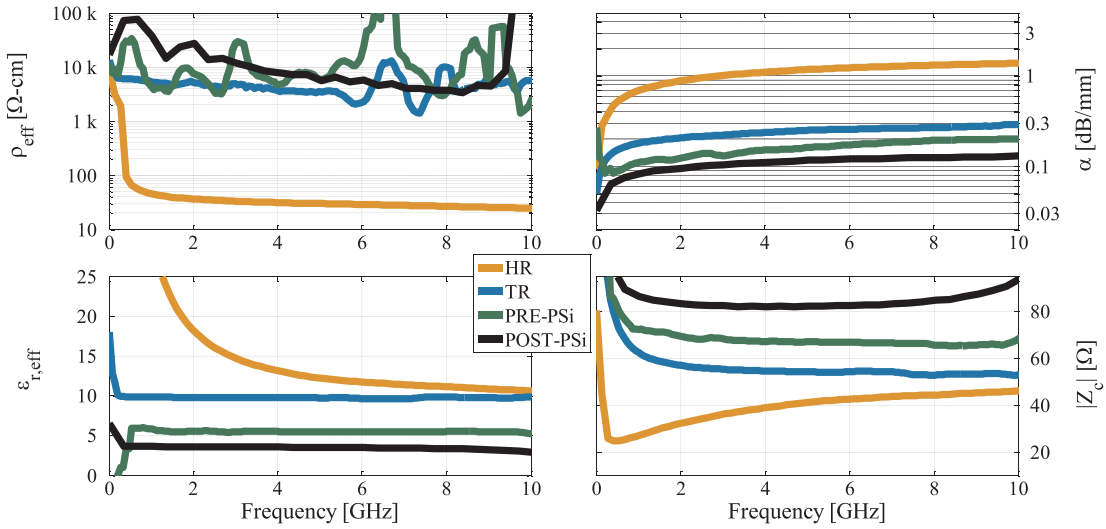

Fig. 4. Effective electrical substrate parameters extracted from wideband S-parameter measurements of RF CPW-lines at 25 °C. Top left: effective substrate resistivity. Bottom left: effective substrate relative permittivity. Top right: CPW line losses per unit length. Bottom right: CPW line characteristic impedance.

quality substrates are low, in the range of 0.11–0.22 dB/mm at 4 GHz, and these losses are almost entirely due to the series metallic losses of the CPW lines themselves. The 0.1 dB/mm difference between the three high-quality samples is associated to slight discrepancies in the deposited metallic layer thickness and roughness, because above effective resistivity values of 3 kΩ cm, the losses associated to the substrate can truly be considered negligible relative to the metallic losses for CPW lines of these dimensions [25]. The metallizations for the samples were performed at different times and likely present variations of 5–10% that are enough to explain the 0.1 dB/mm difference observed.

3.2. Large-signal measurements

To characterize substrate linearity, large-signal measurements of the CPW lines were performed on-wafer using a dedicated setup. A single tone, with fundamental frequency of 900 MHz, is injected into one port of the same 8 mm-long CPW line on each substrate. The power of this input tone, that we shall denote as H'1, is swept from −30 dBm to +25 dBm using 50 Ω reference port impedances, and the output signal is retrieved by a spectrum analyzer. Due to the non-linear behavior of silicon-based substrates signal distortion is introduced and the output signal is in general a multi-tone signal, with a fundamental component (900 MHz in our case), denoted as H1, along with harmonic components at all integer multiples of this fundamental frequency, denoted as H2, H3 and so on. The H2 (at 1.8 GHz) and H3 (at 2.7 GHz) components of the power at the output of the CPW on each substrate are plotted relative to the power of the fundamental component H1 in Fig. 5, at 900 MHz.

The electrical characteristics of the HR substrate are strongly voltage-dependent [26–28], and consequently it presents high levels of harmonic distortion (HD).

By introducing a polysilicon trap-rich layer beneath the BOX of a nominally high-resistivity substrate, reductions of more than 55 and 60 dB are obtained, respectively, for the second and third harmonics generated on a TR substrate. The traps at the Si/SiO_2 interface effectively pin the Fermi-level near mid-gap. Contained to a narrow energy range by these traps, the position of the Fermi-level is rendered much less voltage-sensitive, improving the linearity of the substrate and reducing the substrate-induced distortion in signals propagating through overlying transmission lines [29,30].

The harmonic distortion levels are further reduced when considering PSi as the substrate material. The second harmonic level generated on the PRE-PSi substrate is an impressive 30 dB lower than on

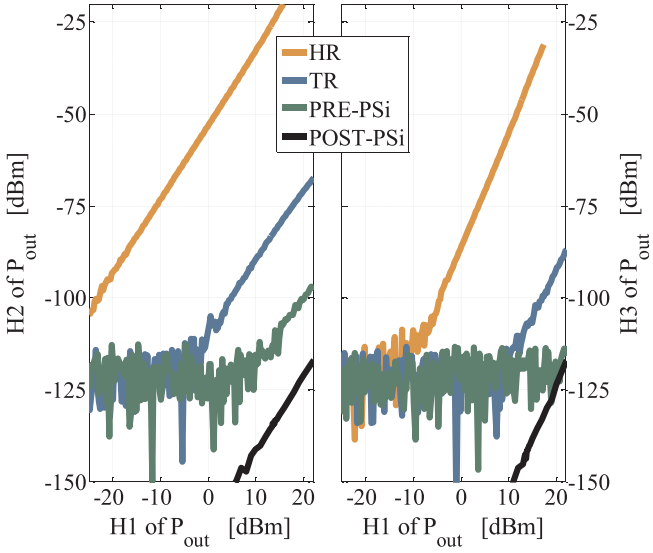

Fig. 5. Comparison of the measured HD levels induced in 8 mm-long CPW lines implemented on the four substrates under consideration. The fundamental frequency is 900 MHz and the lines are biased to 0 V DC.

TR. The noise floor of the setup used to characterize the distortion on the HR, TR and PRE-PSi substrates was at −115 dBm. This was not sufficiently low to characterize the POST-PSi sample, so an ultra-low noise setup (floor at −165 dBm) was used to measure the POST-PSi wafer, that presents a record high-linearity amongst silicon-based substrates, boasting linearity improvements of 51 dB compared to the benchmark TR sample. The TR sample fabricated in this work has a linearity comparable to the commercially available "enhanced Signal Integrity" (eSI™) trap-rich wafers from Soitec. The linearity of the sample considered in this works compares to their 1st generation eSI80 product line [31–33].

The increased linearity for the PSi samples is associated to a tight pinning of the Fermi-level throughout the entire volume of the PSi layers. In contrast to TR substrates, in which the Fermi-level is pinned at the BOX interface due to traps in a thin 300 nm poly-Si layer, the PSi wafers provide trapping centers deep into the substrate, along the pore walls. These trapping centers are created over a depth of 50 μm for the PRE-PSi and over a depth of 380 μm (entire substrate thickness) for the POST-PSi sample. The electrical characteristics of the entire PSi layers

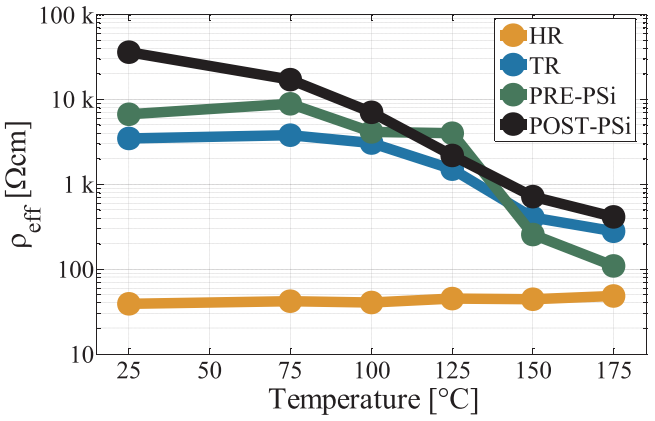

Fig. 6. Extracted effective resistivity as a function of substrate temperature ranging from 25 °C to 175 °C for the five Si-based substrates.

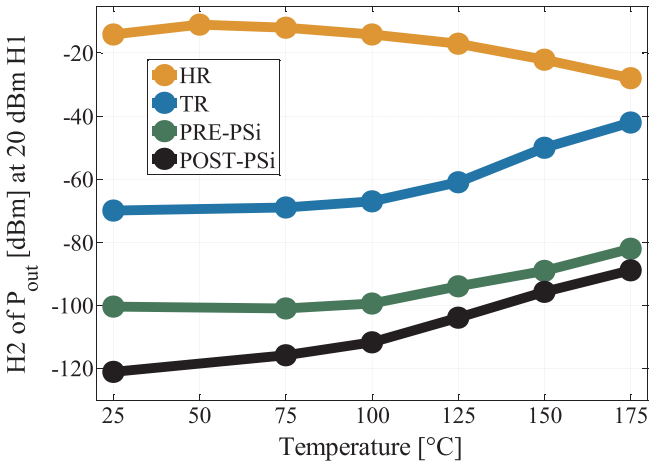

Fig. 7. Measured CPW H2 levels at +20 dBm of H1 component on the TR substrate, PRE-PSi and POST-PSi substrates versus temperature at 0 V DC bias.

resist modulation by large signal RF fields. As a result, the voltage dependence on the Fermi-level, on carrier densities, and therefore on substrate conductivity, is even further reduced, conferring to the CPW transmission lines on PSi substrates remarkably high linearity.

4. RF characterization at high temperature

4.1. Small-signal measurements

Small-signal S-parameter RF measurements of CPW lines on all substrates were also conducted up to 175 °C. During measurements the temperature of the samples was controlled by a Temptronics thermal 8-in chuck tool. Fig. 6 compares the mean effective resistivity in the GHz region on all substrates over a wide temperature range, from 25 °C to 175 °C. Increased temperature in highly resistive semiconductor substrates usually has the effect of degrading their performances, by increasing the number of thermally generated intrinsic free carriers in such carrier-free semiconductors. This in turn decreases the effective resistivity which has the unwanted effects of raising substrate losses as well as noise coupling levels. This phenomenon is observed in the TR substrate above 110 °C as its effective resistivity starts to rapidly decrease; a reduction of one order of magnitude is measured at 175 °C.

The HR's effective resistivity varies little with temperature. The reason for the negligible variations in the HR substrate is that the coupling mechanism is through the parasitic surface conduction channel induced at the Si/SiO_2 interface. In this channel the carrier density is very high, revealed to be of the order of 10^{18} cm^{-3} by Silvaco Atlas simulations. At such high concentrations the carrier mobility is already limited by carrier interactions, and the temperature increase from 25 °C to 175 °C adds a comparatively negligible amount of additional interactions of the carriers with phonons, hardly reducing the carrier mobility any further. This is in good agreement with Arora's mobility modelling in [34].

Below 100–125 °C, the TR and both PSi substrates maintain their significant effective resistivity advantages over HR, preserving performance values in the kilohm-centimeter range.

Above 110 °C, the PRE-PSi sample's effective resistivity curves degrades in a similar fashion to that of the TR substrate's curve. For the POST-PSi sample this temperature point is lower, as a higher effective resistivity value is more sensitive to thermal generations starting from a lower temperature point. The resistivities in the porous layers of both PSi substrate decrease by several orders of magnitude. Mobility is not expected to degrade by several orders of magnitude in the considered temperature range, and this observation leads us to the hypothesis that the carrier concentrations in the porous layer of these substrate drastically increase with temperature, thermally generated from the material's valence band or perhaps from trap energy levels in the porous layer.

4.2. Large-signal measurements

Fig. 7 plots the H2 levels of the four substrates for increasing temperature at a H1 output level of +20 dBm with a 0 V DC bias applied to the 8-mm long CPW lines.

The TR, PRE-PSi and POST-PSi substrates become less linear as the temperature is increased. This increase in HD levels is explained in TR technology by the thermal generation of free carriers in the silicon bulk volume, which increases the conductance through the substrate. This in turn means that more RF current will flow through the non-linear substrate, inducing higher signal distortion.

Above 110 °C the harmonics of the TR and PRE-PSi substrates increase, and this is the same temperature point above which the effective resistivity of both of these samples dramatically decreases, as has been shown and discussed in Fig. 6. Similar temperature dependent behavior of HD levels of a porous silicon substrate fabricated from milliohm-cm resistivity silicon is shown in [18].

The linearity of the POST-PSi substrate degrades starting at lower temperature, and this is also in accordance with the temperature degradation of its extracted effective resistivity discussed in Fig. 6.

Although the HD levels in PRE-PSi and POST-PSi increase by 20 dB and 30 dB, respectively, between 25 °C and 175 °C, they still remain very low, and both provide sufficient linearity performance all the way up to 175 °C for modern day RF applications, and even 5G.

5. Conclusion

In this paper, the RF electrical performances of an innovative POST-PSi substrate were investigated and compared with the benchmark TR solution and the existing PRE-PSi. In this innovative POST-PSi technique, local porosification of pockets of high-quality RF PSi-substrate are formed beneath the RF devices of interest. Only the substrate backside is involved in the process which is strongly compatible with foundry-level processes. POST-PSi provides the highest RF electrical performances with low relative effective permittivity (~3.6), and high effective resistivity (above 25 kΩ cm). And although the RF results of POST-PSi are slightly better than those of PRE-PSi, its main advantage over PRE-PSi lies in its CMOS process compatibility, and in the possibility of a final stronger structural stability due to localized pockets of porosification. The combination of low permittivity and high effective resistivity of POST-PSi allows for the integration of high-quality RF circuits and low crosstalk interference levels.

Acknowledgment

The authors would like to thank Incize for access to their ultra-low noise floor harmonic distortion measurement setup. This research has been supported by the Walloon Region (APOSIS & PROTOSIS projects). The authors thank all the engineers and technicians of the UCL-WINFAB clean rooms and UCL-WELCOME characterization plateform for technical support.

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