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Trap Recovery by in-Situ Annealing in Fully-Depleted MOSFET With Active Silicide Resistor

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***Abstract*— This work reports first original results on the impact of active in-situ electro-thermal recovery, on the electrical and low-frequency noise characteristics of N-type MOS transistor with thick high-k metal gate oxide, from 28 nm Fully Depleted Silicon-On-Insulator (FDSOI) process. In order to recover "typical" device characteristics, four cycles of local thermal annealing up to 590K are applied for 14 ms each, using an active silicide source. Experimental results reveal an important improvement of the "corner" transistor's I-V behavior allowing the recovery of "typical" device characteristics. An increase of the maximum transconductance by 43% is obtained. In the same time, a typical device stays unaffected by this local annealing. Low-frequency noise measurements show a clear reduction of the 1/f noise and Random Telegraph Noise by almost one decade, after the electro-thermal recovery. This can explain the improvement of the electrical characteristics by annealing of defects.**

***Index Terms*— LF noise, 1/f noise, random telegraph noise (RTN), FD-SOI, MOSFET, in-situ thermal annealing.**

I. Introduction

TECHNOLOGICAL innovations keep on down-scaling CMOS transistors in accordance to the Moore's law, ensuring the continuous improvement of the device performance and high packing density [1]. This has led to many process challenges at the gate stack level, leading to advanced solutions like the deployment of High-k metal gate stacks [2]. Nevertheless, uncontrolled active oxide traps remain an unavoidable issue causing the limitation of the device performance and matching according to the process dispersion with ageing impact. The defects impact key MOSFET parameters, with a cumulative degradation during device operation [3]. These can cause limitations in many promising applications, in particular analog and RF circuits with standard and thick-gate oxide process technology [4], [5], [6]. Thick-gate oxide devices in FDSOI present an increasing interest for Input/Output (I/O) and analog circuits, as e.g. low noise amplifiers (LNA) and future integration with quantum devices [7], [8]. Wafer or chip-level thermal annealing has demonstrated reliable and efficient results regarding the recovery from oxide traps. However, this method remains constrained by the post-CMOS annealing limits (e.g. high risks of metallization layer degradation, package thermal limit, in addition to reliability issues related to mechanical stability of the device caused by the different thermal expansion coefficients). Recently, there is an increased interest to the in-situ annealing recovery using different device architectures [9], [10], [11]. In this study we use a customized design of a MOS transistor implemented in the standard 28nm Ultra-Thin Body Ultra-Thin BOX (UTBB) FD-SOI technology (Section II). The layout consists in creating two active contacts connected to the source (and to the drain) of the transistor, forming a silicide resistor between the two source (or two drain) contacts. This resistor is used as a low-voltage local heater based on Joule effect. The electro-thermal response of such local heater was characterized and calibrated in recent works [12]. The recovery of I-V characteristics of thin gate oxide transistors was reported in [13]. This study extends those findings. It demonstrates the contribution of trap recovery to the improvements of thick-gate oxide transistors, implemented in 28nm FDSOI UTBB technology, notably for analog circuits, in correlation to the reduction of low-frequency noise behavior after thermal annealing (Section III).

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II. Device Description and Measurements's Setup

The devices under test feature a high-k thick gate oxide with equivalent oxide thickness (EOT) of 3.4nm, notably developed for analog application at higher voltages than digital CMOS core [12]. Special considerations are made for the metallization layers on silicon demonstrator to sustain the thermal-annealing conditions (i.e. high temperature, high current) without affecting the oxide gate integrity [12]. The transistor is designed (Fig. 1) with 2 μm large channel (W), 150 nm gate length (L) and seven terminal connections as follows: two source contacts (S1 and S2), two gate contacts (G1 and G2), two drain contacts (D1 and D2) and a back-gate contact (BG). The device is used in two modes. First, the standard operation uses one contact of each terminal (D1, G1, S1 and

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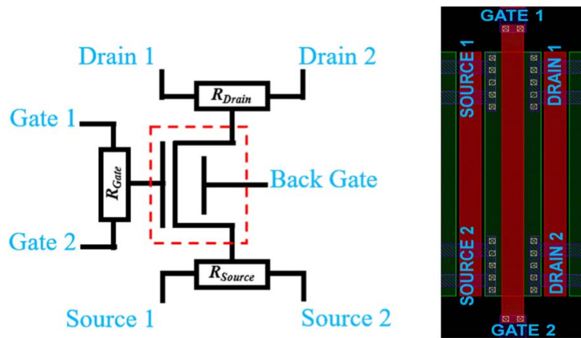

Fig. 1. Schematic & layout presentation of the tested MOSFET.

BG) leaving the other contacts in floating condition. Second, the annealing mode consists in biasing the source resistor through S1 and S2 to generate Joule effect and spread the heat into the structure by thermal conduction. Other contacts left floating. G1 and G2 can be classically used for temperature sensing [13]. Here, for temperature monitoring, the local heater was pre-calibrated by measuring the resistance dependence to the chuck temperature and establishing the temperature coefficient of the material. TCAD simulations have also been performed in [12] to validate the calibration and explore the actual temperature distribution over the structure.

$I-V$ DC characterisation was firstly performed in standard mode, on "fresh" dice, followed by Low Frequency Noise (LFN) as well as transient Random Telegraph Noise (RTN) measurements, using *Keysight LFNA noise Analyser* and *B*1500 semiconductor analyser. LFN measurements were performed from 1 Hz up to 1 MHz and RTN current traces were recorded for 5.3 s with a time step of 82 μs. As the noise in a MOSFET is bias-dependent [14], it is evaluated at different levels of fixed drain current $\sim$ 1 nA, 10 nA, 100 nA and 1 μA for both "corner" and "typical" devices. Secondly, after these reference measurements, four annealing cycles were applied in air via the source contacts of the transistor. Each annealing cycle consists in applying a voltage bias between S1 and S2 ranging from 0 up to 1.4 V and generating a maximum thermal annealing of $\sim$ 590 K at the source level. During the annealing, the other contacts are kept in floating condition. The annealing time is set at 14ms for each cycle. The transconductance (g_m) is extracted from $I-V$ curves after each cycle. After the last cycle (upon $I-V$ and g_m-V curves stabilization), a second run of noise measurements is performed. Among the several dices characterized according to this methodology, we selected and present here two representative extreme cases: a first typical device meeting process specifications noted "Typical-Die", and a second initially-defective device corresponding to a process corner and noted "Corner-Die".

III. Results and Discussion

A. I-V Characterization

This section synthesizes the measured DC Figures of Merits (FoM) of typical and corner devices. After four annealing cycles, the drain current of the corner transistor is enhanced by 40% at V_g = 700 mV and the subthreshold slope (SS) is slightly improved by 5 mV/dec to match the typical values. Nevertheless, FoM of the typical-Die's transistor remains unaltered after four annealing cycles. Fig. 2a supports that by comparing the I-V characteristics of the transistors pre and post-annealing. Also, the g_m/I_d versus g_m analog FoMs of the different devices are compared in Fig. 2b following [15]. The maximum transconductance is stabilized at 126 μA/V, presenting an improvement of g_m by 43%, explained by the increase of effective mobility [16]. The representation of g_m/I_d vs g_m is not sensitive to the threshold voltage, V_{Th}, and further highlights the subthreshold and mobility properties below and near threshold [17]. These appear clearly degraded in the Corner-Die before annealing and improved after annealing, fairly approaching the stable typical-Die. All the parameters of the "corner" device are finally matching, i.e. recovering the typical values.

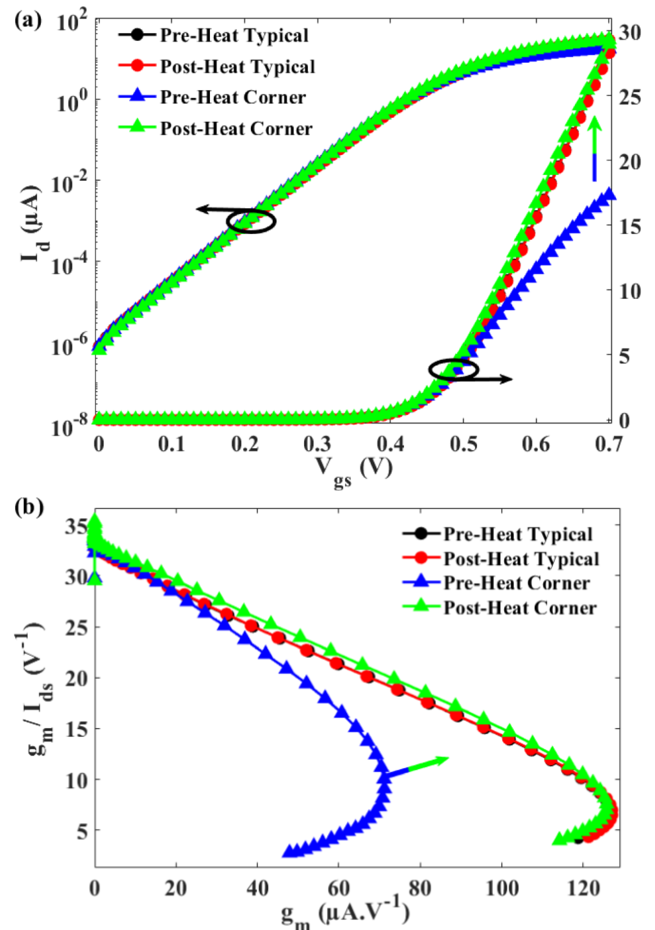

Fig. 2. (a) Drain versus gate voltage of Typical and Corner devices, measured before and after annealing in linear regime with V_d = 50mV. (b) g_m/I_d versus g_m characteristics of tested MOSFETs, extracted before and after annealing in linear regime at V_d = 50 mV. ($V_S = V_{BG}$ = 0V).

B. Low-Frequency Noise Measurements

The power spectral density (PSD) noise measurements of the defective Corner-Die and good typical-Die, are reported before and after annealing (Fig.3). 1/f noise is mostly obtained in the lower frequency and lower current ranges, but at $I_d \sim 1\mu$A (i.e. $V_g \sim V_{Th}$), a clear $1/f^2$ Lorentzian-like behaviour is noticed for the fresh Corner-Die, caused by pronounced RTN component (as confirmed below). This indicates an important trap contribution at the energy level corresponding to a gate voltage close to V_{Th} [18]. Oxide traps manifest only when the local Fermi level in the vicinity of the active trap is close enough (within several kT) to the trap energy level [19]. This is achieved by changing the gate bias, which explains

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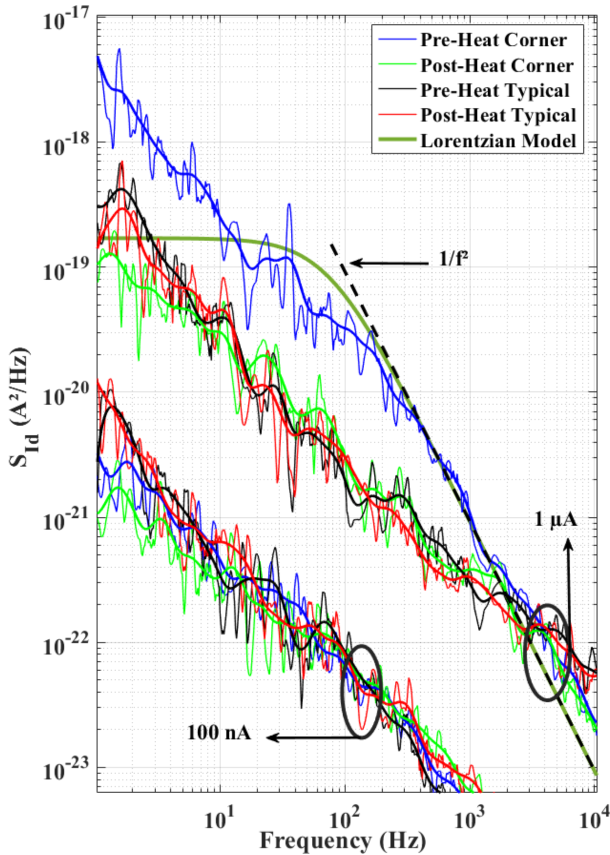

Fig. 3. Noise power spectral density of the MOSFETs in Typical-Die and Corner-Die. Measured before and after annealing in linear regime. The voltage overdrive ($V_o = V_g$-V_{Th}) $V_{o1} = -50$mV and $V_{o2} = -120$mV, respectively, for Id = 1 μA and Id = 100 nA. These values are identical for both Typical and Corner Dices before and after annealing.

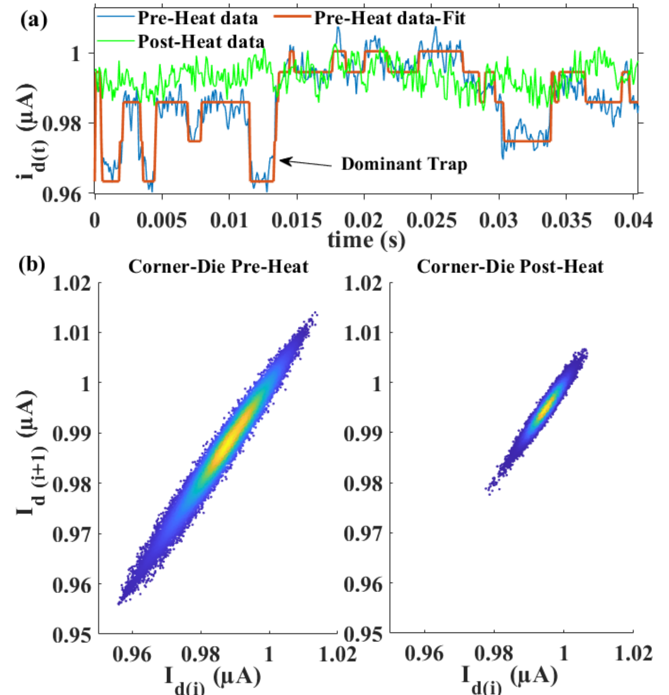

Fig. 4. (a) Time trace measurements of the drain current of the fresh and post-heat Corner-Die in linear regime ($V_d = 50$ mV, with $V_o = -50$ mV), (b) Lag plot of I_d measurements, presented in the same scale before and after thermal annealing, where the colour weighted plot demonstrates the frequency of I_d appearance.

the absence of trap effect at the lower current levels ($I_d < 1\mu$A). The PSD noise of the fresh Corner-Die at $I_d \sim 1\mu$A is about one decade higher compared to the typical-Die. After annealing, 1/f^2 noise has been suppressed and the PSD noise is significantly improved, to closely match the typical-Die level. As for the DC parameters, no significant change is observed on the typical-Die's PSD noise after annealing.

The total noise power is integrated in a bandwidth from 1 Hz to 612 Hz (i.e. limited by the worst-case roll-off frequency of the equipment for respective bias conditions). The corner die shows a decrease of one order of magnitude after thermal annealing, from $\sigma_{id}^2 = 1.91\ 10^{-17}$ (A^2) to $\sigma_{id}^2 = 1.82\ 10^{-18}$ (A^2), respectively. To further probe these observations, the time-domain signature of the measured drain current i_d (t) of the fresh Corner-Die was investigated (Fig. 4a). At $I_d \sim 1\mu$A, a multiple-level RTN signal was observed. The mean emission/capture times constant (τ) and current jump difference (ΔI_d) of the dominant trap are identified, as $\tau = 1.7$ ms and $\Delta I_d = 22.5$ nA. Introducing these parameters in a Lorentzian model [18] fairly reproduces the measured PSD in Fig. 3.

$$S_{id,RTN}(f) = \Delta I_d{}^2 \frac{4\tau^2}{\tau_e + \tau_c} \frac{1}{1 + (2\pi f \tau)^2} \quad (1)$$

where τ_e and τ_c refers to the emission and capture mean time constants extracted by averaging the time constants of the dominant trap levels in Fig. 4 (a).

The histogram distribution of i_d (t) further shows a maximum current fluctuation ΔI_d of about 50 nA at $\pm 3\ \sigma$. The time lag plot (TLP) of i_d (t) (Fig. 4b) clearly demonstrates a very large current spread around the mean value. After thermal annealing, the standard deviation of the histogram distribution is remarkably attenuated, with a maximum ΔI_d less than 25 nA at $\pm 3\ \sigma$ and the Lag plot shows an important shrink of the lobe. That confirms that the noise PSD decrease after annealing in Fig. 3 relates to the recovery of RTN due to oxide traps. As oxide defects highly influence the transistor's FoM (SS, I_{on}, g_m …) depending on their nature (e.g. trap number, position in space and energy…)

[20], [21], their neutralization by annealing is here finally confirmed to contribute to the recovery and stabilization of devices parameters.

IV. Conclusion

In-situ electro-thermal annealing was used to improve high-k thick gate oxide MOSFET performance in 28 nm FDSOI UTBB technology, through trap deactivation. After local annealing with maximum temperature of 590 K, a remarkable recovery of a defective "corner" transistor is observed in terms of SS, I_d and g_m figures of merit towards typical transistor characteristics. An important decrease of noise by more than one decade after annealing was further demonstrated. Close to V_{Th}, a Lorentzian 1/f^2 noise component was suppressed in PSD and multi-trap RTN signatures strongly attenuated in drain current time traces. As a result, noise measurements confirm the recovery of oxide trap-related device defects by in-situ annealing, leading to the improvement and stability of device performance, notably for analog applications.

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