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Determination of Carrier Lifetime in Silicon Using an Ultra-thin Al_2O_3/SiO_2 Dielectric Stack

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***Abstract*—This work investigates different Al_2O_3-based dielectric stacks for various applications, including surface passivation of solar cells and photodetectors, replacement of SiO_2 gate dielectric in advanced MOSFETs. Ultra-thin Al_2O_3/SiO_2 (3/2 nm) stacks were deposited on silicon by using different techniques. A reference sample with only a single dry-grown SiO_2 layer (3 nm) was prepared for comparison purpose. The effective carrier lifetimes were measured by the contactless photoconductance decay method. The lowest surface recombination velocity was calculated to be 34 cm/s in the Al_2O_3/SiO_2 stack. The negative fixed charge density in the stacks was extracted from C–V characteristics. Our results reveal that the effective carrier lifetimes depend on the stacks deposition techniques and conditions, and provide a guideline for optimization.**

Keywords—Effective carrier lifetime, ultra-thin dielectric stack, Al_2O_3/SiO_2, surface recombination velocity.

I. Introduction

Al_2O_3 material has been explored for many applications, including surface passivation in photovoltaics and photodetectors, gate dielectric in downscaling MOSFETs, etc. Al_2O_3 provides good passivation qualities for silicon. The negative fixed charges in Al_2O_3 induce an accumulation layer at the Si interface for *p*-type Si solar cell, shielding surface recombination and thereby increasing efficiency [1]. Recent works [2] have also demonstrated that Al_2O_3 is well suited for the field-effect passivation of *n*-type silicon substrate. It was proven [3] that an Al_2O_3/SiO_2 stack shows better performance than each material used individually. Particularly, the interfacial defect density was shown lower in the stack than in the SiO_2/Si case. The Al_2O_3/SiO_2 stacks produce very low surface recombination velocities (SRV) of less than 2 cm/s and the fixed charge density can be tuned with the SiO_2 layer thickness. In the field of photodetector, the surface recombination velocity and fixed charge density dominate the reverse leakage behavior of the photodiode [4]. Passivation of device surfaces is very important to achieve high performance of photodiodes. Al_2O_3 has also interesting anti-reflection properties. The Al_2O_3/SiO_2 stack should then be one of the considered candidates, especially for lateral photodiodes. SiO_2 is commonly used as the gate dielectric material in MOSFETs. With the scaling of the gate dielectric thickness down to 1-2 nm range, a single layer of SiO_2 faces many issues such as high gate leakage current, standby power consumption and gate oxide reliability [5]. The quality of the dielectric/Si substrate interface plays an important role in the nano-scaled device behavior and final performance. The carrier lifetime and surface recombination velocity are the main parameters to assess the intrinsic interface and dielectric quality. Al_2O_3 appears to be more attractive than other high-k replacements of SiO_2 due to its abundance, low cost and compatibility with CMOS technology. However, high trap density formed at the Al_2O_3/Si substrate increases the interface charge scattering, thereby decreasing the carrier mobility in the transistors' channel [6].

In this work, we investigate the carrier lifetime and surface recombination velocity of the ultra-thin Al_2O_3/SiO_2 stacks on silicon and compare them with that the SiO_2/Si counterpart. To this end, the ultra-thin Al_2O_3 was deposited by plasma enhanced atomic layer deposition (PE-ALD) or thermal atomic layer deposition (T-ALD) on either thermally grown high quality SiO_2 films (Samples 1 and 2, see TABLE I) or PE-ALD SiO_2 thin films (Samples 3 and 4). The photoconductance decay (PCD) technique [7] allows for a fast determination of the carrier lifetime without any electrical contact. It includes two operating modes: transient mode and quasi-steady-state mode. The former with a quick flash of light is especially suitable for long carrier lifetime cases while the later with a slow decay illumination for short carrier lifetimes. In this work, the PCD technique was used to measure the effective carrier lifetimes for the different fabricated dielectric stacks.

II. Experimental Details

Double side polished silicon wafers (FZ, *n*-type, <100>, 1–10 Ω.cm) were used as the starting substrates. After the standard RCA cleaning procedures, different dielectric stacks with the same equivalent oxide thickness (EOT) of 3 nm were symmetrically deposited on both sides of silicon wafers. The EOT of the stack is calculated by a two-capacitor in-series model written as below [8]:

$$\frac{EOT}{\varepsilon_{SiO_2}} = \frac{t_{IL}}{\varepsilon_{IL}} + \frac{t_{high-k}}{\varepsilon_{high-k}} \qquad (1)$$

Where ε_{SiO_2}, ε_{IL}, ε_{high-k} are the dielectric constants of SiO_2, interfacial layer, and high-k dielectric layer respectively, t_{IL} and t_{high-k} are the thicknesses of interfacial layer and high-k dielectric layer. In our work, the interfacial layer is SiO_2 and high-k dielectric layer is Al_2O_3. We prepared four types of dielectric stacks as shown in TABLE

I. A reference sample with 3-nm-thick SiO_2 layer was prepared for comparison purpose. The thermal SiO_2 thin films were grown at 900 °C in Koyo thermal system (Reference sample, Samples 1 and 2). The plasma enhanced atomic layer deposition (PE-ALD) SiO_2 thin films were obtained at 250 °C in Fiji F200 ALD system (Samples 3 and 4). The Al_2O_3 thin films were grown either by plasma enhanced atomic layer deposition (PE-ALD) at 200 °C (Samples 1 and 3) or by thermal atomic layer deposition (T-ALD) at 200 °C (Samples 2 and 4). In both cases, trimethylaluminum (TMA) precursor was used as aluminum source. Oxygen flow and water pulse were used as oxygen source for PE-ALD and T-ALD, respectively. The growth rate was 1 Å per cycle for both of them. The carrier lifetime measurements were performed by Sinton WCT-120 instrument. We used a white light illumination (the wavelength ranges from 400 to 700 nm), which can totally penetrate into the dielectric stacks.

TABLE I. TARGETED AND MEASURED THICKNESS OF SAMPLES (EOT = 3 nm)

Sample number	Dielectric stack	Targeted thickness (nm)	Measured Thickness[c] (nm)
Reference sample	Thermal SiO_2	3	3.9
Sample 1	PE-ALD[a] Al_2O_3 / thermal SiO_2	3 / 2	2.8 / 2.5
Sample 2	T-ALD[b] Al_2O_3 / thermal SiO_2	3 / 2	3.2 / 2.5
Sample 3	PE-ALD Al_2O_3 / PE-ALD SiO_2	3 / 2	3.7 / 2.5
Sample 4	T-ALD Al_2O_3 / PE-ALD SiO_2	3 / 2	3.5 / 2.5

[a.] PE-ALD: plasma enhanced atomic layer deposition.
[b.] T-ALD: thermal atomic layer deposition.
[c.] Measured thickness in nm is the average value of 16 points on one sample.

III. RESULTS AND DISCUSSION

A. Thickness uniformity of ultra-thin dielectrics

Fig. 1 plots the schematic cross-section of an Al_2O_3/SiO_2 stack. One of the key issues for depositing the ultra-thin dielectric stacks on silicon is to achieve a reproducible thickness, which guarantees uniformity of device characteristics. In order to examine the thickness uniformity of the dielectric stacks, a 3-inch silicon wafer was mapped cyclically by Ellipsometry. Fig. 2 shows the typical thickness distribution of a PE-ALD Al_2O_3 layer. The targeted thickness of the Al_2O_3 layer is 3 nm, while the measured average thickness is 2.8 ± 0.7 nm. If the edge region of the wafer is ignored, the standard deviation will be reduced. The thickness deviation may be due to the original roughness of the silicon wafer or to edge effects on wafer sides. It is worth noting that the thermal SiO_2 layer under Al_2O_3 is very uniform.

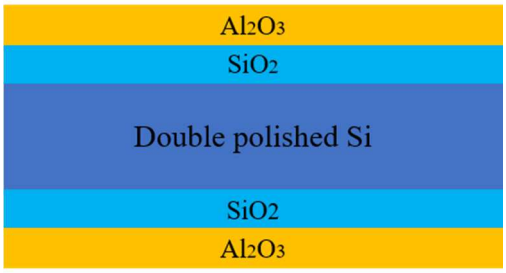

Fig. 1. Cross-section of a dielectric stack.

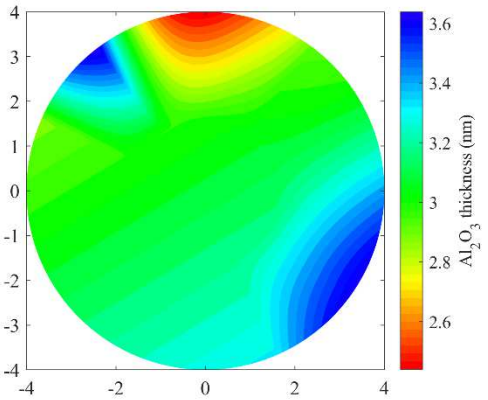

Fig. 2. Thickness distribution of a PE-ALD Al_2O_3 layer over a thermal SiO_2 layer, mapped cyclically by Ellipsometry.

B. Measurement of effective carrier lifetime

Nagel *et al*. [9] developed a generalized model to analyze the relationship between the effective carrier lifetime (τ_{eff}) and the excess carrier density (Δn) by illumination:

$$\tau_{eff}(\Delta n) = \frac{\Delta n}{G_{bulk} - \frac{\delta n}{\delta t}} \qquad (2)$$

Here G_{bulk} is the charge carrier generation rate. In the quasi-steady-state (QSS) case, $\frac{\delta n}{\delta t} \approx 0$, this gives

$$\tau_{eff.QSS}(\Delta n) = \frac{\Delta n}{G_{bulk}} \qquad (3)$$

By considering $G_{bulk} = 0$ in transient case, Equation (2) can be rewritten as:

$$\tau_{eff.trans}(\Delta n) = -\frac{\Delta n}{\frac{\delta n}{\delta t}} \qquad (4)$$

In our measurements of the effective carrier lifetime, both the QSS and transient modes were used. The measurement results obtained from both modes are similar. Fig. 3 illustrates the effective carrier lifetime as a function of the excess carrier density for four samples with different dielectric stacks and the reference sample with only a single SiO_2 layer. TABLE II summarizes the τ_{eff} values of the five cases for the excess carrier density of 5×10^{15} cm^{-3}.

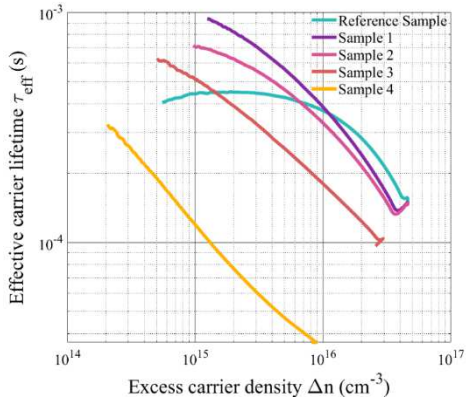

Fig. 3. Effective carrier lifetime vs. excess carrier density for the silicon samples with the different dielectric stacks of TABLE I, measured by using photoconductance decay technique.

TABLE II. EFFECTIVE CARRIER LIFETIME (τ_{eff}) AND CALCULATED EFFECTIVE SURFACE RECOMBINATION (S_{eff}) FOR DIFFERENT SAMPLES, THE VALUES FROM LIFETIME MEASUREMENTS ARE TAKEN AT Δn = 5 x 10^{15} cm^{-3}

Sample number	Dielectric stack	τ_{eff} (us) for Δn = 5×10^{15}cm^{-3}	S_{eff} (cm.s^{-1})
Reference sample	Thermal SiO_2	426	45
Sample 1	PE-ALD Al_2O_3 / thermal SiO_2	561	34
Sample 2	T-ALD Al_2O_3 / thermal SiO_2	460	41
Sample 3	PE-ALD Al_2O_3 / PE-ALD SiO_2	254	75
Sample 4	T-ALD Al_2O_3 / PE-ALD SiO_2	47	402

C. Calculation of surface recombination velocity

When the effective carrier lifetime (τ_{eff}) is obtained by the measurement as mentioned above, surface recombination velocity, S_{eff} can be calculated using the following Equation [10]:

$$S_{eff} = \frac{W}{2\tau_{eff}} - \frac{W}{2\tau_{bulk}} \qquad (5)$$

Where W is the silicon wafer thickness (W = 380 µm in this work). τ_{bulk} is the bulk carrier lifetime and it can be neglected due to the high quality of FZ wafer. In this case, Equation (5) can be approximated to

$$S_{eff} \leq \left(\frac{W}{2\tau_{eff}}\right) \qquad (6)$$

One should note that as the sample structure is symmetrical (i.e., the dielectric stack was deposited on both sides of the double side polished silicon wafer), the surface recombination velocity is identical for the front and back surfaces ($S_{front} = S_{back} = S_{eff}$). Therefore, hereafter S_{eff} refers to the effective surface recombination velocity.

Fig. 4 plots the S_{eff} as a function of Δn curves for the samples with different dielectric stacks and the reference sample. The S_{eff} values are calculated using Equation (6) with the measured τ_{eff} values shown in Fig. 3. TABLE II provides the typical S_{eff} values taken at $\Delta n = 5 \times 10^{15}$ cm^{-3}.

In comparison to the PE-ALD Al_2O_3/PE-ALD SiO_2 and T-ALD Al_2O_3/PE-ALD SiO_2 samples, the PE-ALD Al_2O_3/thermal SiO_2 and T-ALD Al_2O_3/thermal SiO_2 samples feature lower effective surface recombination velocity and higher effective carrier lifetimes. This could be explained by the fact that plasma makes the silicon surface rough during PE-ALD SiO_2 process [11]. In other words, the thermal SiO_2 layer can protect the silicon surface from damage. Therefore, the deposition method of the ultra-thin interfacial layer SiO_2 is crucial for the stack fabrication.

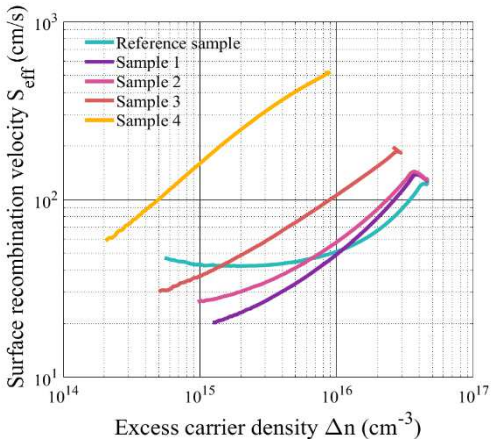

Fig. 4. Calculated effective surface recombination velocity vs. excess carrier density for the silicon samples with different dielectric stacks and the reference sample with only SiO_2.

Fig. 5 shows the C-V characteristics for the reference sample and Sample 1 measured at 1 kHz. According to the flatband voltages in the figure, the fixed charge densities (Q_f) are extracted to be $+1.36\times10^{10}$ and -2.54×10^{10} cm^{-2} for the reference sample and Sample 1, respectively. Although the equivalent oxide thickness is reduced down to 3 nm, the negative fixed charge density was still obtained in the ultra-thin PE-ALD Al_2O_3/thermal SiO_2 stack (2.8/2.5 nm).

From Fig. 3 and 4, we can also see that when $\Delta n < 1\times10^{16}$ cm^{-3}, the effective surface recombination velocity is lower in the PE-ALD Al_2O_3/thermal SiO_2 and T-ALD Al_2O_3/thermal SiO_2 samples than in the reference sample. This indicates that the ultra-thin stack of the ALD-Al_2O_3/thermal SiO_2 shows better field-effect passivation for silicon compared with a single thin SiO_2 layer. Dingemans et al. [12], [13] fabricated two stacks with different thickness of ALD-Al_2O_3 and thermal SiO_2. Stack 1 and 2 were composed Al_2O_3/SiO_2 (30/1 nm) and Al_2O_3/SiO_2 (5/10 nm). With injection levels (Δn) of 5×10^{14} and 1×10^{14} cm^{-3}, the surface recombination velocities (S_{eff}) were measured to about 17 and 3 cm/s for Stack 1 and 2, respectively. Their S_{eff} values depend on the choice of the injection level (Δn). As shown in Fig. 4, if the injection level was extended into $\Delta n = 1\times10^{14}$ cm^{-3}, our S_{eff} values are approach to Dingemans's results. To further increase effective carrier lifetime and decrease S_{eff} value, we could active the negative fixed charges in the stacks at optimized temperature in forming gas or ozone. We also can adjust SiO_2

or Al_2O_3 thickness. However, the other performance of the ultra-thin stack, such as interface trap state density and leakage current should be further investigated in the future.

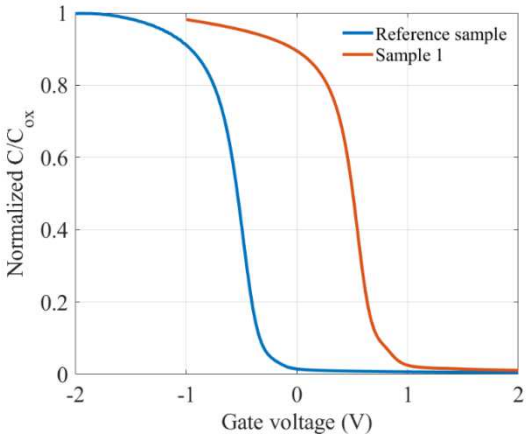

Fig. 5. Normalized C-V characteristics of the reference sample and sample 1 at 1 kHz.

IV. Conclusion

We have demonstrated that, compared with a single ultra-thin SiO_2 layer (3 nm), the ultra-thin Al_2O_3/SiO_2 (3/2 nm) stack allows to decrease the effective surface recombination velocity (increase effective carrier lifetime) at lower injection level ($\Delta n < 10^{16}$ cm^{-3}). This is suggested to be related to electric-field passivation caused by negative fixed charges in Al_2O_3. Importantly, the growth method and condition of the ultra-thin Al_2O_3 and SiO_2 layers are crucial for the stack preparation.

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