Time Dependence of RF Losses in GaN-on-Si Substrates

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***Abstract*— GaN-on-Si HEMT technology suffers from RF losses and non-linearities originating from the conductive Si substrate. The understanding and modeling of substrate performance are the keys to enabling next-generation front-end modules. In this letter, we show that when subjected to a chuck bias step, the effective substrate resistivity of a typical *C*-doped HEMT stack shows a dynamic behavior. Using a dedicated setup, stress/relaxation sequences at different temperatures are performed to understand this phenomenon. With the help of TCAD simulations, it is shown that redistribution of charges trapped in deep defects located in the III-N buffer can qualitatively explain the observed trends. Trap activation energies of 0.43 and 0.33 eV are extracted from measured data.**

***Index Terms*— *C*-doped buffers, CPW lines, effective substrate resistivity, GaN-on-Si, RF losses, traps.**

I. Introduction

GaN-on-Si HEMT technology is seen as a promising candidate for 5G and beyond front-end modules. It could combine the attractive material properties of GaN with the use of low-cost, large-area Si wafers [1]. However, the use of a Si substrate brings additional challenges compared to other materials such as SiC. In particular, the conductive nature of Si leads to increased substrate crosstalk, RF losses, and non-linearities [2]. It is generally assumed that losses and non-linearities originate from a parasitic surface conducting (PSC) layer located close to the Si surface. This channel is formed by diffusion of Al and Ga atoms (p-type dopants in Si) during high-temperature III-N growth [3].

A GaN-on-Si HEMT stack typically contains a multilayered semi-insulating III-N buffer. To increase its resistivity, the top buffer layers can be doped by a high concentration of Fe or C atoms. These dopants create deep traps throughout the buffer, which can alter the functioning of overlying HEMTs. For instance, the dynamic ON-state resistance (R_{ON}) dispersion phenomenon has been linked to charge trapping in the buffer of *C*-doped III-N stacks [4]–[6].

Deep buffer traps can also affect substrate RF performance. In [7], it was shown that slow charging and discharging of defects in the upper III-N layers could create strong hysteresis in the bias-dependence of substrate effective resistivity (ρ_{eff}) [8]. This complicates the prediction of substrate harmonic distortion (HD) compared to Silicon-on-Insulator (SOI) technology, where HD can be linked to ρ_{eff} and its bias dependence [2].

In this work, we show that deep buffer traps can also lead to a "dynamic ρ_{eff}" effect. By tracking RF losses during a chuck bias stress/relaxation sequence, ρ_{eff} is seen to vary by a factor that can exceed two with time constants exceeding several hundreds of seconds. With the help of TCAD simulations, this behavior is linked to the redistribution of trapped charges inside the *C*-doped III-N layers.

II. Experimental Details

A. Substrate Fabrication and Processing

The III-N stack studied in this work was grown using a Veeco Turbodisc Maxbright MOCVD reactor on a 200-mm, 3-6-k$\Omega \cdot$ cm CZ-Si wafer [9] [Fig. 1(a)]. It comprises an AlN nucleation layer ($\sim$175 nm), followed by a $\sim$2.2-μm-thick carbon-doped superlattice buffer, and finally, a $\sim$300-nm GaN channel. No barrier was grown on the channel in order to avoid any 2-D electron gas (2DEG) formation.

Following the growth, CPW lines were patterned on the semiconducting stack. They consist of a $\sim$10/500-nm thick Ti/Al stack.

B. Measurement Techniques

On-wafer measurements were carried out in dark conditions on a temperature-controlled chuck. To track the time evolution of ρ_{eff} in reaction to a chuck bias step, a custom setup was developed [Fig. 1(b)]. Chuck bias and vector network analyzer (VNA) trigger were synced by the controller PC, which also tracks stress and relaxation time. The time resolution of this setup is of $\sim$100 ms, corresponding to the sum of PC-VNA communication, data acquisition and saving times. A limited number of frequency points were measured around a frequency $f_0 = 2$ GHz to reduce the VNA acquisition time associated with a full frequency sweep.

C. Simulation Framework

A simple TCAD model of the III-N epi stack was implemented to understand the physics behind ρ_{eff} transients [10].

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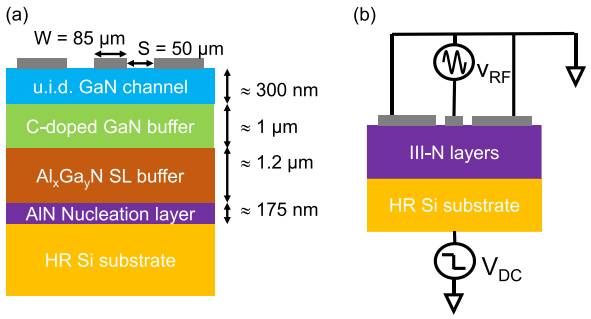

Fig. 1. (a) III-N Epi stack studied in this work. To avoid 2DEG formation, no Al(Ga)N barrier was grown on top of the GaN channel. (b) Measurement procedure: An RF small-signal (V_{RF}) is applied by the VNA on the CPW line and superposed on the dc stepping of chuck bias (V_{DC}). A controller script synchronizes the two instruments while also acting as a chronometer.

In this model, the complex buffer is represented by three successive layers.

1) 175-nm AlN nucleation layer.
2) 2.2-μm C-doped (10^{18} cm^{-3}) Al_xGa_yN buffer. The molar fraction and permittivity were set to the average of the different layers (1-μm GaN and 1.2-μm superlattice).
3) 300-nm GaN channel.

C doping was modeled as a dominant acceptor trap level ($E_t = E_v + 0.9$ eV) compensated by shallow donor traps (compensation ratio: 50%) [6]. Metallic contacts were defined on top of the structure according to CPW dimensions used in the experiment. Default drift-diffusion and SRH recombination models were used in these simulations.

III. Results and Discussion

A. Experimental Relaxation Transients

At 25 °C and prior to any stress, the considered GaN-on-Si stack showed a $\rho_{eff} = 1.4$ k$\Omega \cdot$ cm (for $f_0 = 2$ GHz, not shown). The sample was subjected to a chuck bias stress ($V_{stress} = \pm 50$ V) during 300 s, after which ρ_{eff} came to equilibrium. After switching back the chuck bias to 0 V, the sample was allowed to relax for up to 5000 s, during which ρ_{eff} was monitored at logarithmically spaced intervals. Relaxation curves showing ρ_{eff} versus time for the two V_{stress} situations are displayed in Fig. 2 as a function of temperature. Note that data points at 25 °C were omitted as they did not reach equilibrium after 5000 s. Values of ρ_{eff} normalized to the final data point are plotted to remove the effect of ρ_{eff} decrease with increasing temperature. Indeed, for lowly doped Si substrates, an increase in temperature of the intrinsic carrier density n_i will increase bulk Si conductivity, lowering ρ_{eff} [11].

From Fig. 2, it can first be observed that ρ_{eff} relaxation times can exceed 1000 s at 50 °C. Second, relaxation transients are non-monotonous and pass through either maxima or plateaus. The occurrence of these features corresponds to shorter times as temperature increases, pointing to a thermally activated mechanism.

B. Charge Balance in III-N Stacks

In GaN-on-Si stacks, the bias applied on the chuck must be compensated by the charge located inside the semiconductor stack.

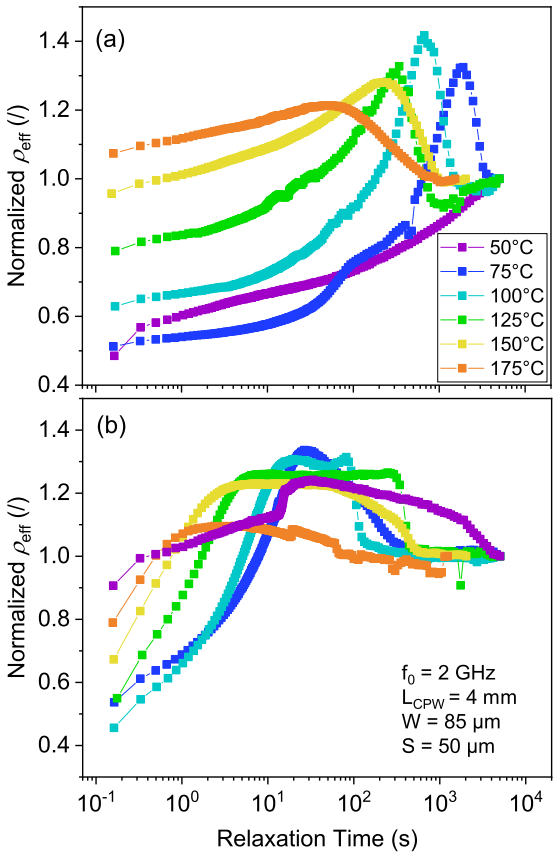

Fig. 2. Experimental normalized ρ_{eff} relaxation transients after a 300 s stress at (a) $V_{stress} = +50$ V and (b) $V_{stress} = -50$ V. Relaxation times can exceed 1000 s, and curve features are temperature dependent.

Compensation charge can originate from different contributions.

1) Mobile carriers in Si: Q_{Si}.
2) Ionized traps in III-N layers, in particular, C-related traps: Q_{buffer}.

These contributions are associated with different response times. In Si, free carriers redistribute in response to a bias change according to successive mechanisms. Details can be found elsewhere [12], but Q_{Si} typically reaches equilibrium after 10–100 ms, comparable to the time resolution of the experimental setup. In the resistive III-N layers where free carrier concentration does not exceed 10^5 cm^{-3}, the main charge compensation mechanism is the charging and discharging of buffer traps. In reaction to a change in substrate bias, trapped charge redistributes across the C-doped buffer, as shown by simulation data in Fig. 3 for a 1-D stack. For $t_{relax} < 0$, the stress condition $V_{stress} = -50$ V attracts positive charge toward the bottom of the structure. When chuck bias is switched from -50 to 0 V (relaxation phase), traps close to the bottom and top of the buffer emit and capture holes (making them more and less negatively charged), respectively. This redistribution takes place in a few tens of seconds at 25 °C. In the PSC layer, free carriers governing ρ_{eff} react instantaneously (i.e., in less than ~100 ms) to the slow change in Q_{buffer} shown in Fig. 3. In Fig. 4, the surface-free carrier concentration is tracked during the relaxation phase. The inclusion of C doping in the buffer slows down drastically the PSC layer response to the bias step: equilibrium is reached after ~20 s when C traps

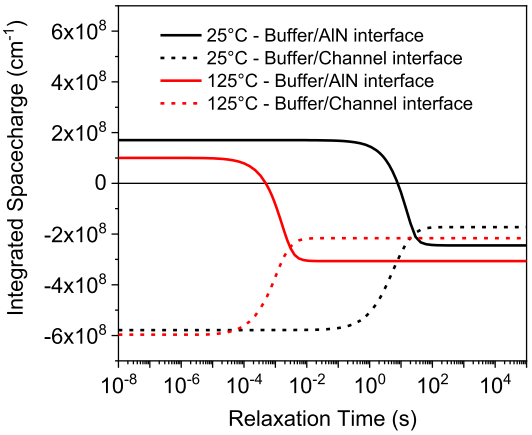

Fig. 3. Simulated evolution of spacecharge (main contributor: C traps) in upper (dashed) and lower (continuous) regions of the C-doped buffer during relaxation phase (for negative times, Vstress = -50 V).

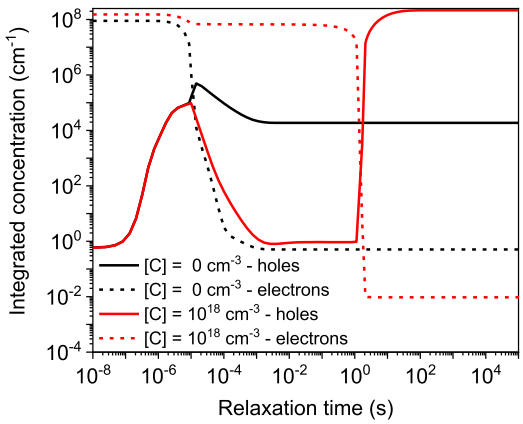

Fig. 4. Simulated relaxation transients ($V_{\text{stress}} = -50$ V) for a 1-D stack. The evolution of free carrier concentration close to Si surface (integrated over a 1 μm deep region) is highly dependent on the inclusion of C traps in the III-N buffer.

are included instead of a few ms for the undoped stack. Non-monotonous evolution of free carrier concentration similar to what appears in Fig. 4 can also be observed in simulations of SOI structures [12].

C. Linking ρ_{eff} Maxima and Trap Properties

Free carrier concentration in the PSC layer dictates its conductivity, and thus ρ_{eff}. To illustrate this, a combined small-signal and transient simulation of a CPW line is performed in Fig. 5. The extracted ρ_{eff} shows a similar non-monotonous, temperature-dependent relaxation transient as observed in measurements. It can be verified that a maximum in ρ_{eff} corresponds to a depleted PSC layer. The times corresponding to simulated ρ_{eff} maxima follow an Arrhenius dependence with an activation energy $E_a = 0.89$ eV, corresponding to E_t of the carbon traps used as input in the simulation (not shown). Adjusting the trap cross-section shifts the curves in Fig. 5, possibly allowing a more precise match to experiments.

Applying the same procedure on experimental curves, activation energies of 0.43 and 0.33 eV are obtained for V_{stress} of $\pm$50 V, respectively (Fig. 6). Although different from the 0.9 eV defect energy used in simulations, these energies are in the range of values found in the literature for C-related defects, which can be of various configurations [13].

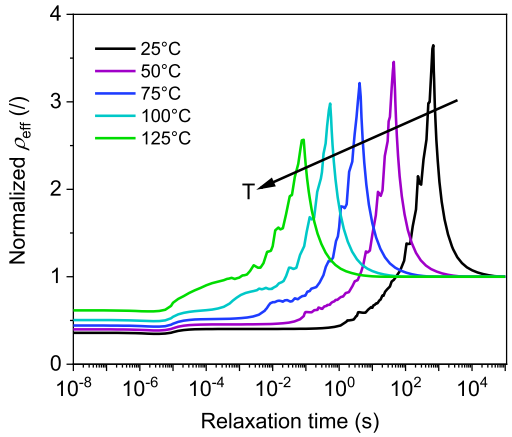

Fig. 5. Simulated ρ_{eff} relaxation transients ($V_{\text{stress}} = -50$ V) for a CPW structure. Temperature-dependent maxima are observed, similar to experiments.

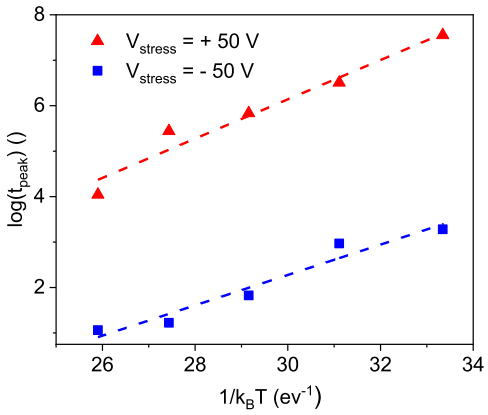

Fig. 6. Arrhenius plot of times corresponding to ρ_{eff} maxima in experimental relaxation transients shown in Fig. 2. Activation energies of 0.43 eV ($V_{\text{stress}} = +50$ V) and 0.33 eV ($V_{\text{stress}} = -50$ V) are extracted.

Furthermore, different stress bias conditions have been found to excite buffer defects of different nature [5].

D. Reliable HD Measurements and Modeling

In general, substrate HD is directly correlated with its ρ_{eff}. For GaN-on-Si stacks, the significant time dependence of ρ_{eff} needs to be considered when reporting HD. Indeed, a change in ρ_{eff} by a factor of 2 (such as observed in Fig. 1) could lead to a difference of up to 8.5 dB in the second harmonic (H2) according to [2]. As a consequence, measured HD levels should be reported after complete relaxation and trapping effects discussed here for reliable HD modeling.

IV. Conclusion

In this letter, stress/relaxation sequences were used to characterize the transient behavior of RF losses in a GaN-on-Si HEMT stack. It was shown that relaxation times in reaction to a chuck bias step can exceed 1000 s, during which ρ_{eff} can vary by a factor of 2. The temperature dependence of non-monotonous features was linked to the redistribution of charge trapped in deep levels of the C-doped III-N buffer.

Finally, properly considering transient phenomena was shown to be necessary for accurate substrate non-linearities characterization and modeling in GaN-on-Si substrates.

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