Accurate SOI MOSFET Characterization at Microwave Frequencies for Device Performance Optimization and Analog Modeling

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***Abstract*— The maturation of low-cost silicon-on-insulator (SOI) MOSFET technology in the microwave domain has brought about a need to develop specific characterization techniques. An original scheme is presented, which, by combining careful design of probing and calibration structures, rigorous *in situ* calibration, and a new powerful direct extraction method, allows reliable identification of the parameters of the non-quasi-static (NQS) small-signal model for MOSFET's. The extracted model is shown to be valid up to 40 GHz.**

***Index Terms*— Integrated circuit measurements, microwave measurements, MOSFET's, scattering parameters measurements, silicon-on-insulator technology.**

I. Introduction

SILICON-ON-INSULATOR (SOI) MOSFET's exhibit interesting features such as higher current drive [1] and lower parasitic source and drain capacitances [2] compared to bulk silicon MOSFET's, which allow SOI circuits to offer excellent high-frequency performances. MMIC technologies offering a complete range of active and passive devices have been developed combining CMOS processing with high-resistivity wafers (5000 and 10 000 $\Omega\cdot$cm) [3], [4]. The maturation of low-cost SOI MOSFET technology in the microwave domain has brought about a need to develop specific characterization techniques. Characterization at microwave frequencies relies on scattering (S-) parameters measurements. However, description of the measured frequency response in terms of an equivalent circuit is much more useful, both for analog design and performance analysis. In particular, choosing the equivalent circuit topology so as to reflect the underlying physics of the device, one may significantly simplify the characterization and the modeling tasks. This approach is advocated by several authors [5], [6], and one of the most striking examples of it is the F50 method from [7], which allows to fully characterize the noise behavior of FET's, using only one noise measurement at the bias point of interest together with a "physical" equivalent circuit.

To benefit from the advantages of physical modeling using on-wafer S-parameters measurements, one must be able to identify correctly the equivalent circuit elements of a device that is representative of what will be used in functional circuitry. This imposes constraints on the design of the probing structure, on the deembedding and the parameter-extraction procedures. It is the purpose of this paper to present the original solutions that were developed for the characterization of SOI MOSFET's up to 40 GHz.

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II. Measurement Procedure

The MOSFET's to be characterized are embedded in a coplanar waveguide structure designed to minimize the ground inductance. Using standards implemented on the SOI wafer, a through-reflect-line (TRL) calibration is performed according to the algorithm of [8]. As a result, the reference planes are positioned close to the devices, effectively reducing the input and output shunt capacitances. To allow accurate conversion of S-parameters to admittance (Y) or impedance (Z) parameters, the reference impedance of the calibration is determined using the method of [9]. The strength of this procedure is that it is based on the general purpose TRL algorithm, which is well documented and renown for its accuracy. It remedies to the fundamental limitations of the widely-used deembedding methods proposed by [10] and [11]. These deembedding methods are primarily intended for small devices. They omit to take the parasitics of the calibration devices themselves into account so that the correction is generally overestimated. The net result is an artificial reduction of some parasitic elements of the devices under test (DUT). This effect becomes nonnegligible when the active zone of the DUT has a large periphery, as is the case for microwave MOSFET's.

III. Device Fabrication and Modeling

Thin-film SOI MOSFET's are fabricated with a CMOS-compatible process on low-resistivity (20 $\Omega\cdot$cm) SIMOX wafers. The initial 200-nm silicon film is thinned down to about 100 nm by oxidation and oxide strip. After a semi-recessed LOCOS isolation step, a 30-nm gate oxide

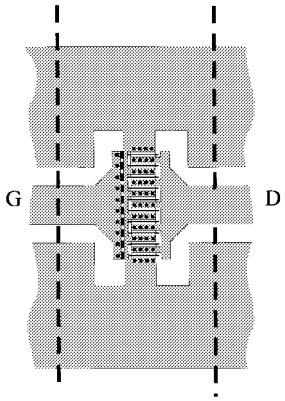

Fig. 1. Layout view showing a MOSFET with $W = 240\,\mu$m, $L_{\rm eff} = 0.5\,\mu$m, and ten gate-fingers, embedded in the probing structure. The reference planes are materialized by the vertical dashed lines.

is grown and boron is implanted to adjust the n- and p-channel threshold voltages. A 340-nm thick polysilicon is then deposited, doped (implantation, As, 100 keV, 1×10^{16} cm^{-2}), and patterned. Arsenic (80 keV, 4×10^{15} cm^{-2}) and boron (20 keV, 5×10^{15} cm^{-2}) are implanted to form the source/drain regions, followed by an RTA (950 °C, 40 s) activation step. Then, a 150-nm thick SiO_2-layer is deposited and etched by RIE to form spacers. After a short-time 2% HF dip, either a titanium or a nickel layer, or a titanium/cobalt stack layer is deposited using an e-gun system with thicknesses of 30, 25, or 7 nm/13 nm, respectively. The conventional two-step SALICIDE process is used for titanium [12]–[14] and cobalt [15] silicidation (Ti: 675 °C, 45 s and 900 °C, 15 s; Ti/Co bilayer: 675 °C, 45 s and 900 °C, 30 s). Nickel monosilicide [16], [17] is formed with a one-step annealing at 550 °C for 40 s. Unreacted metals are selectively removed by a $H_2\,SO_4 + H_2\,O_2$ (2 : 1) mixture. A nitride/oxide layer is then deposited and contact holes are opened to access the devices. An aluminum metallization is used to complete the process. The gate sheet resistance of the wafers with $TiSi_2$, $CoSi_2$, and NiSi are 6.2, 4.4, and 2.8 Ω/square, respectively. In order to obtain optimized high-frequency performances, a ten-fingers comb-like gate structure is used for the microwave MOSFET design. Fig. 1 shows a common source MOSFET embedded in the microwave probing structure.

The model used for the common-source SOI MOSFET in saturation is shown in Fig. 2. According to the physical meaning attributed to the elements, the circuit can be split into three parts.

1) Index "i" denotes the intrinsic elements which model the useful transistor effect, and are thus dependent on the bias conditions and on the size of the active zone. In agreement with the theory from [18] and the experimental evidence from [19], a non-quasi-static (NQS) formulation is adopted, in order to account for channel propagation delays, and thus extend the validity of the model at least up to the cutoff frequency of the MOSFET's.
2) Index "e" denotes the extrinsic elements, which are independent of bias, but scale with the active zone. In particular, $R_{\rm se}$ and $R_{\rm de}$ can be expected to be constant versus bias in view of the drain and source fabrication technology used.
3) Index "a" denotes the shunt admittances caused by the metal connections just outside of (adjacent to) the active zone. The frequency behavior of these admittances is determined by the characteristics of the SOI substrate. It is constant under normal biasing conditions, and not dependent on the width of the active zone.

In agreement with these definitions, the equations corresponding to the circuit of Fig. 2 are shed into the following form for subsequent developments as in (1)–(4), shown at the bottom of the page, where $\boldsymbol{Y}_\mu$ is the Y-matrix measured at the reference planes.

IV. Extraction Method

In order to identify the equivalent circuit elements in a reliable manner, an original direct extraction procedure has been set up. It extends the applicability of the approach recently proposed by Lee *et al.* [20] to the NQS small-signal model for MOSFET's.

The method developed by Lee *et al.* allows to determine all the series extrinsic elements from small-signal measurements at a single bias point, and hence to deembed the matrix $\boldsymbol{Y}_\pi$. It is based on a quasi-static (QS) formulation of the MOSFET model, so that the influence of $R_{\rm gsi}$ and τ is not accounted for explicitly in the developments. The result is that the extracted values for the series extrinsic circuit elements become bias-dependent under the influence of the NQS effects, which are not negligible even at a few GHz.

$$[Y_\mu - Y_\alpha]^{-1} = Z_\sigma + Y_\pi^{-1} \triangleq Z_{\sigma\pi} \tag{1}$$

$$Y_\alpha = \begin{bmatrix} Y_{\rm ga} & 0 \\ 0 & Y_{\rm da} \end{bmatrix} \tag{2}$$

$$Z_\sigma = \begin{bmatrix} R_{\rm ge} + R_{\rm se} & R_{\rm se} \\ R_{\rm se} & R_{\rm de} + R_{\rm se} \end{bmatrix} + j\omega \begin{bmatrix} L_{\rm ge} + L_{\rm se} & L_{\rm se} \\ L_{\rm se} & L_{\rm de} + L_{\rm se} \end{bmatrix} \tag{3}$$

$$Y_\pi = \begin{bmatrix} j\omega\left(\dfrac{C_{\rm gsi}}{1 + j\omega R_{\rm gsi} C_{\rm gsi}} + C_{\rm gse} + C_{\rm gde}\right) & -j\omega C_{\rm gde} \\ \dfrac{G_{\rm mi} \cdot e^{-j\omega\tau}}{1 + j\omega R_{\rm gsi} C_{\rm gsi}} - j\omega C_{\rm gde} & G_{\rm dsi} + j\omega(C_{\rm dse} + C_{\rm gde}) \end{bmatrix} \tag{4}$$

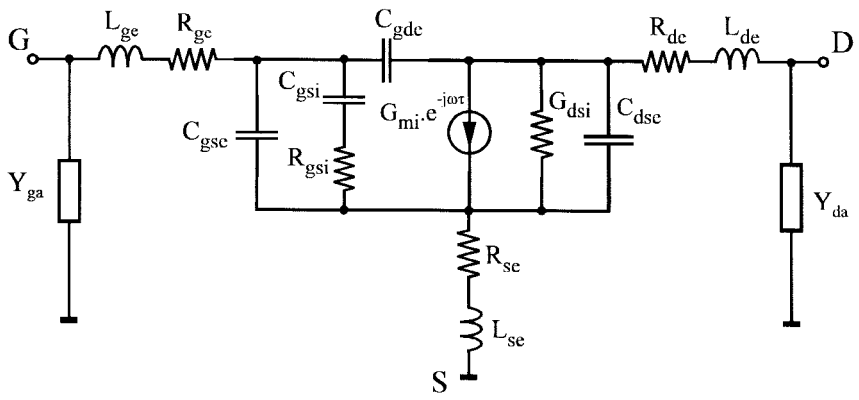

Fig. 2. Small-signal equivalent circuit model for a common-source SOI MOSFET in saturation.

To assess the limits of the applicability of the QS extraction scheme, extractions were performed on S-parameter data generated using the NQS equivalent circuit of Fig. 2 in a band stopping at 15 GHz. Several sets of circuit element values where used, corresponding to device widths ranging from 60 to 240 μm and bias-points with $V_{\rm gs} = V_{\rm ds}$ varying from 0.5 to 3 V. Extrinsic and intrinsic elements were obtained according to the method detailed in Section IV-B. The extracted values (denoted by $'$) were compared to the original circuit element values used to generate the S-parameter data set. Amongst the series extrinsic elements, $R'_{\rm ge}$, $R'_{\rm de}$, $L'_{\rm ge}$, $L'_{\rm de}$, and $L'_{\rm se}$ suffered less than 10% error with respect to their original values; $R'_{\rm se}$ was found to increase up to 150% of the original $R_{\rm se}$. The extracted values of the shunt extrinsic elements, $C'_{\rm gse}$, $C'_{\rm dse}$, $C'_{\rm gde}$, as well as all QS intrinsic elements and even τ' showed only a small error, below 2%. $R'_{\rm gsi}$ was affected by errors on the order of 75%. The sensitivity of the extracted intrinsic elements values with respect to a perturbation of the series extrinsic elements and to S-parameters measurement errors was also investigated. The results of this analysis show that the extraction scheme based on the QS approximation can be used up to 15 GHz in order to estimate the following parameters with reasonable accuracy: $C_{\rm gsi}$, $G_{\rm mi}$, $G_{\rm dsi}$, $C_{\rm gse}$, $C_{\rm gde}$, and $C_{\rm dse}$ and above 15 GHz to extract τ.

In accordance with these findings, the new extraction procedure proceeds as follows: determination of the feed admittances; extraction of the intrinsic and shunt extrinsic elements in the QS framework, determination of the NQS elements, and correction of the series extrinsic elements.

A. Gate and Drain Feed Admittances

To evaluate $Y_{\rm ga}$ and $Y_{\rm da}$, the dependency of the measured admittance matrix $\boldsymbol{Y}_\mu$ is considered in function of the width of the active zone (W_f), which is equal to the total width (W) divided by the number of gate fingers

$$Y_\mu(W_f) = Y_\alpha + Y_{\sigma\pi}(W_f). \tag{5}$$

In particular, for transistors measured in deep depletion at $V_{\rm ds} = 0$ V, one can reasonably assume that $\boldsymbol{Y}_{\sigma\pi}$ is directly proportional to W_f. So that the elements of $\boldsymbol{Y}_\alpha$ can be obtained from a linear regression on the elements of $\boldsymbol{Y}_\mu$ measured on transistors of varying W_f. The advantage of this procedure is that it is not necessary to postulate any specific frequency behavior for the gate and drain feed admittances. In the vicinity of dielectric relaxation frequencies of the substrate, this behavior can be quite complex, and accurate modeling of these effects is out of the scope of this article. Fig. 3 illustrates the application of this method. Three transistors were measured, having all ten gate fingers, a 0.5-μm effective channel length, and active zone widths equal to 6, 12, and 24 μm. The plotted capacitances $C_{\mu g}$, $C_{\mu d}$, and $C_{\mu \rm gd}$ were obtained by fitting the slope of, respectively, $Im(Y_{\mu 11} + Y_{\mu 12})$, $Im(Y_{\mu 22} + Y_{\mu 21})$, and $-Im(Y_{\mu 21})$ versus frequency, in the band from 3 to 20 GHz. The evolution of these capacitances is almost exactly linear in function of W_f. The fact that the $C_{\mu \rm gd}$ curve crosses the origin corroborates the assumption that the off-diagonal elements of $\boldsymbol{Y}_\alpha$ are zero.

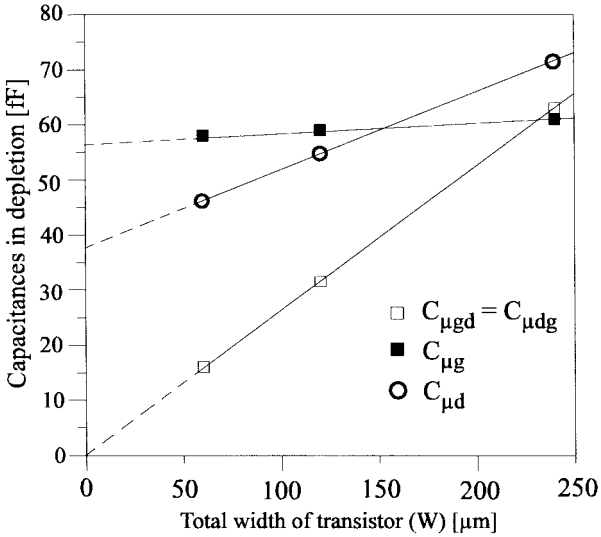

Fig. 3. Evolution of the total capacitances measured in depletion for various active zone widths (W_f).

B. Quasi-Static Modeling

In agreement with the work of Seonghearn *et al.* [20], the following analytical expressions are derived from (1) in the quasi-static case (developments are shown in detail in the

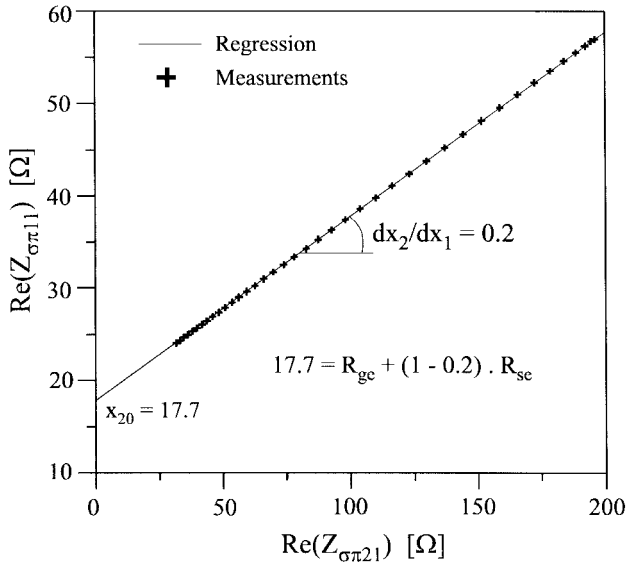

Fig. 4. Parametric plot of resistances in the 0.5–40 GHz band for a nMOSFET with $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 2$ V.

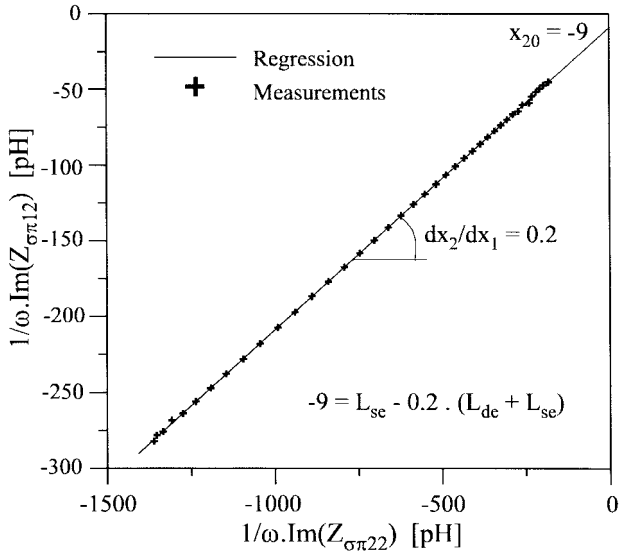

Fig. 5. Parametric plot of inductances in the 0.5–40 GHz band for a nMOSFET with $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 2$ V.

Appendix)

$$\mathrm{Re}(Z_{\sigma\pi \mathrm{ij}}) = \mathrm{Re}(Z_{\sigma \mathrm{ij}}) + \frac{A_{\mathrm{ij}}}{\omega^2 + B} \quad \text{for } i, j \in \{1, 2\} \tag{6}$$

$$\frac{1}{\omega} \cdot \mathrm{Im}(Z_{\sigma\pi \mathrm{ij}}) = \frac{1}{\omega}\mathrm{Im}(Z_{\sigma \mathrm{ij}}) - \frac{E_{\mathrm{ij}}}{\omega^2 + B} - \frac{F_{\mathrm{ij}}}{\omega^2 \cdot (\omega^2 + B)} \quad \text{for } i, j \in \{1, 2\} \tag{7}$$

where B, A_{ij}, E_{ij}, and F_{ij} are real and frequency independent expressions involving only the intrinsic and shunt extrinsic elements.

All series resistances and inductances can thus be obtained from the asymptotic values taken by (6) and (7) at infinite frequency. In order to evaluate these asymptotic values, the authors of [20] use an optimizer to fit the expressions on the right-hand side of (6) and (7) individually to the evolutions of measured data over the available frequency band. It is however possible to transform the determination of the asymptotic values into simple linear regression problems.

In the case of the series resistors, this is done by considering the parametric curves defined in a two-dimensional plane $[x_1, x_2]$ by $\{\mathrm{Re}[Z_{\sigma\pi \mathrm{ij}}(\omega)], \mathrm{Re}[Z_{\sigma\pi \mathrm{kl}}(\omega)]\}$, where $\{i, j\} \neq \{k, l\}$. Using (6), it is straightforward to establish that these curves must be straight lines, and that their intercept at the origin $[0, x_{20}]$ and slope dx_2/dx_1 is given by

$$x_{20} = \mathrm{Re}(Z_{\sigma k l}) - \frac{A_{\mathrm{kl}}}{A_{\mathrm{ij}}} \cdot \mathrm{Re}(Z_{\sigma \mathrm{ij}}) \tag{8}$$

$$\frac{dx_2}{dx_1} = \frac{A_{\mathrm{kl}}}{A_{\mathrm{ij}}}. \tag{9}$$

Substituting the values of the intercept and the slope obtained from a linear regression on the measured data points into (8) and (9) yields a linear equation relating the series resistances. Combining three such equations formed by varying the indices i, j, k, l, it is possible to construct a fully determined set of linear equations from which the series resistances can be determined. The most reliable results are obtained from measurements of saturated MOSFET's and with the following pairs: $[\mathrm{Re}(Z_{\sigma\pi 21}), \mathrm{Re}(Z_{\sigma\pi 11})]$, $[\mathrm{Re}(Z_{\sigma\pi 21})\mathrm{Re}(Z_{\sigma\pi 12})]$, and $[\mathrm{Re}(Z_{\sigma\pi 12}), \mathrm{Re}(Z_{\sigma\pi 22})]$. Fig. 4 illustrates the quality of the linear regressions performed on data measured from 500 MHz to 40 GHz.

For the series inductances the situation is a little different, because of the more complicated frequency behavior of the right hand side in (7), when $j = 1$. As can be seen in Fig. 5, the pair $[\mathrm{Im}(Z_{\sigma\pi 22})/\omega, \mathrm{Im}(Z_{\sigma\pi 12})/\omega]$ produces one useful equation based on the following relations:

$$x_{20} = L_{\mathrm{se}} - \frac{E_{12}}{E_{22}} \cdot (L_{\mathrm{de}} + L_{\mathrm{se}}) \tag{10}$$

$$\frac{dx_2}{dx_1} = \frac{E_{12}}{E_{22}}. \tag{11}$$

A second equation can be obtained by considering the parametric curve defined in the three-dimensional space $[x_1, x_2, x_3]$ by $[\mathrm{Im}(Z_{\sigma\pi 21})/\omega, \mathrm{Im}(Z_{\sigma\pi 12})/\omega, \mathrm{Im}(Z_{\sigma\pi 11})/\omega]$ measured on the saturated MOSFET. Equation (7) imposes that this curve is contained in a plane, of which the intercept at the origin $[0, 0, x_{30}]$ and the slope coefficients dx_3/dx_1 and dx_3/dx_2 can be determined from a linear regression on the measured data

$$x_{30} = L_{\mathrm{ge}} + L_{\mathrm{se}} \cdot \left[1 - \frac{F_{11}}{F_{21}} - \left(\frac{E_{11}}{E_{12}} - \frac{F_{11}E_{21}}{F_{21}E_{12}}\right)\right] \tag{12}$$

$$\frac{dx_3}{dx_1} = \frac{F_{11}}{F_{21}}; \quad \frac{dx_3}{dx_2} = \frac{E_{11}}{E_{12}} - \frac{F_{11}E_{21}}{F_{21}E_{12}}. \tag{13}$$

At this point, it is not possible to combine the measured curves to produce a third linearly independent equation to form a fully determined set of equations. However, extractions of the series inductances performed on depleted transistors by identifying the square pulsation term in $(\omega Z_{\sigma\pi \mathrm{ij}})$ showed that, due to the layout design, L'_{se} is negligible with respect to L'_{de} and

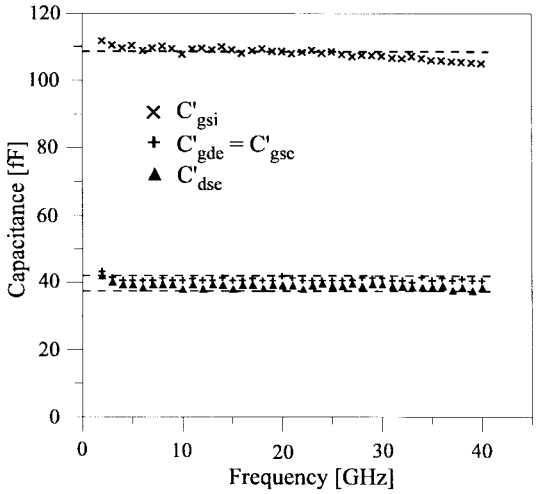

Fig. 6. Extracted capacitance values versus frequency for a nMOSFET with $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m at $V_{\rm gs} = 1$ V, and $V_{\rm ds} = 2$ V. The dotted lines are mean values over the 3–15 GHz band.

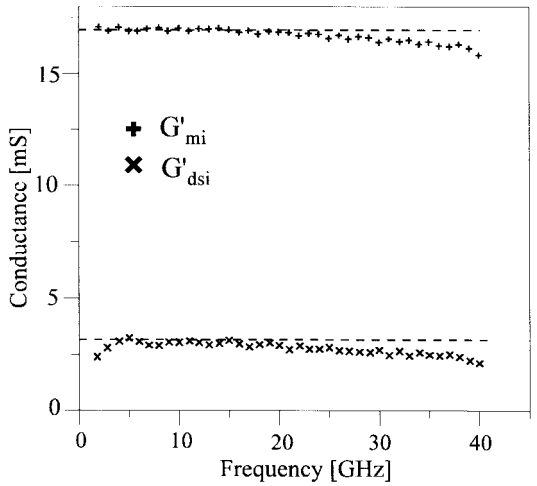

Fig. 7. Extracted conductance values versus frequency for a nMOSFET with $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 2$ V. The dotted lines are mean values over the 3–15 GHz band.

$L'_{\rm ge}$, being at least 30 times smaller. Accordingly, the third equation used for the evaluation of the inductances is simply $L'_{\rm se} = 0$. The main advantage of the method based on the parametric curves with respect to the optimization of [20], is that decreasing the device size does not compromise accuracy. Indeed, (8)–(13) are not influenced by the device size, as it cancels out in the ratios $A_{\rm ij}/A_{\rm kl}$, $E_{\rm ij}/E_{\rm kl}$, and $F_{\rm ij}/F_{\rm kl}$. The optimization criteria used by Lee are, on the contrary, based on (6) and (7), where the $A_{\rm ij}$, $E_{\rm ij}$, and $F_{\rm ij}$ terms tend to mask the influence of the series elements in the case of small devices. Other important features of the present method are that it takes advantage of the disymmetry $Z_{\sigma\pi}$ to enhance accuracy, and also that the shared frequency dependence of the $Z_{\sigma\pi{\rm ij}}$ is correctly and coherently accounted for during the extraction. This latter alleviates the need to discard data below a certain frequency during the extraction of $L'_{\rm ge}$ [20].

Using the extracted values of $R'_{\rm ge}$, $R'_{\rm de}$, $L'_{\rm ge}$, and $L'_{\rm de}$ and assuming $R'_{\rm se} = R'_{\rm de}$ and $L'_{\rm se} = 0$ the matrix $\boldsymbol{Z}_\sigma$ is reconstructed and subtracted from $\boldsymbol{Z}_{\sigma\pi}$ to deembed $\boldsymbol{Y}_\pi$. Inversion of the analytical expressions of the components of $\boldsymbol{Y}_\pi$ at all frequency points yields the curves of Figs. 6–8. Deviations of these curves from the horizontal are attributed at the low end of the band to the low-frequency limit of the TRL calibration, while at the high end, the deviation is attributed to the inappropriate (QS) modeling. $C'_{\rm gsi}$, $G'_{\rm mi}$, $G'_{\rm dsi}$, $C'_{\rm gse}$, $C'_{\rm gde}$, and $C'_{\rm dse}$ are obtained from the curves by taking the mean on the 3–15 GHz band and τ' by taking the mean on the 15–40 GHz band because below 15 GHz τ is very sensitive to the measurement errors on S-parameters. As indicated in Fig. 3, $C'_{\rm gse}$ is chosen equal to $C'_{\rm gde}$. The validity of this assumption has been verified by individual extraction of the capacitances in depletion, and is confirmed by the negligible slope of $C_{\mu g}$ versus W_f in Fig. 3. According to the considerations developed previously, $C'_{\rm gsi}$, $G'_{\rm mi}$, $G'_{\rm dsi}$, τ', $C'_{\rm gse}$, $C'_{\rm gde}$, and $C'_{\rm dse}$ are adopted as final values for the corresponding circuit elements.

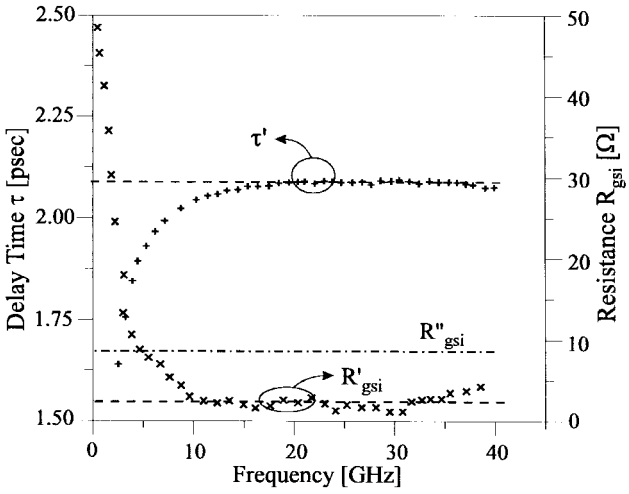

Fig. 8. Extracted values of the NQS parameters versus frequency for a nMOSFET with $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 2$ V. The dotted lines are mean values of τ' and $R'_{\rm gsi}$ over the 15–40 GHz band. The dash-dot line is the final value $R''_{\rm gsi}$.

C. Non-Quasi-Static Modeling

The important variations of the $R'_{\rm gsi}$ curve reveal that the proposed QS extraction scheme cannot be applied to the estimation of this NQS parameter. To solve this problem, an alternative approach based on the complete NQS expression of $\mathrm{Im}(Z_{\sigma\pi 12})$ is used. This expression involves $L_{\rm se}$, which is known to be negligibly small, and all intrinsic elements. $R''_{\rm gsi}$ is obtained by fitting the analytical expression of $\mathrm{Im}(Z_{\sigma\pi 12})$ to the measured data over the whole band, using only $R_{\rm gsi}$ as a optimization variable. Fig. 9 reveals the good agreement obtained between the measured curve and the simulation results based on $R''_{\rm gsi}$.

Substituting $R''_{\rm gsi}$, $C'_{\rm gsi}$, $G'_{\rm mi}$, $G'_{\rm dsi}$, τ', $C'_{\rm gse}$, $C'_{\rm gde}$, and $C'_{\rm dse}$ in the complete NQS expressions of $\mathrm{Re}(Z_{\sigma\pi{\rm ij}})$ and $\mathrm{Im}(Z_{\sigma\pi{\rm ij}})$, new values (denoted by $''$) are obtained for $R_{\rm ge}$, $R_{\rm de}$, $R_{\rm se}$, $L_{\rm ge}$, and $L_{\rm de}$, which are adopted as the final values of the extraction for these parameters.

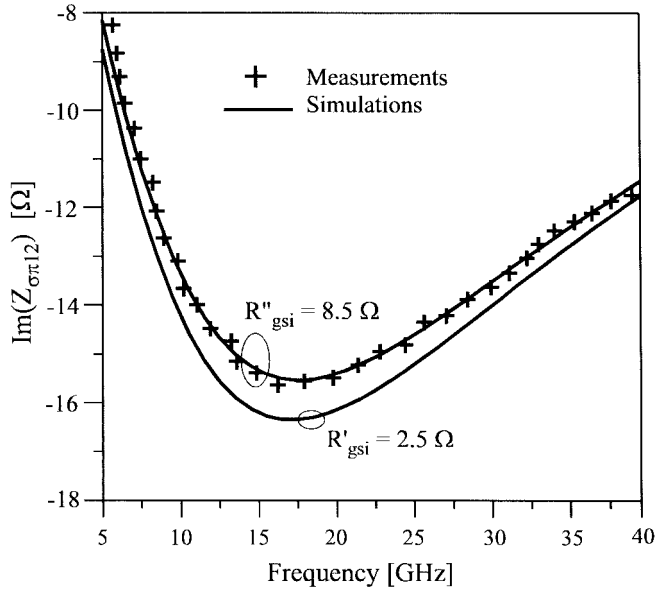

Fig. 9. Comparing the agreement between measurements and simulation for the initial ($'$) and final ($''$) values of parameter $R_{\rm gsi}$ for a nMOSFET with $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 2$ V.

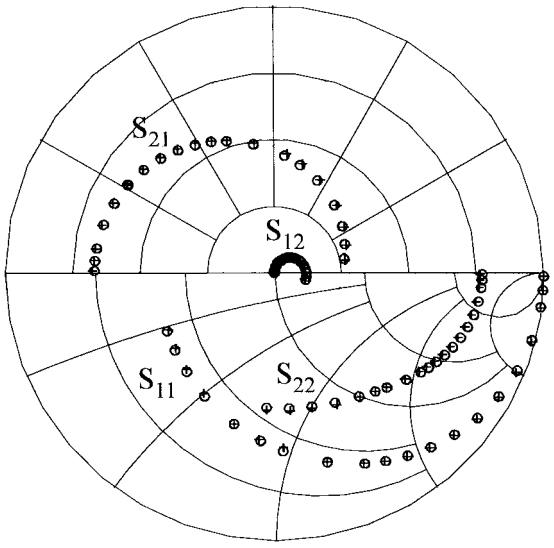

Fig. 10. Measured (O) and modeled (+) S-parameters from 0.5 to 40 GHz for a nMOSFET with $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m, at $V_{\rm gs} = 1$ V and $V_{\rm ds} = 2$ V. $L_{\rm ge} = 36$ pH, $L_{\rm de} = 44$ pH, $L_{\rm se} = 0$ pH, $R_{\rm ge} = 11.2\ \Omega$, $R_{\rm de} = 3.8\ \Omega$, $R_{\rm se} = 3.5\ \Omega$, $C_{\rm gsi} = 109$ fF, $C_{\rm gse} = C_{\rm gde} = 40.5$ fF, $C_{\rm dse} = 37$ fF, $G_{\rm mi} = 17$ mS, $G_{\rm dsi} = 2.9$ mS, $\tau = 2.07$ ps, $R_{\rm gsi} = 8.5\ \Omega$.

V. Results

The extraction procedure described in the previous section is used to monitor and analyze the device performance, in order to guide the process engineers in their effort to produce high-performance low-voltage low-power SOI MOSFET's. This new characterization scheme has been successfully applied to both enhancement-mode n-channel and accumulation-mode p-channel SOI MOSFET's of various sizes. Fig. 10 shows the good match which is typically obtained between the measured S-parameter curves and the simulations based on the extracted parameters, up to 40 GHz. The ability of the method to identify correctly $R_{\rm gsi}$ and τ has been tested by performing extractions on a single device at different bias points. The results are summarized in Table I. Despite important variations of $R_{\rm gsi}$ versus bias, the series extrinsic resistances remain constant, as anticipated from technological considerations. Table II illustrates the correlation between various silicidation technologies, the extracted series resistances and global device performances [21]. Fig. 11 reveals state-of-the-art low-voltage performance for 0.5-μm n-channel SOI MOSFET's fabricated using conventional CMOS technology combined with nickel-silicidation of gate, source and drain. A current-gain transition frequency of 14 GHz and a maximum oscillation gain frequency of 30 GHz at 1 V supply voltage render these devices suitable for low-power telecommunications applications.

TABLE I
Final Extracted Values in Different Biasing Conditions for a nMOSFET with $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m

	NQS elements		Final values of the extraction				
Applied Voltages	τ' [ps]	R''_{gsi} [Ω]	R''_{ge} [Ω]	R''_{de} [Ω]	R''_{se} [Ω]	L''_{ge} [pH]	L''_{de} [pH]
$V_{ds} = 2$ V, $V_{gs} = 1$ V	1.95	8.5	11.2	3.8	3.5	36.1	44
$V_{ds} = 1$ V, $V_{gs} = 1$ V	2.07	10.8	11.24	3.78	3.46	36.4	44.2
$V_{ds} = 1.5$ V, $V_{gs} = 0.5$ V	2.16	15.6	11.28	3.68	3.57	36	44.7

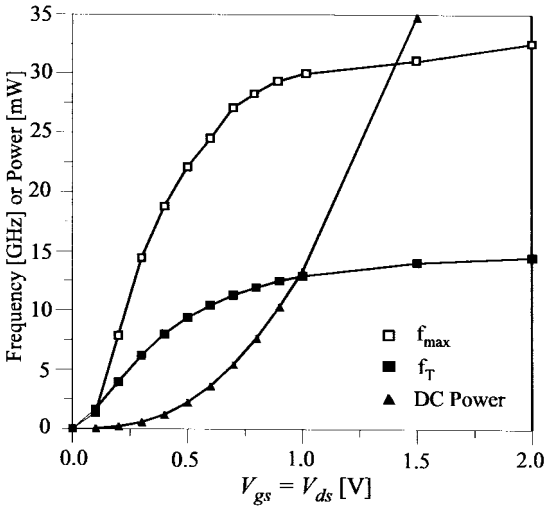

Fig. 11. Current-gain transition frequency (f_T), maximum oscillation frequency ($f_{\rm max}$), and dc power consumption as a function of supply voltage ($V_{\rm ds} = V_{\rm gs}$) for a nMOSFET with Ni silicidation, $W = 240\,\mu$m and $L_{\rm eff} = 0.5\,\mu$m.

VI. Conclusion

An accurate characterization procedure for SOI MOSFET's has been demonstrated. Combining careful design of probing and calibration structures, rigorous *in situ* calibration, and a new powerful direct extraction method, reliable identification of the parameters of the NQS small-signal model has been achieved. All intrinsic and extrinsic parameters, the shunt input and output feed admittances excepted, are extracted from S-parameters measurements at a single bias point in saturation. The extracted model fits the measured data well over the whole 40 GHz measurement band. This new characterization scheme

TABLE II
EXTRACTED VALUES OF SERIES PARASITIC RESISTANCES, UNITY-CURRENT GAIN FREQUENCY (f_T), AND MAXIMUM OSCILLATION GAIN FREQUENCY ($f_{\max}$) AT $V_{\rm gs} = V_{\rm ds} = 1$ V FOR n- AND p-SOI MOSFET'S WITH $W = 240\,\mu$m AND $L_{\rm eff} = 0.5\,\mu$m, USING VARIOUS SILICIDE PROCESSES

	$TiSi_2$ (6.2 Ω/sq.)					$CoSi_2$ (4.4 Ω/sq.)					NiSi (2.8 Ω/sq.)				
	R_{ge}	R_{de}	R_{se}	f_T	f_{max}	R_{ge}	R_{de}	R_{se}	f_T	f_{max}	R_{ge}	R_{de}	R_{se}	f_T	f_{max}
nMOSFET	11.2	3.8	3.5	12	14.3	8.1	2.1	1.5	14	19.3	4.1	1	1.2	14	30
pMOSFET						8.4	2.5	2.4	5.7	9.2	3.4	1.8	1.3	8.6	14.7

has proven to be an efficient tool for analog modeling and for the optimization of device performances.

APPENDIX

As explained in Section IV, analytical QS expressions for the elements of $Z_{\sigma\pi}$ are obtained by substituting the definition of the matrices Z_σ (3) and Y_π (4) in (1) and setting $R_{\rm gsi} = \tau = 0$.

$$Z_{\sigma\pi 11} = R_{\rm ge} + R_{\rm se} + j\omega(L_{\rm ge} + L_{\rm se}) + \frac{G_{\rm dsi} + j\omega(C_{\rm gde} + C_{\rm dse})}{D} \tag{A1}$$

$$Z_{\sigma\pi 12} = R_{\rm se} + j\omega L_{\rm se} + \frac{j\omega C_{\rm gde}}{D} \tag{A2}$$

$$Z_{\sigma\pi 21} = R_{\rm se} + j\omega L_{\rm se} - \frac{G_{\rm mi} - j\omega C_{\rm gde}}{D} \tag{A3}$$

$$Z_{\sigma\pi 22} = R_{\rm de} + R_{\rm se} + j\omega(L_{\rm de} + L_{\rm se}) + \frac{j\omega(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})}{D} \tag{A4}$$

where $D = Y_{\pi 11}Y_{\pi 22} - Y_{\pi 12}Y_{\pi 21}$

$$D = -\omega^2[(C_{\rm gsi} + C_{\rm gse})(C_{\rm dse} + C_{\rm gde}) + C_{\rm gde}C_{\rm dse}] + j\omega[G_{\rm mi}C_{\rm gde} + G_{\rm dsi}(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})]$$

Next, splitting (A1)–(A4) in their real and imaginary part, one obtains eight equations which can be summarized as follows:

$$\mathrm{Re}(Z_{\sigma\pi{\rm ij}}) = \mathrm{Re}(Z_{\sigma{\rm ij}}) + \frac{A_{\rm ij}}{\omega^2 + B} \quad \text{for } i, j \in \{1, 2\} \tag{A5}$$

$$\frac{1}{\omega}\cdot\mathrm{Im}(Z_{\sigma\pi{\rm ij}}) = \frac{1}{\omega}\mathrm{Im}(Z_{\sigma{\rm ij}}) - \frac{E_{\rm ij}}{\omega^2 + B} - \frac{F_{\rm ij}}{\omega^2\cdot(\omega^2 + B)} \quad \text{for } i, j \in \{1, 2\}. \tag{A6}$$

As can be seen in (A7)–(A19), shown at the bottom of the page, the coefficients B, $A_{\rm ij}$, $E_{\rm ij}$, and $F_{\rm ij}$ are independent of frequency. As stated in Section IV-B, the extraction of the series resistors works best when the device is saturated. This easily explained, considering that three parametric curves are

$$B = \frac{[G_{\rm mi}C_{\rm gde} + G_{\rm dsi}(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})]^2}{Den^2} \tag{A7}$$

$$A_{11} = \frac{C_{\rm gde}[G_{\rm mi}C_{\rm dse} + C_{\rm gde}(G_{\rm mi} + G_{\rm dsi})]}{Den^2} \tag{A8}$$

$$A_{12} = \frac{C_{\rm gde}[G_{\rm mi}C_{\rm gde} + G_{\rm dsi}(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})]}{Den^2} \tag{A9}$$

$$A_{21} = \frac{G_{\rm mi}[(C_{\rm gsi} + C_{\rm gse})(C_{\rm dse} + C_{\rm gde}) + C_{\rm gde}C_{\rm dse}] + C_{\rm gde}[G_{\rm mi}C_{\rm gde} + G_{\rm dsi}(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})]}{Den^2} \tag{A10}$$

$$A_{22} = \frac{(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})[G_{\rm mi}C_{\rm gde} + G_{\rm dsi}(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})]}{Den^2} \tag{A11}$$

$$E_{11} = \frac{C_{\rm dse} + C_{\rm gde}}{Den} \tag{A12}$$

$$E_{12} = E_{21} = \frac{C_{\rm gde}}{Den} \tag{A13}$$

$$E_{22} = \frac{C_{\rm gsi} + C_{\rm gse} + C_{\rm gde}}{Den} \tag{A14}$$

$$F_{11} = \frac{G_{\rm dsi}[G_{\rm mi}C_{\rm gde} + G_{\rm dsi}(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})]}{Den^2} \tag{A15}$$

$$F_{12} = 0 \tag{A16}$$

$$F_{21} = \frac{-G_{\rm mi}[G_{\rm mi}C_{\rm gde} + G_{\rm dsi}(C_{\rm gsi} + C_{\rm gse} + C_{\rm gde})]}{Den^2} \tag{A17}$$

$$F_{22} = 0 \tag{A18}$$

with

$$Den = (C_{\rm gsi} + C_{\rm gse})(C_{\rm gde} + C_{\rm dse}) + C_{\rm gde}C_{\rm dse} \tag{A19}$$

needed to provide three independent equations involving the resistors. This number of equations cannot be obtained unless $Z_{\sigma\pi 12}$ and $Z_{\sigma\pi 21}$ are substantially different from each other, which is only the case when G_{mi} is nonzero. The ability of the new extraction method to determine all series resistances from S-parameters measurements at a single bias-point, constitutes a significant improvement over previously published methods [5], [6], [22], [23], which concentrate on measurements at $V_{\mathrm{ds}} = 0$ V, when G_{mi} is zero.

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