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Application-Specific Design of Ultra-Low-Power Low-Noise Vagus Nerve Front-End Circuits for the Detection of Epileptic Seizures

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Abstract

EPILEPSY is a neurological condition affecting about 70 million patients worldwide, one third of which do not respond to medication. Closed-loop vagus nerve stimulation (VNS) is a promising alternative treatment for patients suffering from drug-resistant epilepsy, improving their quality of life thanks to a reduction in seizure frequency and severity. This neuromodulation therapy has the potential to be more efficacious than its open-loop counterpart by delivering stimulation at the seizure onset. It however requires accurate seizure detection capabilities. For that task, several biomarkers can be used, but detecting seizures from the vagus nerve electroneurogram (VENG) offers a minimally invasive potential solution. The targeted closed-loop VNS system based on the VENG is powered by a battery and implanted in the patient's chest. Hence, it should work with a power budget around 50 µW for both sensing and stimulation to ensure a 10-year lifetime, 10-15 µW of which can be allocated to the analog front-end (AFE) circuits used for sensing. Due to the low µV-range amplitude of the VENG signals captured by an extraneural electrode, the acquisition of the signals is sensitive to noise and interference. In general, the most stringent AFE specifications are (i) an ultra-low power budget, (ii) a low intrinsic noise in the acquisition circuits, and (iii) the need for the rejection of electromyogram (EMG) interference from nearby muscles activity. The acquisition of VENG signals is scarcely addressed in the literature and no published AFE design meets the specifications of that application.

In this thesis, we propose methodologies and circuit techniques for the design of an integrated VENG-specific AFE tackling the aforementioned challenges. This work spans across several abstraction layers: (i) studying the noise-power trade-off of the low-noise amplifier (LNA) from de-

vice level to circuit level, (ii) designing and modeling a complete ultra-low-power (ULP) AFE, and (iii) linking circuit-level performance and non-idealities to seizure detection accuracy. The approach chosen in this thesis consists in relying on system and application knowledge to design and validate highly efficient circuits specific to VENG sensing. System knowledge includes the characteristics of the input signals and of the nerve interfacing electrode, and details about the seizure detection algorithms.

The first chapter of this thesis investigates the context of this work, from biomedical application to circuit design. The choice of the VENG sensing application is motivated by medical needs and ethical concerns over other treatment solutions. Next, our knowledge about the closed-loop VNS system is linked to analog circuit specifications (e.g., noise and power consumption). State-of-the-art circuits are presented to meet those constraints in a VENG-specific AFE. Finally, seizure detection algorithms are presented to offer insights on the signal processing tasks performed after signal acquisition.

The second chapter of this thesis dives into the study of the LNA, which is the bottleneck of the system in terms of noise and power consumption. Hence, the fundamental limits of the noise-power trade-off in biomedical amplifiers are analyzed with a semi-analytical approach using the g_m/I_D methodology and a limited number of technology-dependent parameters. We show that the minimum achievable noise efficiency factor (NEF) with a fixed topology can be accurately estimated analytically, allowing designers to compare LNA topologies without requiring time-consuming numerical optimizations. The novel methodology is then applied to the design and optimization of an LNA with an innovative topology combining current reuse for noise efficiency, and common-gate input for resistorless high-pass filtering of interference. The proposed LNA is prototyped on a 22-nm fully-depleted silicon-on-insulator chip and reaches an NEF of 1.97, representing a 2× NEF improvement compared to the only existing VENG-specific LNA in the state of the art.

In the third chapter of this work, the previously designed LNA is integrated into a complete low-power AFE dedicated to the acquisition of VENG signals. It is first demonstrated that rejecting in-band EMG requires a true tripole input with electrode imbalance compensation and low gain mismatch. While imbalance compensation was tackled in previous works, gain mismatch still has to be addressed. To do so, we propose an inter-channel chopping technique that performs dynamic element matching and modulates the residual interference to high frequency while keeping the

VENG signal in its original band, achieving a measured gain mismatch level of 0.35%. The analog circuits are interfaced with ULP circuits including filters and an analog-to-digital converter to form a complete front-end. The proposed circuits are prototyped in a 65-nm CMOS technology and consume an average power of 13.3 µW, which is at the limit of the AFE's power budget. We show that the proposed front-end circuits enable the accurate capture of action potential waveforms with an amplitude down to 20 μV_{PP}, which is the expected amplitude of VENG signals.

The last chapter of this thesis bridges the gap between the circuit-level specifications of the front-end and the performance of the seizure detection algorithm. Bio-interface circuit specifications are often based on preconceptions of applicative requirements, and an arbitrary signal-to-noise ratio. However, the exact needs of the applicative context are unknown, leading to non-functional or inefficient designs due to too stringent specifications. This chapter uses experimental VENG data obtained on rats, a behavioral model of the front-end, and a seizure detection algorithm to study the sensitivity of detection accuracy to AFE limitations. The sensitivity analysis results are then leveraged to extract optimal specifications for the front-end while minimizing its power consumption. We show that it is possible to reduce the front-end power consumption down to 2.1 µW by relaxing its specifications while maintaining excellent seizure detection accuracy, paving the way for more efficient VENG-specific front-end designs and closed-loop VNS implants with a longer lifetime.

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List of publications

Related journal papers

[JP1] S. Favresse, D. Bol and D. Flandre, "A Combined Analytical and Simulation-Based Methodology for Quantifying the Noise-Power-Area Trade-Offs in Biomedical Amplifiers," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 71, no. 12, pp. 6177-6189, Dec. 2024.
DOI: 10.1109/TCSI.2024.3414649.

[JP2] S. Favresse, A. Nonclercq, R. El Tahry, D. Bol and D. Flandre, "Analysis of the Impact of Hardware Front-End Limitations on Vagus Nerve Electroneurogram-Based Seizure Detection," *submitted for publication*.

[JP3] S. Favresse, P. Maistriaux, D. Flandre and D. Bol, "An Ultra-Low-Power Instrumentation Amplifier with Low Gain Mismatch for Tripolar ENG Recording," *submitted for publication*.

Related conference papers

[CP1] S. Favresse, D. Bol and D. Flandre, "A 1.88-NEF 3-kHz Current-Reuse Common-Gate Amplifier Featuring Resistorless High-Pass Filtering," *31st IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, 2024, pp. 1-4.
DOI: 10.1109/ICECS61496.2024.10848910.

[CP2] S. Favresse, P. Maistriaux, P. Harpe, D. Flandre and D. Bol, "An Ultra-Low-Power Dual-Channel Analog Front End for Vagus

Nerve Sensing with Chopping-Minimized Gain Mismatch," *21st IEEE Biomedical Circuits and Systems Conference (BioCAS)*, 2025, pp. 121-125.
DOI: 10.1109/BioCAS67066.2025.00036.

Unrelated conference papers

[UCP1] N. Verbeek, S. Favresse, F. Baudart and B. Dehez, "Estimation of Equivalent Thermal Conductivity of PCB Airgap Windings," *IEEE International Conference on Electrical Machines (ICEM)*, 2022, pp. 1362-1368.
DOI: 10.1109/ICEM51905.2022.9910744.

List of acronyms

A-BPF	Analog Band-Pass Filters
AAF	Anti-Aliasing Filter
ADC	Analog-to-Digital Converter
AED	Antiepileptic Drug
AFE	Analog Front-End
AHB	Advanced High-Performance Bus
ANN	Artificial Neural Network
AP	Action Potential
AUC	Area Under the ROC Curve
BCI	Brain-Computer Interface
BG	Background
BPF	Band-Pass Filter
CG	Common Gate
CM	Common Mode
CMFB	Common-Mode Feedback
CMOS	Complementary Metal-Oxide-Semiconductor
CMRR	Common-Mode Rejection Ratio
CPU	Central Processing Unit
CR	Current Reuse
D-BPF	Digital Band-Pass Filters
DAC	Digital-to-Analog Converter
DBE	Digital Back-End
DBS	Deep Brain Stimulation
DEM	Dynamic Element Matching
DFE	Digital Front-End
DMA	Direct Memory Access
DMEM	Data Memory
DSL	DC Servo Loop

(Continued)

ECG	Electrocardiogram
EDO	Electrode DC Offset
EEG	Electroencephalogram
EMG	Electromyogram
ENBW	Equivalent Noise Bandwidth
ENG	Electroneurogram
ESD	Electrostatic Discharge
FD-SOI	Fully-Depleted Silicon-On-Insulator
FDSA	Fully differential Summing Amplifier
FG	Foreground
FoM	Figure of Merit
GBW	Gain-Bandwidth Product
HPF	High-Pass Filter
HR	Heart Rate
HVT	High Voltage Threshold
HW	Hardware
IA	Instrumentation Amplifier
IC	Integrated Circuit
iEEG	Intracranial Electroencephalogram
IIR	Infinite Impulse Response
IoT	Internet of Things
IPG	Implantable Pulse Generator
IRN	Input-Referred Noise
IRR	Interference Rejection Ratio
k-NN	K-Nearest Neighbor
LFP	Local Field Potential
LNA	Low-Noise Amplifier
LOO	Leave-One-Out
LP	Low-Power
LPF	Low-Pass Filter
LSB	Least Significant Bit
LUT	Look-Up Table
LVT	Low Voltage Threshold
MCU	Microcontroller Unit
ML	Machine Learning
MOM	Metal-Oxide-Metal
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MSB	Most Significant Bit
NCC	Normalized Cross-Correlation
NEF	Noise Efficiency Factor
OSR	Oversampling Rate

(Continued)

OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PEF	Power Efficiency Factor
PNS	Peripheral Nervous System
PSD	Power Spectral Density
PSRR	Power Supply Rejection Ratio
PTZ	Pentylenetetrazol
PVT	Process, Voltage and Temperature
QT	Quasi Tripole
RNS	Responsive Neurostimulation
ROC	Receiver Operating Characteristic
SAR	Successive Approximation Register
SLVT	Super-Low Voltage Threshold
SNDR	Signal-to-Noise-and-Distortion Ratio
SNR	Signal-to-Noise Ratio
SoC	System-on-Chip
SUDEP	Sudden Unexpected Death in Epilepsy
SVM	Support Vector Machine
SW	Software
THD	Total Harmonic Distortion
TT	True Tripole
ULP	Ultra Low Power
VENG	Vagus Nerve Electroneurogram
VNS	Vagus Nerve Stimulation

Introduction

BIOPOTENTIAL acquisition technologies represent a fast-growing field driven by demand in various applications such as medical diagnostic, health monitoring, closed-loop neuromodulation, and neuroscience research [1]. Biopotential measurements are used to characterize the electrical activity of several organs or body parts, namely the electrocardiogram (ECG) for the heart, the electroencephalogram (EEG) for the brain, the electromyogram (EMG) for muscles, and the electroneurogram (ENG) for neurons of the peripheral nervous system (PNS). The acquisition technologies are integrated into electronic systems that can be of different natures, from fixed hospital devices to wearables and implants. Depending on the nature and target application of the system, its design specifications differ. For example, high-resolution equipment is preferred for hospital monitoring, whereas ultra-low-power (ULP) operation is required for implantable devices due to tight energy constraints.

In multiple sectors nowadays, there is a growing demand for connected devices for the Internet of things (IoT). The field of healthcare is no exception to that trend, and sees the development of small and low-power wearable or implantable devices for continuous real-time monitoring of physiological parameters. Those systems require advanced front-end circuits for the amplification, filtering, and digitization of biopotential signals with high performance on different metrics. For battery-powered devices, the analog circuits must typically work with a sub-mW power consumption to ensure device longevity. Additionally, most biopotential signals are sensed with an amplitude below 1 mV, making their acquisition sensitive to parasitic signals such as physiological interference and noise from the acquisition circuits [2]. Furthermore, the analog front-end (AFE) must be interfaced with an electrode that converts ionic currents into detectable

electronic voltages. This bio-interface entails complications such as DC offset and series impedance. Finally, the acquisition of biopotential signals also often requires small silicon area and good matching in the case of multiple recording channels.

Generic biopotential AFEs can reach high performance in terms of noise-power trade-off [3] or inter-channel matching [4]. However, each type of signal and application have their own specific constraints. For instance, ECG and EEG sensing systems with dry electrodes require a MΩ-level AFE input impedance [5]. In a separate case, the action potentials (APs) that constitute the ENG signal typically have an ultra-low amplitude in the 10-µV range and therefore require a high gain and an ultra-low noise level [6]. Finally, the ECG is located at low frequencies (< 100 Hz) and necessitates flicker noise mitigation techniques [7]. Generic architectures can thus be non-functional or be sub-optimal when integrated for a specific context. Application-specific architectures can be designed with a good knowledge of the exact use, thus only integrating techniques and specificities required in that application. This ensures a functional and optimal operation at the system level given a known applicative context and avoids over-constraining the designs. Specific front-end architectures are widespread for the monitoring of ECG [8–12], EEG [13–15], or intracranial EEG [16–20], but the literature on ENG-specific front-ends is scarcer.

In this thesis, we focus on the design of an ENG-specific AFE driven by a genuine need in a biomedical application, and leverage the knowledge of the intended use environment to optimize the AFE performance and ensure its functionality.

⋆ Target Application: Vagus Nerve Activity Recording

Epilepsy is a neurological condition affecting about 70 million patients worldwide, causing recurrent seizures. Patients are primarily treated with medication, although about one third of them have a drug-resistant form of the disease and need another form of treatment. Vagus nerve stimulation (VNS) is a palliative therapy often suggested in that case. It consists in regularly stimulating the left vagus nerve with electrical pulses via an implant, thereby reducing the severity and frequency of seizures. VNS shows a moderate efficacy that could be improved by operating in closed loop, i.e., delivering a strong stimulation at the start of a seizure. For that pur-

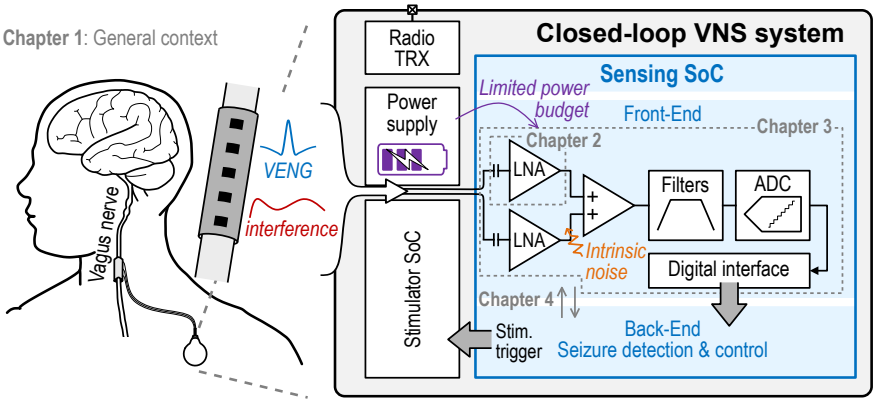


Fig. 1 Block diagram of an implantable closed-loop VNS system with architectural details on the sensing SoC. The technical challenges linked to the front-end design are highlighted. The chapters of this thesis that address the design or analysis of different parts of the system are also indicated.

pose, sensing capabilities must be included in the system to detect seizure onsets. While seizure detection can be achieved through several biomarkers, it has recently been proven that seizures could be detected from spontaneous vagus nerve activity, paving the way for a minimally-invasive closed-loop VNS modality using the same electrode for both sensing and stimulation [21–23].

Fig. 1 presents a potential closed-loop VNS system based on vagus nerve electroneurogram (VENG) recording. As illustrated, the system is composed of a cuff electrode and a single implant with multiple systems-on-chip (SoCs), radio modules, and a power supply. The sensing SoC includes a front-end which serves the purpose of VENG signal acquisition, and a back-end for signal processing, seizure detection and system control. The front-end is composed of amplifiers, filters, an analog-to-digital converter (ADC), and a digital interface. Its design is the focus of this thesis and faces several technical challenges.

As introduced above, the total power budget is limited. Given that the system is implanted, replacing the battery necessitates a surgical intervention, which should be avoided. For a 10-year lifetime, first-order estimations give a power budget of 50 µW for the entire system and a maximum around 10 to 15 µW for the front-end under certain assumptions detailed in Chapter 1. ULP circuit design techniques are thus required to reach good performance in this system. In addition, the amplitude of the detectable

VENG signals is typically around 20-μV_{PP} [23]. To achieve a good signal-to-noise ratio (SNR), the intrinsic noise from the acquisition circuits should thus be maintained low, using a low-noise amplifier (LNA) at the input of the AFE. However, reducing LNA noise comes at the price of increased power consumption. The noise-power trade-off is thus a bottleneck in VENG-sensing AFEs. Moreover, ENG acquisition is corrupted by EMG interference from nearby muscles, with an amplitude up to 100-1000$\times$ that of the useful ENG signal [24]. Circuit-level and AFE-level techniques exist to reject the in-band and out-of-band interference at the price of additional power consumption and design complexity.

⋆ Research Question

The performance of state-of-the-art biopotential recording architectures is presented in Fig. 2. The LNA performance is characterized via the current consumption - input-referred noise (IRN) trade-off in Fig. 2(a). The target performance of the LNA for the VENG system is shown. It can be seen that while LNA designs respecting those specifications exist, none is designed for ENG sensing. Those thus lack ENG specificities such as rejection of EMG interference and very low input amplitude. Similarly, Fig. 2(b) shows the performance of biopotential sensing AFEs on a power - power efficiency factor (PEF) curve. The PEF, defined in Chapter 1, quantifies the noise and power performance of a front-end. A lower PEF indicates a better performance. As illustrated, a previous VENG-specific AFE was designed at UCLouvain (Dekimpe and Bol, [25]), but its power consumption of 104 µW is too high compared to the specification of 10-15 µW.

In this thesis, circuit techniques and design methodologies are leveraged for implementation in a VENG-specific architecture. A detailed knowledge of the applicative context is used to define accurate requirements and specifications in terms of power consumption, noise, and interference rejection. The main research question raised in this thesis is summarized as:

"How can circuit design techniques
and a solid knowledge of the application
be leveraged for the design and validation
of an ultra-low-power, low-noise, EMG-robust,
VENG-specific analog front-end?"

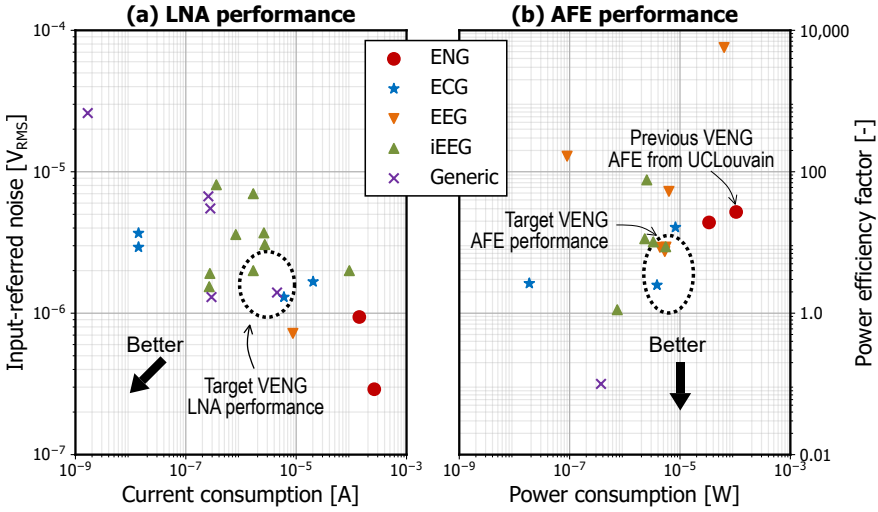


Fig. 2 State-of-the-art of low-power biopotential recording architectures. (a) Current consumption - IRN curves for the LNA, (b) power consumption - PEF curves for the entire AFE. No published design fits all specifications (power, noise, EMG rejection, bandwidth) for VENG sensing.

In this thesis, intermediate research questions are raised in each chapter to form a sub-division of the challenges addressed in this work.

⋆ Thesis Outline

Fig. 3 indicates the topic of each chapter on an abstraction scale. This thesis starts by exploring the applicative context and state-of-the-art circuit design techniques to define targets and specifications for the VENG-specific AFE in a top-down approach. The next chapters then work bottom-up to address the application-specific technical challenges. Noise in the LNA is first studied by linking device-level noise models with the circuit-level performance of various biomedical LNA topologies. Next, ULP circuits are designed, from the LNA to a complete AFE with different interference rejection techniques. Finally, system-level research is performed in the last chapter to verify and optimize the AFE performance as a function of its impact on the signal and on the accuracy of seizure detection algorithms. The different chapters are detailed next.

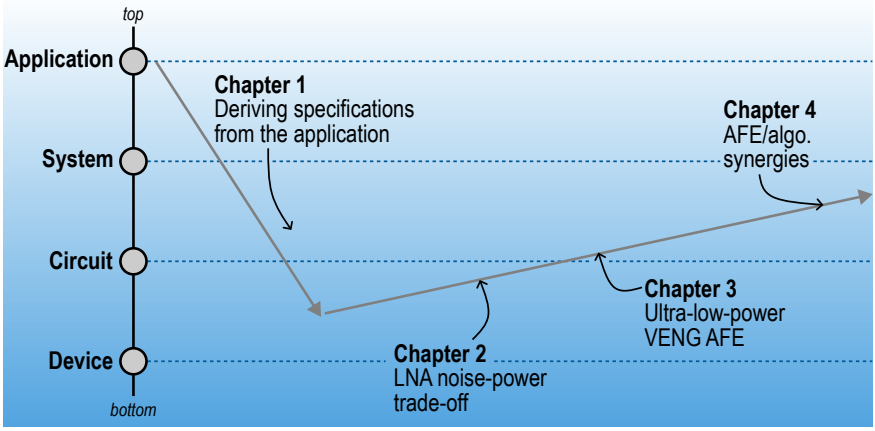


Fig. 3 Location of each thesis chapter on a scale of abstraction layers.

Chapter 1 analyzes the context and the state-of-the-art, providing background knowledge related to the topic of this thesis. The biomedical context is first described. Closed-loop VNS is identified as a promising treatment for epilepsy based on therapeutic efficacy and ethical matters. The choice of VENG as a biomarker for seizure detection is based on the low invasiveness and potential good accuracy of that modality. Technical specificities of VENG signals acquisition are presented, such as the nature and amplitude of the signal, the required bandwidth and the presence of interference. Power budgets of 50 µW for the entire system and 10-15 µW for the front-end are derived from existing power supply technologies. In the second part of this chapter, state-of-the-art analog design techniques for biomedical AFEs are presented, addressing the technical challenges linked to VENG specificities. Presented techniques tackle the interfacing between the electrode and the acquisition circuits, the rejection of out-of-band and in-band interference, low-noise amplifications in LNAs, and low-power operation in ADCs. Finally, the last part of this chapter explores biosignal processing and seizure detection techniques. EEG-based algorithms are first introduced, showing a wide variety of approaches. Then, a few experiments focused on VENG-based seizure detection with rat subjects are presented, demonstrating good classification results with limited generalization. A VENG-based automated seizure detection algorithm is introduced to serve as basis for signal processing and seizure detection addressed in Chapter 4.

Chapter 2 explores the noise-power trade-off at the level of the LNA. It is based on our TCAS-I publication [JP1] and on our ICECS conference paper [CP1]. The first part of this chapter introduces a semi-analytical methodology aiming to easily estimate the optimal performance of an LNA in terms of noise, power consumption, and silicon area. The proposed methodology uses bias- and technology-dependent noise models at the device level based on the transistor's (g_m/I_D) design parameter. Then, those models are integrated into LNA-level analytical optimizations that yield the optimal noise-power-area performance achievable by a certain topology. The developments in this chapter are specific to VENG acquisition by considering the VENG bandwidth and the rejection of out-of-band interference with a high-pass filter at the LNA input, although the proposed methodology can be generalized to any low-noise application. A current reuse LNA topology is considered as case study, and the results of the semi-analytical optimizations are compared to numerical optimization outputs. This comparison shows that the proposed methodology estimates the thermal noise performance with negligible error, whereas a 20% difference in flicker noise level exists between the analytical estimation and the numerical results. In the second part of this chapter, the aforementioned methodology is leveraged to propose and optimize a novel VENG-specific amplifier topology combining low-noise performance and input high-pass filtering. Using a common-gate (CG) input, it eliminates the need for noisy passive resistors or other filtering techniques. The proposed LNA design is introduced and its performance is estimated analytically. The CG LNA is prototyped on a 22-nm fully-depleted silicon-on-insulator (FD-SOI) complementary metal-oxide-semiconductor (CMOS) chip and measurement results indicate a power consumption of 4.29 µW for an IRN of 1.72 μV_{RMS}, resulting in an noise efficiency factor of 1.97 with filtering of out-of-band interference below 300 Hz.

Chapter 3 presents the design of a ULP EMG-robust VENG-specific AFE, based on our BioCAS conference paper [CP2] and on a journal publication in writing process [JP3]. First, the rejection of in-band EMG interference is addressed through behavioral simulations considering a true tripole amplifier configuration, imbalance in the cuff electrode, and gain mismatch in the instrumentation setup. Cuff imbalance and gain mismatch are both identified as bottlenecks for EMG rejection. Since cuff imbalance compensation is already addressed in previous works, this chapter is focused on minimizing the gain mismatch. An inter-channel chopping

scheme is introduced and detailed mathematically, modulating the EMG to high frequencies while preserving the VENG signal. Second, the architecture of the ULP AFE is presented from block diagram to transistor-level implementations. The LNA from Chapter 2 is integrated into the proposed AFE which also features the proposed inter-channel chopping scheme, analog filters, a ULP successive-approximation register ADC, and digital decimation. The AFE is prototyped on a 65-nm CMOS chip, and measurement results indicate a 11.8-µW power consumption for the analog parts with an IRN of 1.80 μV_{RMS}, resulting in a PEF of 5.9. Using chopping and digital calibration, the gain mismatch is measured at 0.35%, which offers a 55-dB rejection of interference and brings the mV-range EMG down to the intrinsic noise level. The prototype chip is also evaluated for seizure detection by applying AP waveforms as inputs. The acquisition preserves the signal integrity for AP amplitudes above 20 μV_{PP}, validating the use of the proposed front-end in the target applicative context.

Chapter 4 explores a higher abstraction level by bridging the gap between the performance of a seizure detection algorithm and the circuit-level specifications of the VENG-specific front-end. This chapter is based on our journal paper [JP2] and characterizes the impact of front-end specifications on system performance by analyzing the sensitivity of seizure detection performance to front-end non-idealities and design choices. An optimization of the front-end specifications is then proposed, so as to decrease front-end power consumption while improving seizure detection accuracy. This chapter is based on experimental VENG data obtained on 8 rats, a behavioral model of the front-end, and a seizure detection algorithm modified to enable real-time processing. The front-end design choices and non-idealities studied in this chapter are: intrinsic noise, common-mode rejection, dynamic range, quantization resolution, and oversampling rate. The reported performance of the seizure detection algorithms is based on the SzCORE framework for the evaluation of seizure detection algorithms. It is shown in this chapter that noise and dynamic range are the main factors limiting seizure detection accuracy. An optimization of front-end specifications demonstrates a tolerance to noise up to 3 μV_{RMS} with a mere 6-bit ADC resolution, resulting in a 2.1-µW power consumption and a perfect seizure classification on the VENG dataset.

Finally, the **Conclusion** of this thesis provides a summary of the research presented in this work, highlighting answers to the various research

questions introduced throughout the thesis. Ultimately, we share some perspectives for further research in the continuation of this work in the fields of biomedical and microelectronics engineering.

1

Vagus Nerve Sensing: Background Foundations from Biomedical Context to Analog Circuit Design

The goal of this chapter is to provide an overview of the basic concepts and state of the art related to this thesis, from the biomedical context to analog circuit design and signal processing algorithms. Four different objectives are targeted in this chapter: (i) motivating the choice of vagus nerve electroneurogram (VENG) recording as target application, (ii) developing solid knowledge about application-specific constraints, (iii) identifying the key circuit-level challenges for the acquisition of VENG signals, and (iv) presenting state-of-the-art circuit techniques used in biopotential recording circuits.

We first introduce the biomedical context in Section 1.1 to motivate the choice of VENG recording as target application. The different treatment options in epilepsy are presented and several neuromodulation techniques are compared, including closed-loop vagus nerve stimulation (VNS). Some ethical concerns linked to brain-computer interfaces (BCIs) are also addressed, motivating research on alternative seizure detection and sensing

modalities such as the VENG. After defining the target application, we identify technical challenges specific to VENG recording, such as a power budget, the signal amplitude and bandwidth, and the presence of interference.

In Section 1.2, analog front-end (AFE) architectures for biopotential acquisition are reviewed. The specifications and circuit-level bottlenecks are first introduced based on the challenges of VENG recording identified previously. Afterwards, several techniques are presented to improve the noise and power performance of low-noise amplifiers (LNAs) and analog-to-digital converters (ADCs). The integration of a VENG-specific AFE in a closed-loop VNS system is also discussed.

Finally, Section 1.3 presents seizure detection algorithms by first introducing major electroencephalogram (EEG)-based approaches, then acute VENG experiments and VENG-based seizure detection algorithms. Understanding the signal processing performed downstream the acquisition circuit helps validating the AFE in a specific application context.

1.1 Biomedical Context: VNS as Treatment for Epilepsy

1.1.1 Epilepsy

Epilepsy is a common neurological disorder characterized by a predisposition to generate seizures. It is estimated that epilepsy affects 70 million patients worldwide with an average of 50 new cases detected each year out of 100,000 people [26]. Seizures are linked to abnormal neural activity leading to different possible symptoms, from loss of awareness to stiffening and jerking [27]. Epilepsy can be defined by different observed conditions, among which the occurrence of unprovoked seizures at least 24 h apart [28]. Epileptic patients suffer from a wide range of consequences linked to their condition, including behavioral and cognitive changes, social stigma [29] and, in some cases, death [30–33]. In fact, sudden unexpected death in epilepsy (SUDEP) describes the death of epileptic patients with unknown causes and is a major driver of premature death for those people [30].

Epileptic seizures can be of different types. As of 2025, the International League Against Epilepsy classifies seizures in four main classes: focal, generalized, unknown and unclassified [34]. Focal seizures are discretely lo-

calized or more widely distributed but have a consistent site of onset and originate from one brain hemisphere. In generalized seizures, bilateral patterns are more important [35].

1.1.2 Treatments for Refractory Epilepsy

Finding treatments for epilepsy is a major research field today. The principal ones are antiepileptic drugs (AEDs), surgery and neuromodulation. Drug-based treatments are the preferred option as they allow patients to live seizure free. However, about 30% of the patients do not respond adequately to anti-epileptic drugs and need another form of treatment. Patients are typically diagnosed with refractory epilepsy (i.e., drug-resistant epilepsy) when the trials with two different AEDs are ineffective [36–38]. Fig. 1.1 presents a flowchart of treatment options.

Surgery is a curative procedure consisting in resecting the epileptogenic zone (i.e., brain tissues identified as seizure focus). It is suggested to patients suffering from refractory epilepsy with focal seizures if the two following conditions are met: (i) the seizure focus is clearly identified, and (ii) it is safe to remove the known seizure focus in terms of neurological outcome [39]. To evaluate those conditions, EEG monitoring and neuroimaging during seizures at hospital prior to surgery are necessary. Epilepsy surgery can offer seizure freedom, but the outcomes of that procedure strongly depend on the type of seizures and the type of surgery [40]. A significant number of patients are either ineligible to surgery or reluctant to undergo that procedure [38]. As a result, epilepsy surgery is rarely used [41].

When the conditions for resective surgery are not met or when the patient refuses the procedure, neuromodulation is preferred as a palliative treatment. It comes in different approaches and consists in interfering with the nervous system to prevent or abort ictal events (i.e., seizures). It should be noted that neuromodulation is also used for treatment of other neurological conditions such as Parkinson's disease, essential tremor, and depression [42, 43]. Three neuromodulation modalities are currently used for epilepsy: deep brain stimulation (DBS), responsive neurostimulation (RNS) and vagus nerve stimulation (VNS). DBS and VNS are approved in Europe and in the US, whereas RNS is only approved in the US [38, 44]. Those three neuromodulation techniques are presented next and compared in Table 1.1.

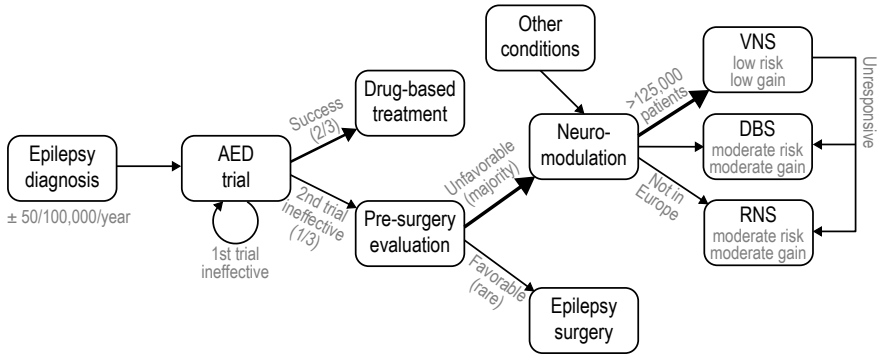


Fig. 1.1 Flowchart of treatments proposed in epilepsy inspired by [38]. Bold arrows indicate the most used options and decisions.

DBS consists in intermittently stimulating the anterior nucleus of the thalamus, deep inside the brain. The implantable pulse generator (IPG) is a pacemaker-like device placed in the patient's chest that delivers electrical pulses to the thalamus via depth electrodes following a pre-defined cycle in an open-loop manner. DBS generally has a good patient response, as shown in Table 1.1. DBS can however also generate severe adverse effects, from implant site pain to mood changes and depression. It is seen as a moderate-risk and moderate-gain therapy [38].

RNS is another type of brain stimulator suggested to patients whose seizure focus is clearly identified. The IPG is placed in the skull and uses intracranial EEG (iEEG) measurements to detect seizure-related electrical patterns. Upon detection, electrical stimulation is delivered to interrupt the seizure, thus completing a closed-loop operating mode. Overall, the efficacy of RNS is similar to that of DBS [38, 46]. The expected adverse effects are also similar but less frequent in the case of RNS. Nevertheless, a major flaw in invasive neural recording systems is the short lifespan of penetrating electrodes. Accurate positioning of the electrode close to the neurons is required, and maintaining the proximity and stability over time is challenging. As a result, the quality of the recordings decreases over time [47]. The only approved device for this type of neuromodulation is the NeuroPace® Responsive Neurostimulator [48]. An appreciated functionality of that RNS device is to provide a log of detected ictal events, which can be used by physicians at follow-up visits.

VNS is a less invasive neuromodulation technique that targets the left vagus nerve in the neck. Similarly to DBS, the IPG is located in the chest.

Table 1.1 Efficacy and adverse effects of different neuromodulation methods. Adapted from [38].

	DBS	RNS	VNS
Target zone	Anterior nucleus of the thalamus	Ictal onset zone	Left vagus nerve
Stimulation type	Open loop	Closed loop	Open or closed loop
Reduction in seizure frequency after 3 months	44%	42%	31% / 19%▷
50% responder rate◁ after 1 year	43%	44%	37% / 50%▷
Seizure free after 2 years	13%	9%	0%
Implant site infection*	13%	12%	Not available
Frequent adverse effects	Paraesthesia; Implant site pain	Paraesthesia; Implant side pain; Headache	Hoarseness; Paraesthesia; Coughing
Possible long-term disorders†	Depression; Suicidality; Memory complaints	Depression; Suicidality; Memory complaints	Not reported
Level of invasiveness	High	High	Moderate
Chance of long-term seizure freedom	Low	Low	Low
Average gain in quality of life	Moderate	Moderate	Moderate

◁ Defined as the proportion of patients achieving a reduction in seizure frequency of at least 50%. * At long term. † Disputed association with neuromodulation. ▷ E-37 trial with closed-loop feature enabled [45].

Efficacy evaluations come from multiple studies and the comparison should be interpreted with caution.

In the last 25 years, more than 125,000 people have been implanted with a VNS system [42, 49], making it the most popular neuromodulation technique for epilepsy. VNS is also approved as treatment for other diseases such as depression, which is a comorbidity of epilepsy. The efficacy of VNS in epilepsy treatments is slightly less than that of DBS or RNS but the invasiveness is lower. Regarding the adverse effects of VNS such as voice alteration, those are mild and reversible whereas brain stimulation-related depression and memory problems are considered more severe. Additionally, the adverse effects of VNS typically decrease over time [50]. VNS is thus seen as a low-risk low-gain method. However, a better therapeutic efficacy can be expected from a closed-loop form of VNS [51–55], where the stimulation parameters are adapted as a function of the state of the patient, boosting the stimulation intensity at seizure onset. With a closed-loop implementation, it is estimated that VNS could be elevated to a low-risk medium-gain method. It should be noted that VNS also significantly reduces the risk of SUDEP [31, 56] and that VNS is the only neuromodulation modality approved for children.

Thanks to its low cost, low risks, low invasiveness, and technique maturity, VNS is by far the preferred neuromodulation technique for the treatment of epilepsy [57]. On the other hand, closed-loop brain implants involving the measurement of iEEG signals present some ethical issues that we analyze in the next section.

1.1.3 Brain-Computer Interfaces: Medical and Ethical Considerations

BCIs can be used for capabilities enhancement, entertainment or healthcare purposes, creating a strong human-machine symbiosis. However, this recent field raises various ethical, medical and social challenges that should be discussed alongside or prior to technological development.

BCIs designate devices connecting brain signals and digital technologies. While no clear definition exists, technologies identified as BCIs usually have the ability to detect and classify brain activity, and to provide feedback to the user in real time, forming closed-loop interactions [58]. It is unclear whether purely stimulating devices should be included in the definition of BCI or not [59].

BCIs can be used for a wide range of applications, as studied in [60]. In the medical field, those are used for RNS, but also as therapy for patients suffering from post-stroke memory deficits by providing reward and feed-

back to modulate specific brain rhythms [61]. Moreover, post-stroke patients can benefit from BCIs for neuro-motor rehabilitation [62]. Finally, BCIs are also used for assistive purposes, such as helping for speech and overall communication [63, 64].

Brain interfaces are used in other fields as well, from recreative purposes to cognitive analyzes and enhancement of human capabilities. First, there are multiple examples of EEG monitoring applications when the user performs physical or cognitive tasks (e.g., driving [65]), allowing to optimize the work environment or to perform emergency actions. Second, for educational purposes, BCIs are suggested to track the level of attention of students during classroom activities as a feedback to the teacher [60]. Next, in the entertainment industry, users could play video games by means of EEG-based controls [66]. EEG sensors can also be integrated into virtual reality headsets to enhance user immersion [60]. Then, the marketing industry can benefit from BCIs, with the emerging field of neuromarketing. Although the definition of that term is vague, it includes the study of the cognitive and emotional response of consumers to a marketing stimulus through EEG. That field faces many controversies, such as concerns that advertisers might find a "buy button" in the consumer's brain [67]. Finally, cyborgs are defined as the combination of organic and machines in a single being. With today's BCI technologies, different types of animal cyborgs have been developed. For example, stimulating specific brain areas in a rat can enhance its vision capabilities [68], or control its movements [69]. Neuralink is a major company developing systems-on-chip (SoCs) capable of simultaneous high-precision neural recording and brain stimulation for clinical applications [70]. However, that company targets to go beyond medical applications to create a symbiosis between humans and digital technologies such as artificial intelligence through brain implants [71].

Alongside the applications of BCIs, safety issues are often mentioned [59, 60]. First, there are risks linked to the surgical placement of an implant in the brain, from infection to tissue damage. Second, the reversibility is also questioned: can the brain function as normal if the implant is removed? Third, BCIs can lead to user dependence, and failure at critical instants could put the user in dangerous situations [59]. Finally, hacking BCIs is also possible. For example, it is possible to inject false brain waves into the EEG recording device and obtain specific desired outputs [72].

For the patient or user, BCIs can also have non-physical impacts. For example, EEG decoding inaccuracies in a speech assistive technology could place the patient in unwanted or awkward situations, worsening the so-

cial stigma. Some studies also report psychiatric complications in patients implanted with a DBS system [73]. However, it is unclear whether those observed effects are caused by brain stimulation [74,75]. Concerns about losses of identity are also raised in [76]. The BCI technology could become part of the user's nervous system and shape their identity. This can impact their autonomy and disrupt self-cognition upon disconnection.

On a larger scale and in the wide spectrum of opinions regarding brain implants, the massive development of advanced BCI technologies is feared to lead mankind to a dystopian future if no consumer and personal rights safeguards are put in place [77]. One can foresee scenarios including massive surveillance, thought manipulation and emotion control through BCIs, endangering fundamental libertarian values, facilitating the rise of totalitarianism, and enabling the general control of human subjects [78,79].

Therefore, the proven risks of using BCIs specialized for epilepsy treatment are similar to those of other implantable devices. Given the medical benefits of those technologies, one could argue that research toward innovations in such devices is clearly worth the risks. However, neurotechnologies are subject to dual use. The term *dual use* is primarily intended to designate the application in the military sector of technologies intended for civilian use. It is transposed and extended in this thesis to describe how scientific and medical breakthroughs can be used for purposes unintended by researchers, as suggested in [80].

To conclude, research on closed-loop neuromodulation based on iEEG for epilepsy treatment may offer significant therapeutic benefits. However, the likelihood of dual use of those technologies could facilitate the development of aforementioned non-medical applications where the risks-benefits ratio still has to be evaluated. Therefore, it is our choice to orient this work toward other neuromodulation technologies that do not rely on brain implants nor recordings of brain signals. We believe that closed-loop VNS based on vagus nerve recordings has a much less important dual-use potential thanks to its looser connection to brain tissues.

1.1.4 Closed-Loop Vagus Nerve Stimulation

VNS is a neuromodulation technique consisting in stimulating the left vagus nerve. While the exact mechanisms of action still have to be understood, it has been shown that VNS works by activating specific brain areas through the afferent fibers of the vagus nerve [81].

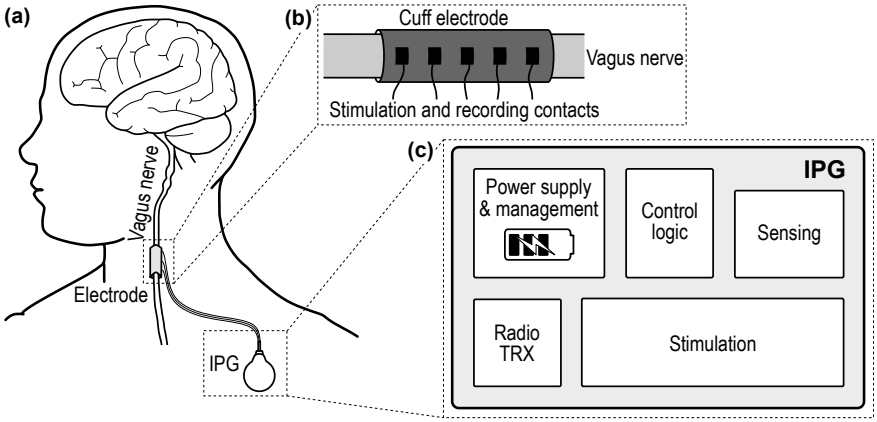


Fig. 1.2 (a) Overview of an implantable VNS system. (b) Cuff electrode used for stimulation and recording. (c) Block diagram of a typical IPG.

The most widely adopted VNS devices are the ones from LivaNova, such as the AspireSR M106 and the SenTiva M1000 [52]. Those products offer open-loop, on-demand and/or closed-loop neuromodulation. A typical implantable VNS system similar to the ones from LivaNova is presented in Fig. 1.2. The IPG is located in the chest and includes a power supply, a radio module, a control block and a stimulator. In case of on-demand or closed-loop operation, it also includes sensing capabilities.

A wide range of different powering techniques are possible for implantable electronics [82]. However, most nerve stimulators today are powered by primary or rechargeable bio-compatible batteries [42]. On the one hand, primary batteries are non-rechargeable and thus have a significantly shorter lifetime than their rechargeable counterparts. On the other hand, rechargeable batteries have a lower energy density, require additional circuitry for wireless recharge and impose a burden on the patient. For a given battery volume and a maximum lifetime, rechargeable batteries offer a slight advantage. However, the implant volume is often dominated by connectors, such that the choice of battery technology should not be primarily dictated by volume constraints. The most popular VNS devices are supplied by lithium-carbon monofluoride primary batteries of capacity from 1,000 to 2,500 mAh. The limited battery capacity makes low power consumption an important design objective to maximize the battery lifetime [42]. Since battery replacement involves a surgery, the system should be designed for a lifetime of multiple years.

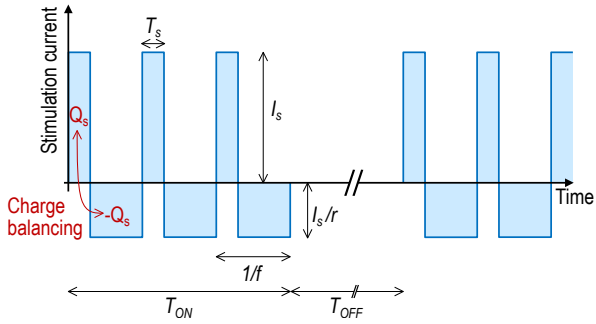


Fig. 1.3 Vagus nerve stimulation current waveform with the definition of stimulation parameters. Charge balancing is achieved by alternating between positive and negative currents.

The IPG is connected to the vagus nerve in the neck via an electrode. Several electrode types exist to interface the peripheral nervous system: extraneural, intraneural and regenerative. There is an important trade-off between nerve damage and selectivity of nerve fibers activated by stimulation. Extraneural electrodes are the least invasive ones but also offer the lowest selectivity [83]. Cuff electrodes are of the extraneural type and are used in many VNS devices and experiments [84–86]. Those electrodes are placed around the nerve and can be used for both stimulation and recording, such as illustrated in Fig. 1.2(b). Intraneural and regenerative electrodes are considered too invasive for long-term implants.

Neuromodulation is achieved by delivering electrical current to the nerve. In order to avoid nerve damage due to charge accumulation at the electrode-tissue interface, the net electrical charge delivered should be equal to zero [17, 42]. The stimulation current waveform thus follows the pattern illustrated in Fig. 1.3, where phases of high positive currents are followed by longer phases of negative currents with the exact opposite charge. Circuit-level techniques are required to ensure an exact charge balance [42]. The stimulation current is composed of pulse trains during 'ON' periods, followed by 'OFF' periods of about 5 min. Typical values of the stimulation parameters are shown in Table 1.2. To adapt the stimulation to the patient's needs, those parameters are usually adapted by the physician at follow-up visits. The parameters are thus tuned manually, usually by increasing the stimulation amplitude to improve the efficacy of the treatment. However, larger currents can lead to more severe adverse effects and reduce battery life.

Table 1.2 Typical stimulation parameters for open-loop VNS [50,87].

Parameter		Value(s)
Pos/neg ratio	r [-]	60 - 200
Output current	I_s [mA]	0.25 - 3.0
Pulse width	T_s [µs]	250 - 500
Frequency	f [Hz]	20 - 30
ON time	T_{ON} [s]	30
OFF time	T_{OFF} [min]	5

VNS comes in different modalities illustrated in Fig. 1.4. Open-loop stimulation is the standard technique: the stimulation current follows predefined schedules with fixed parameters to prevent seizures on the long term. However, stimulating at seizure onset in a closed-loop mode provides acute effects to abort seizures and helps reach a better overall efficacy [54,55]. Adaptive stimulation modalities are thus introduced to adapt the stimulation parameters to the instantaneous state of the patient. With on-demand stimulation, the patient or a caregiver can deliver a stimulation by passing a magnet over the generator when they feel a seizure coming. This on-demand VNS has demonstrated clinical advantages to terminate seizures [88]. However, this technique is limited since the patient might be asleep or unaware of a starting seizure, and the magnet might be out of reach [89]. Closed-loop stimulation is a more recent development consisting in detecting seizure onset via biomarkers and automatically delivering a stimulation at that instant.

In Fig. 1.4(c)-(e), closed-loop VNS is illustrated for three different biomarkers: heart rate (HR), EEG, and VENG. HR-based seizure detection is included in the commercially available devices from LivaNova [52,90]. Those systems trigger extra stimulation current upon the detection of tachycardia, i.e., HR increases by at least 20%. The HR can be sensed by the IPG or the electrode on the vagus nerve, without requiring additional bulky components. Some tachycardia events indicate seizures, although ictal-related HR variations vary strongly among patients. Several studies have shown that HR-based seizure detection has a poor specificity [45,91], leading to a high false-alarm rate.

Closed-loop VNS based on EEG feedback is a more recent field and not yet available in commercial devices. Since EEG is considered the gold

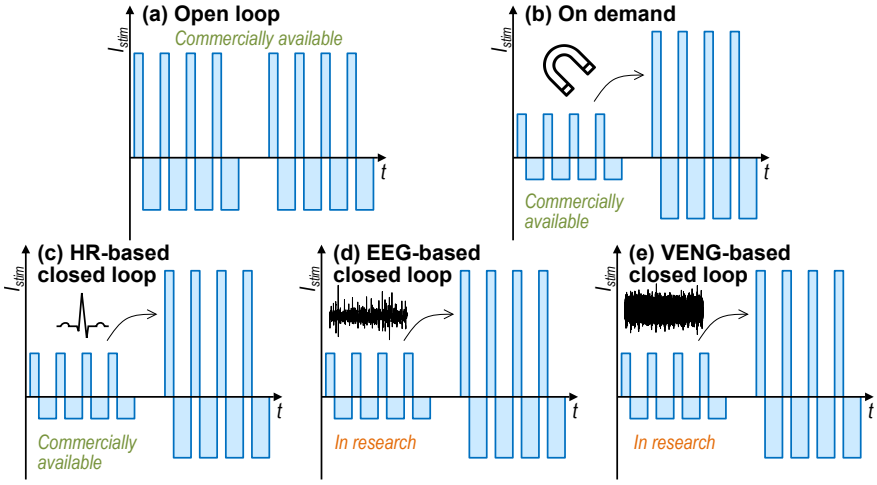


Fig. 1.4 Illustration of different VNS modalities: (a) open loop, (b) on demand with magnet activation, (c) closed loop with HR feedback, (d) closed loop with EEG feedback and (e) closed loop with VENG feedback. Option (e) is studied in this work.

standard for seizure detection, it could provide better seizure detection performance than the HR. [13] presents a closed-loop VNS system using a wearable scalp EEG recorder that shows good seizure detection accuracy in a preliminary study. However, wearable EEG headsets are impractical to wear daily. Implanted iEEG sensors could offer a similar or better seizure detection accuracy but are significantly more invasive than HR sensors and hold greater dual-use potential, as explained in Section 1.1.3.

It was recently proven that seizure biomarkers could be detected from vagus nerve activity, i.e., the vagus nerve electroneurogram [21–23]. In [23], generalized tonic-clonic seizures were induced in rats subjects by injecting pentylenetetrazol (PTZ). The VENG was recorded using a tripolar cuff electrode tied around the vagus nerve and the neural origin of the recorded signals was verified. The follow-up analysis [92] proposed an automatic VENG-based detection of seizures that reaches a perfect detection on the rat subjects. Detecting seizures from vagus nerve activity using the same cuff electrode for both sensing and stimulation could offer a minimally invasive solution for closed-loop VNS. Therefore, VENG-based sensing is the VNS modality studied in this thesis.

1.1.5 VENG Sensing: System Requirements

The engineering behind the acquisition of spontaneous vagus nerve activity is scarcely addressed in the literature. Fig. 1.5 shows the number of scientific publications available on IEEEXplore mentioning several biopotential signals. While electrocardiogram (ECG) and EEG have an increasing popularity in engineering-related publications, the field of VENG signals acquisition is limited to a few papers in the last years. This observation leads to two conclusions. First, to design VENG acquisition circuits, techniques introduced in other applications such as ECG and EEG should be leveraged and adapted to the VENG application. Second, there exists a gap between the biomedical field where VENG-related experiments have been conducted, and the field of integrated circuit (IC) design that still has to address the acquisition of VENG signals in an ultra-low-power (ULP) implant. This is particularly important since VENG signals present specificities that are linked to performance requirements for the acquisition circuit. The specificities of the signal and recording system are: (i) the nature of the signal, (ii) its typical amplitude, (iii) its bandwidth, (iv) the presence of interference, and (v) the power budget for a closed-loop VNS system. Those are detailed next.

i) ***Signal nature:*** the vagus nerve is composed of thousands of fibers with diameters in the µm range. Spontaneous nerve activity consists of action potentials (APs) travelling along those fibers. When interfacing the vagus nerve with an extraneural cuff electrode, only the external membrane potentials are recorded. Spikes observed in the signal are thus a combination of the APs from multiple fibers. Depending on the number of simultaneously activated nerve fibers, the amplitude of the combined APs varies. The shape of the detected spikes can be analyzed to discriminate the type of activated fibers in the nerve [93]. In this work, the recorded combinations of APs are referred to as action potentials for simplicity. In [23], the combined firing rate (i.e., the spiking frequency) of all fibers in the nerve observed during acute recording on rats is around 120 Hz. Variations in AP amplitude and firing rate are used in [92] to detect ictal events.

ii) ***Signal amplitude:*** the amplitude of the recorded APs varies with the type of electrode used and with the inter-contact distance on the electrode [23, 93]. The larger the distance, the higher the amplitude of the signals. In [23], APs with an amplitude around 20 μV_{PP} are recorded in anaesthetized rats for an inter-contact distance of 2 mm. Given the reported variability of AP amplitude, a VENG recording circuit should be able to faith-

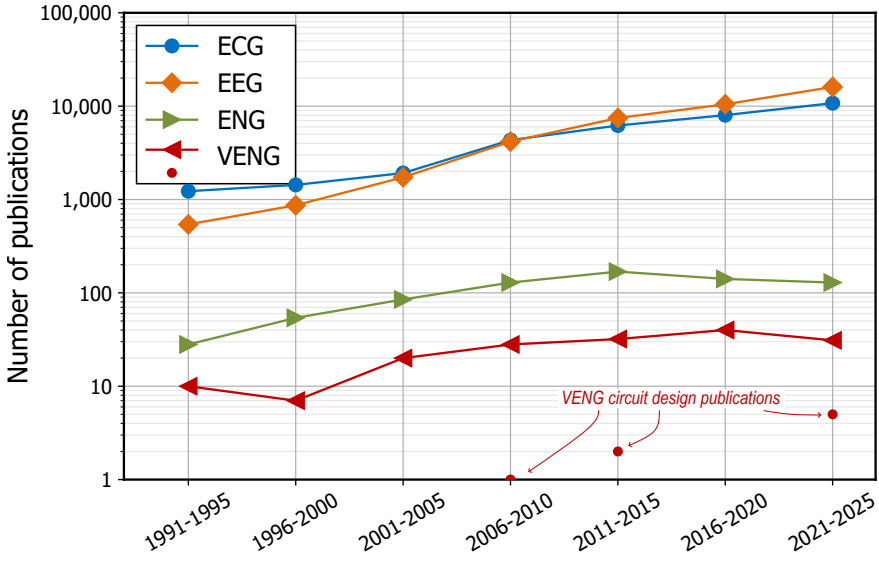


Fig. 1.5 Number of published papers mentioning biopotential signals available on IEEEXplore over five-year periods. Research terms used: ("All Metadata":electrocardiogram) OR ("All Metadata":ECG) OR ("All Metadata":electrocardiography) OR ("All Metadata":EKG) OR ("All Metadata":"heart activity") OR ("All Metadata":"heart recording") for ECG, ("All Metadata":electroencephalogram) OR ("All Metadata":electroencephalography) OR ("All Metadata":EEG) OR ("All Metadata":iEEG) OR ("All Metadata":ECoG) OR ("All Metadata":sEEG) OR ("All Metadata":aEEG) OR ("All Metadata":electrocorticography) for EEG, ("All Metadata":electroneurogram) OR ("All Metadata":"nerve activity") OR ("All Metadata":"nerve recording") for ENG, and ("All Metadata":"vagus nerve electroneurogram") OR ("All Metadata":"vagus nerve activity") OR ("All Metadata":"vagus nerve recording") for VENG with additional requirements ("Publication Title":circuits) OR ("Publication Title":sensors) for circuit design-related publications.

fully acquire APs with an amplitude from 10 to 30 μV_{PP}. Recording signals with such a low amplitude is highly sensitive to biosignal interference and noise from the acquisition setup. In human recordings, the inter-contact distance can be larger [84], thereby increasing the AP amplitude [23] compared to experiments on rats.

iii) ***Signal bandwidth:*** the frequency band of the VENG signals goes up to the kHz range. For the acute recordings presented in [23], the signal is band-pass filtered to keep the [12-12k] Hz band. Other works refer to different bandwidths, e.g. [500-10k] Hz for electroneurogram (ENG) sensing [24], and [300-3k] Hz for AP detection from the VENG [94, 95]. In this work, a bandwidth from 0.3 to 10 kHz is considered as specification for the acquisition circuits.

iv) ***Interference:*** on top of spontaneous nerve activity, cuff electrodes recordings are also sensitive to interference from nearby muscles. The

electromyogram (EMG) from muscles in the vicinity of the cuff results in an electric field inside the electrode. The cuff has a linearization property, which means that the EMG electric field results in a linear gradient along the cuff [96]. The EMG potential at the electrode contacts can have an amplitude up to the mV range and a frequency band overlapping that of the useful VENG signal. Filtering and other circuit-level techniques should thus be implemented to attenuate the EMG interference such that the VENG signal is detectable. In addition to EMG, in a closed-loop VNS system, stimulation results in high-amplitude artifacts at the electrode contacts. If not dealt with, those artifacts could saturate or damage the recording circuits.

v) ***Power budget:*** the power budget of a closed-loop VNS system is limited by the capacity of its battery. The AspireSR M106 VNS device has a lithium-carbon monofluoride battery with a volume of 4.92 cm^3, a capacity of 1,700 mAh and a voltage of 3.3 V. Assuming the same battery for a closed-loop device, it gives an average power consumption of maximum 64 µW for a 10-year lifetime. In [42], it is estimated that an average power around 6 µW delivered to the nerve is necessary to achieve a therapeutic effect via VNS to treat epilepsy. The 6-µW value is computed from the stimulation current waveform (Fig. 1.3) assuming $I_s = 1.5$ mA, $T_s = 250$ µs, $f = 20$ Hz, a T_{ON} of 100%, and an inter-contact impedance of 500 Ω. The stimulator power consumption thus depends on the stimulation parameters set by the physician, with a significant impact on battery life [51]. In [42], a maximum efficiency of 25% is also presented for stimulators, stating that 75% of the implant power goes to the control unit or is lost in various circuit blocks (e.g., power management and stimulation current generation). The sensing parts of the system should thus have a µW-range power consumption for signal acquisition and seizure detection. In this work, a power budget of 10-15 µW is specified for the signal acquisition parts. However, minimizing it is beneficial to allocate a larger budget for the seizure detection unit, or to increase the lifetime of the battery.

1.2 Analog Design: Biopotential Front-End Circuits

ICs designed for the recording of VENG signals face stringent specifications in terms of power consumption, intrinsic noise and rejection of interference. The design of low-power analog circuits for biopotential signals

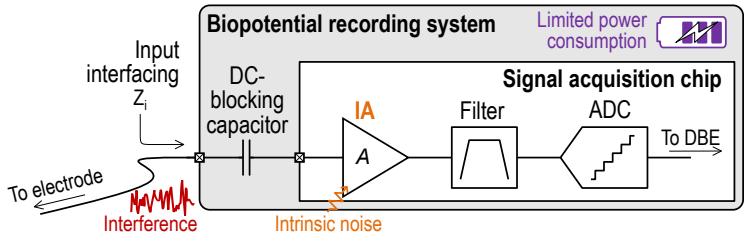


Fig. 1.6 Simplified block diagram of the AFE with highlights on the three main design challenges introduced in this chapter.

acquisition is a wide field. However, as demonstrated in Section 1.1.5, the literature on ECG and EEG applications is more widespread than VENG-related publications. Since those biopotential sensing applications share many design challenges and considerations with VENG recording, this section presents design techniques from the literature on ECG and EEG sensing that can be leveraged in a VENG-sensing circuit. The similarities and differences regarding circuit design for the different applications are also discussed in this section.

Fig. 1.6 presents a conventional architecture of an AFE designed for the acquisition of biopotential signals. The on-chip components form a traditional structure with amplifier, filter and ADC. The digitized signal is sent to the digital back-end (DBE) for signal processing. As illustrated, the main analog design challenges addressed in this work are: (i) ULP operation of each circuit block, (ii) noise reduction in the acquisition circuits, and (iii) rejection of interference added to the input signals. This work also addresses the interfacing between the electrode and the input of the recording system, and the analog-to-digital conversion.

1.2.1 Input Interface

To interface an implanted IC with an organic nerve, precautions must be taken to avoid injecting DC current, as net charge injection may result in tissue damage [97]. The ISO 14708-1 standard states that no leakage current of more than 1 µA should be sustained from implantable electronics [98]. To ensure this limit even in case of IC malfunction (e.g., leakage from the electrostatic discharge (ESD) protection), large DC-blocking series capacitors are often placed off chip in commercial devices [99, 100].

Fig. 1.7 presents a model for the impedance of the tissue-electrode in-

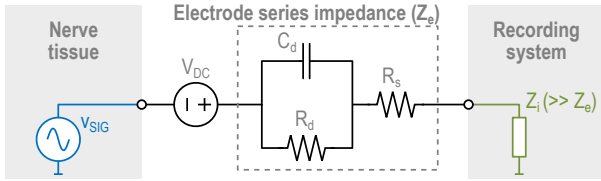


Fig. 1.7 Model of the series impedance of the tissue-electrode interface, inspired by [104].

terface, that acts as a series impedance for the electrode. The total series impedance Z_e can vary from one type of electrode to the other. In the case of skin-surface EEG or ECG recordings with dry electrodes, the series impedance can reach the MΩ level [5]. It is thus necessary for the recording system to have an input impedance Z_i significantly larger than Z_e to limit signal and signal-to-noise ratio (SNR) degradation due to the voltage divider. Z_i includes the DC-blocking capacitor from Fig. 1.6 but is usually characterized in the middle of the signal bandwidth and is therefore not affected by series capacitors in that case. In multi-channel recordings, a mismatch in the electrode series impedances can also lead to gain mismatch between channels if Z_e is not negligible compared to Z_i. Depending on the instrumentation amplifier (IA) topology adopted in the AFE, impedance-boosting techniques might be necessary to reach a sufficient Z_i, possibly increasing the design complexity and power consumption. In the case of VENG recording with a cuff electrode, Z_e is in the kΩ range. In [101], the measured impedance Z_e is lower than 7.5 kΩ. Additionally, [102] presents a 28-day long chronic experiment conducted on rats, and reveals no significant drift in electrode impedance over time. In human implants, the cuff can be larger and thus benefits from a lower impedance. [103] indicates that an electrode impedance larger than 1.7 kΩ is a sign of faulty contact for human recording with a cuff electrode. Therefore, in this work, we assume $Z_e \approx 1.5$ kΩ. As a result, the constraints on the input impedance of the AFE are relaxed compared to ECG or EEG recording.

In Fig. 1.7, the DC voltage source V_{DC} represents the half-cell potential that develops between the electrode and the tissue. Its value depends on the materials used for the electrode and can be higher than 100 mV. This phenomenon results in an additional DC bias at the input of the AFE that is often referred to as the electrode DC offset (EDO). If the EDO is directly applied to the input of the IA, it can be amplified and saturate the amplifier, making the useful signal invisible. If a DC-blocking capacitor is placed in

series between the electrode and the recording IC, the EDO is rejected. In other cases, specific circuit-level techniques such as DC servo loops must be applied to minimize the impact of the EDO.

1.2.2 Rejection of Interference and Artifacts

VENG recordings are subject to EMG interference and stimulation artifacts that should be attenuated down to the noise level for a correct detection of the VENG signals.

Fig. 1.8 presents a model of a tripolar cuff including the representations of VENG signals and EMG interference. In that model, Z_0 represents the impedance of the tissue outside the cuff, $Z_{tAB,tBC}$ are the impedances of the nerve between the electrode contacts, and $Z_{eA,eB,eC}$ model the impedances of the electrode/tissue interfaces. i_{EMG} represents the source of EMG artifacts. Since the cuff has a larger impedance than the surrounding tissue, the near totality of the EMG current flows through Z_0, resulting in a linear potential difference across the cuff given by

$$v_{\mathrm{EMG}} = i_{\mathrm{EMG}} Z_0. \tag{1.1}$$

That voltage can reach the mV level and a frequency band up to a few kHz. The exact characteristics of the EMG depend on the electrode size and location, and on the importance of muscles activity. However, most of the EMG power is located at low frequencies [6, 24].

Since the lower limit of the VENG bandwidth is around 300 Hz, the EMG at lower frequencies can be filtered out, thus eliminating a large part of the interference power. The high-pass filter (HPF) used for that purpose should ideally be placed before any amplifier to avoid distortion or saturation due to the EMG. In addition, the HPF should not add a significant contribution to the total input-referred noise (IRN). Fig. 1.9 presents three configurations that combine HPF and LNA functions. The optimal configuration depends on the desired HPF cut-off frequency and on system specifications. The passive configuration is the simplest one and is used for VENG recording in [25]. The RC components form the HPF and an LNA follows for amplification. For a cut-off frequency close to 300 Hz, the RC product is 530 MΩ·pF, which is difficult to achieve on chip with passive components within a limited area. In [25], the passive HPF is thus implemented off chip. The DC-blocking capacitor can be used to form that off-chip HPF. However, resistor R_i adds thermal noise to the amplifier in-

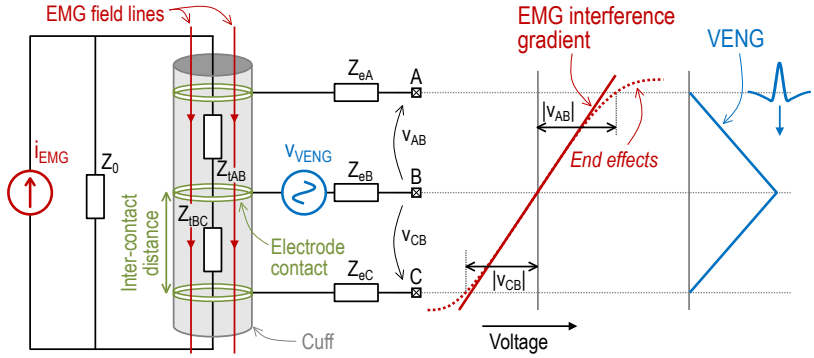


Fig. 1.8 Lumped elements model of a tripolar cuff electrode for ENG recording, according to [105]. Illustration of EMG interference linearization by the cuff. End effects are represented on the EMG potential.

puts, which can be non negligible in certain conditions. The active filter in Fig. 1.9(b) needs R_{fb} and C_{fb} to be implemented on chip. To reach a high RC product, R_{fb} can be implemented using a pseudo-resistor, as illustrated. However, those structures can shift significantly over process, voltage and temperature (PVT) variations. The filter with active feedback, shown in Fig. 1.9(c) and proposed in [106], is a more complex structure based on a DC servo loop (DSL) but is less PVT-dependent than the previous one. The HPF cut-off frequency is fixed by the transconductance G_m of the feedback operational transconductance amplifier (OTA) and the feedback capacitor. It is thus possible to achieve low-noise amplification and high-pass filtering using pF-range on-chip capacitors and no resistors. However, the feedback OTA adds power consumption and noise and is slightly dependent on PVT variations. In this thesis, we propose an alternative to structure (a) by replacing the off-chip noisy resistor by the controlled input impedance of a common-gate differential pair.

Specific techniques must then be used to reject the in-band interference. For that purpose, tripolar electrodes are preferred, as illustrated in Fig. 1.8. Assuming an ideal symmetrical cuff, the EMG voltages sensed between the electrode contacts respect

$$v_{AB,\mathrm{EMG}} = -v_{CB,\mathrm{EMG}}, \tag{1.2}$$

where $v_{AB,\mathrm{EMG}}$ (resp. $v_{CB,\mathrm{EMG}}$) are the voltages due to EMG interference captured between the A and B (resp. C and B) contacts. $v_{AB,\mathrm{EMG}}$ and

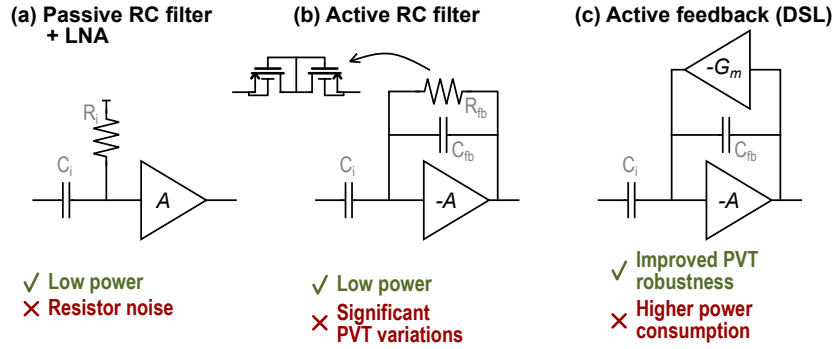


Fig. 1.9 Single-ended representations of pre-amplifier high-pass filtering strategies: (a) passive RC filter with open-loop amplifier, (b) active RC filter, and (c) filter with active feedback.

$v_{CB,\mathrm{EMG}}$ can be summed to cancel out the interference while amplifying the VENG signal. The tripolar electrode can be leveraged in two different IA configurations to perform this summation, as illustrated in Fig. 1.10. The quasi tripole (QT) configuration shorts the two outer electrode contacts. If the cuff is perfectly symmetrical, the resulting voltage at the negative input of the amplifier is the average of v_A and v_C. The true tripole (TT) configuration performs the voltage sum in the analog domain, requiring two input amplifiers and a sum operation. In case of cuff asymmetry, the gains G_{L1} and G_{L2} can be adjusted to maximize the rejection of EMG interference whereas the QT configuration is more difficult to adapt in those situations [24, 105]. The TT architecture however requires two LNAs, apparently doubling the current consumption compared to the QT configuration. However, since the signal amplitude is also doubled in the TT case, the IRN power is halved compared to a single-amplifier architecture. The overall noise-power trade-off is therefore not affected. The power consumption of the summing amplifier in the TT configuration can nevertheless impact the performance of the system if it is not negligible compared to the power consumption of the input amplifiers. In the TT configuration, the output voltage is expressed as

$$v_{\mathrm{TT}} = G_F \left(G_{L1} v_{AB} + G_{L2} v_{CB}\right) \approx -2 G_F G_L v_{\mathrm{VENG}}, \tag{1.3}$$

where G_{L1} and G_{L2} are the gains of the two input amplifiers, G_F is the gain of the summing amplifier, G_L is the average of G_{L1} and G_{L2}, and v_{VENG}

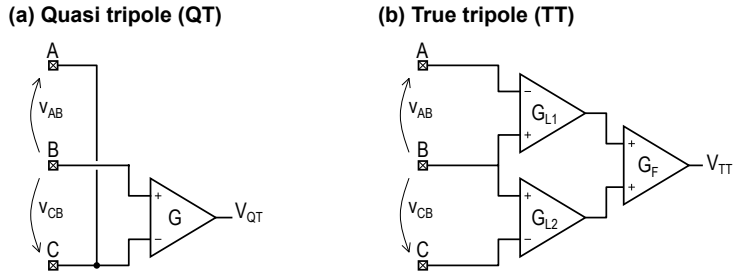


Fig. 1.10 Tripolar IA configurations for EMG-robust acquisition of VENG signals: (a) quasi tripole, (b) true tripole. Inspired by [105].

is the VENG signal. Two limitations impact the rejection of interference in the TT configuration: (i) imbalance in the cuff electrode, and (ii) gain mismatch in the acquisition circuits. In this thesis, both limitations are considered and circuit-level techniques are proposed to mitigate them.

Stimulation artifacts are high-voltage spikes due to the mA-range stimulation currents injected to the nerve when the same electrode is used for stimulation and sensing. Without any specific cancellation technique, those artifacts are applied directly to the inputs of the sensing SoC with three different issues: (i) the VENG signal is invisible during stimulation due to the saturation of the amplifiers, (ii) if the spikes exceed the supply voltage of the sensing SoC, the ESD protection diodes inject leakage current to the nerve, and (iii) if the spikes reach a voltage higher than the maximum tolerated voltage by the sensing SoC, the latter can be damaged. In the context of closed-loop VNS, simultaneous stimulation and recording is not necessary since stimulation is triggered after seizure detection. The easiest solution to the last two issues is thus to disconnect the sensing SoC inputs from the electrode during stimulation in an operation called blanking and used in [70, 107]. As illustrated in Fig. 1.11, since the stimulator SoC is aware of the instants of stimulation, it can control the switches between the electrode and the sensing SoC. In this work, it is assumed that the stimulator SoC is implemented in a high-voltage-tolerant technology to sustain those voltage spikes. A relatively scaled CMOS technology is however used for the sensing SoC to minimize the power consumption of the digital seizure detection module. The blanking switches are thus integrated into the stimulator SoC to sustain those high voltages and ease their control.

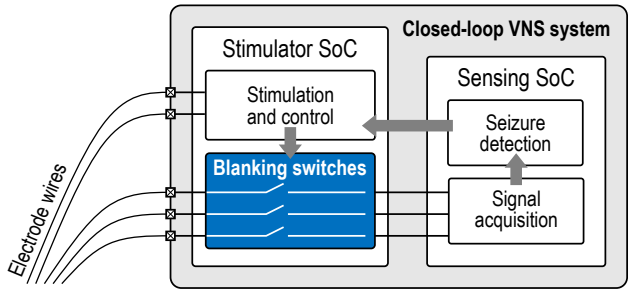


Fig. 1.11 Block diagram of a closed-loop VNS system where blanking is used in the stimulator SoC to protect the sensing SoC from high-voltage stimulation artifacts.

1.2.3 Intrinsic noise

In sensor interfaces, noise from the signal acquisition circuitry is often a major constraint. In biopotential sensing applications, the noise level is particularly critical due to the low amplitude of the input signals, often leading to low SNRs. As shown in Fig. 1.12, the major biopotential signals have a wide variety of amplitude and frequency characteristics. It can be seen that VENG signals have both a very low amplitude and a large bandwidth compared to other signals, making those signals more sensitive to noise than those with higher amplitude or smaller bandwidth.

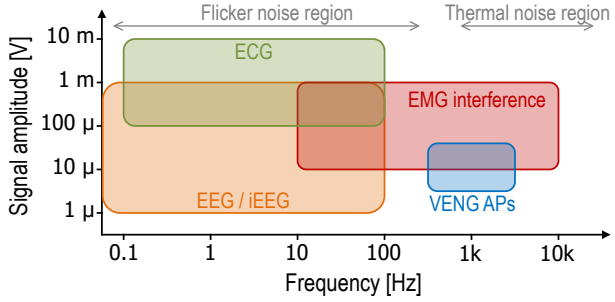


Fig. 1.12 Amplitude and bandwidth characteristics of main biopotential sensing applications, inspired by [2, 108].

In the kHz bandwidth, flicker and thermal noise sources from transistors, resistors, and capacitors dominate the total intrinsic noise. For ECG and EEG applications with a bandwidth limited to around 100 Hz, flicker noise typically dominates. Therefore, modulation-based noise reduction

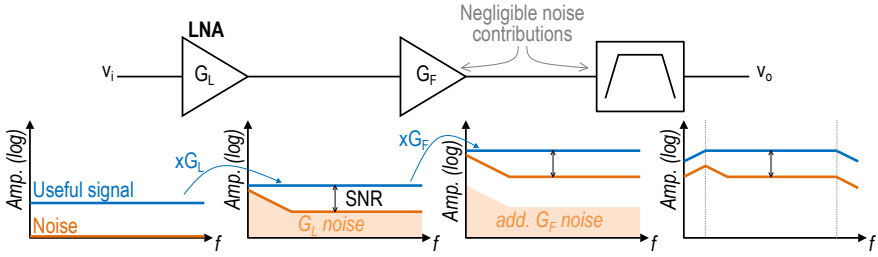


Fig. 1.13 Sketches of signal and noise frequency contents along an AFE, where the LNA is the major noise contributor.

techniques such as chopping are used in those cases. In the context of VENG sensing with a bandwidth in the kHz range, both flicker and thermal noise sources are typically non negligible. The exact repartition and corner frequency depend on the circuit topology and sizing.

Fig. 1.13 represents a typical AFE structure with the evolution of the signal and noise frequency contents. The noise on the input signal is usually low and neglected in this work. The LNA amplifies the signal and adds a significant amount of noise. As represented, an SNR can be computed at the output of the LNA. After the LNA, a high-gain amplifier and a filter follow, impacting both the signal and the noise from the LNA. The noise contribution from those blocks is relatively less important for the overall SNR since the signal is already amplified by the LNA.

Reducing the IRN of a circuit block often comes at the price of higher current consumption and/or larger silicon area. In noise-constrained AFEs, the LNA is thus often a major contributor to the total current consumption and is the focus of many research works focusing on the acquisition of biopotential signals [9, 18, 109–114]. To compare the performance of different LNA or AFE topologies, the noise efficiency factor (NEF) is introduced as figure of merit. It is proposed in [115] with the definition

$$\mathrm{NEF} \triangleq v_{\mathrm{in,RMS}} \sqrt{\frac{I_{\mathrm{tot}}}{4kTV_T f_H \pi/2}}, \tag{1.4}$$

where $v_{\mathrm{in,RMS}}$ is the IRN of the circuit integrated up to $f_H\pi/2$ and expressed in V, I_{tot} is the total current consumption, k is Boltzmann's constant, T is the absolute temperature in K, V_T is the thermal voltage, and f_H is the upper frequency limit of the signal. This definition of the NEF is equivalent to normalizing the IRN voltage to the thermal noise of an ideal

bipolar transistor with the same DC current and with an additional factor of 2 on the noise power. The NEF is thus based on device equations and quantifies how a circuit performs compared to a theoretical noise limit. For a system perspective, the power efficiency factor (PEF) is also introduced in [116] as

$$\mathrm{PEF} = V_{\mathrm{DD}}\,\mathrm{NEF}^2, \tag{1.5}$$

where V_{DD} is the power supply voltage. To first order, V_{DD} does not impact the noise of the transistors in an amplifier. Introducing V_{DD} in the definition of the PEF is thus not related to the bottom-up view of the noise-current performance of devices and circuits but is useful for a top-down evaluation of the performance of a ULP system. In this work, both metrics are reported. The NEF and PEF can be evaluated on a single noise-constrained circuit such as an LNA, or on a complete AFE.

1.2.4 Low-Noise Amplifier Design Techniques

To optimize the performance of the LNA and reach a low NEF, several design techniques exist.

First, chopping is used mainly in amplifiers working at a low frequency, where flicker noise dominates. It consists in modulating the input signal to a high frequency region with lower flicker noise power spectral density (PSD) and where thermal noise dominates. After demodulation, the signal is mostly affected by thermal noise rather than flicker noise. In very-low frequency applications such as HR detection, the flicker noise level is so high that without chopping, the low-amplitude signals are invisible. Chopping mechanisms are thus widely used in circuits targeting low-frequency operation [9, 15, 20, 108, 111, 117]. However, chopping has a few downsides. First, if placed at the input of the circuit without any DC-blocking capacitor, the chopper modulates the EDO and low-frequency interference. Those parasitics can then saturate the amplifier. Additional circuitry such as DSLs can be added to filter out the low-frequency parasitics using an active feedback configuration [108]. However, the range of tolerated EDO and interference remains limited. Second, chopping affects the impedance seen at its input. The input impedance becomes approximately $1/(2f_{\mathrm{chop}}C_{\mathrm{in}})$, where f_{chop} is the chopping frequency and C_{in} is the capacitance seen at the node after the chopper. Considering that the chopping frequency must be significantly higher than the noise corner frequency of the amplifier, the input impedance can be severely degraded

by this technique. Impedance boosting feedback loops are then added to increase the input impedance [9, 20, 108, 117]. Next, since chopping modulates the signal to high frequency, the amplifier must be designed for a larger gain-bandwidth product than for baseband operation. Finally, due to the additional components and specifications on the amplifier, chopping also adds noise and power consumption, therefore degrading the NEF. In the case of VENG sensing with a bandwidth in the kHz range, both flicker and thermal noise sources are usually non negligible. Chopping thus represents a less significant improvement in the noise performance. In this work, other techniques than chopping (e.g., large gate areas) are preferred to mitigate the flicker noise.

The sizing of the transistors in the LNA can also be optimized to minimize the effects of thermal noise. The input components of LNAs are usually a differential pair, as represented in Fig. 1.14. The transistors forming the differential pair generate thermal noise, represented by a parallel noisy current source of constant PSD equal to S_{id}. A property of that noise PSD in A^2/Hz is

$$S_{\text{id}} \propto g_m, \tag{1.6}$$

where g_m is the transconductance of the differential pair [118]. Assuming identical transistors, the noise PSDs are equal. The noise sources are also uncorrelated, such that the noise PSD at the output due to thermal noise of the differential pair is given by

$$S_{\text{out}} = 2S_{\text{id}}R_{\text{out}}^2, \tag{1.7}$$

where R_{out} is the output resistance of the circuit, usually determined by the load. Referred to the input, the IRN PSD is thus

$$S_{\text{in}} = 2S_{\text{id}}/g_m^2, \tag{1.8}$$

$$S_{\text{in}} \propto \frac{g_m}{g_m^2} = \frac{2}{I_{\text{tot}}} \frac{1}{\left(\frac{g_m}{I_D}\right)}, \tag{1.9}$$

where I_{tot} the DC bias current from the source, and I_D is the transistor's drain current. From (1.9), two observations can be made. First, increasing the bias current reduces the IRN, as discussed for the definition of the NEF. Second, the IRN PSD is inversely proportional to (g_m/I_D). Maximizing the (g_m/I_D) (i.e., biasing the differential pair in weak inversion) is therefore an efficient method to reduce the IRN, as used in [9, 18, 114]. However,

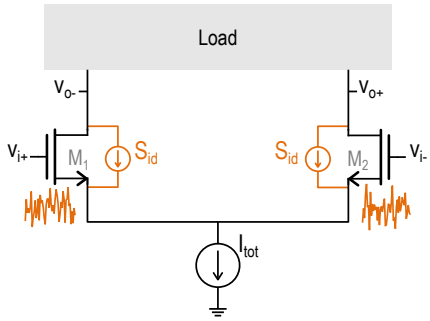


Fig. 1.14 Simplified diagram representing the noise in an NMOS common-source differential pair.

(g_m/I_D) is usually limited to values around 30 V^{-1}, thus bringing a lower bound on the achievable NEF.

Biasing transistors in weak inversion is equivalent to maximizing the transconductance of the differential pair for a given bias current. Although it increases the output noise, it also boosts the gain and thus reduces the IRN. That principle can be leveraged one step further by duplicating the differential pair, as represented in Fig. 1.15. The transconductances of the two differential pairs add up to form a large total transconductance $G_m = g_{mN} + g_{mP}$. Those two differential pairs share the same bias current and this structure does therefore not require any additional current compared to the topology in Fig. 1.14. This technique is thus called current reuse (CR) and is adopted in [113]. Compared to a topology with single use of DC current, the output noise PSD is approximately doubled due to the larger number of transistors, but the IRN PSD is halved thanks to the larger gain and transconductance.

The principle of increasing the total transconductance G_m at constant bias current can be pushed further by stacking multiple OTAs between ground and V_{DD} [9, 119], as represented in Fig. 1.16. The n OTAs are AC-coupled and share the same bias current. The total transconductance G_m increases with n whereas S_{in} decreases by the same proportion. Stacking is thus very efficient to reduce the NEF. Each individual OTA in a stacked amplifier can implement CR, further improving the performance. In [9], stacked circuits with $n = 3$ and $n = 5$ are presented, achieving an NEF of 0.86. However, stacking also impacts the linearity and the output swing of the amplifier. Additionally, a large V_{DD} is required for a large n, thus limiting the benefits on the PEF.

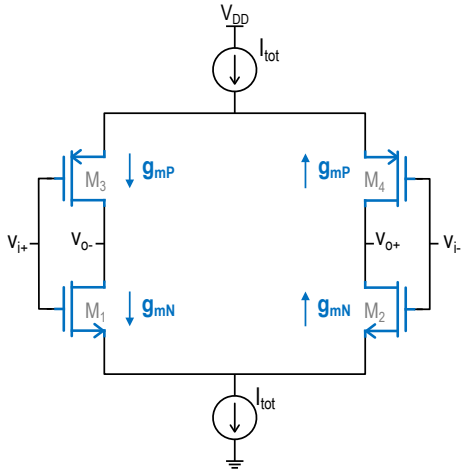


Fig. 1.15 Simplified diagram representing the double differential pair in a current-reuse circuit.

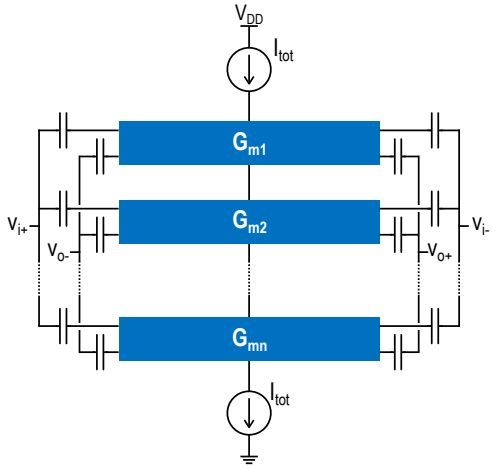


Fig. 1.16 Simplified diagram representing an LNA based on OTA stacking.

To reach noise levels below those of differential pairs, switched-capacitor amplifiers working in discrete time are proposed in [3, 109]. Inspired by DC-DC converter structures, those amplifiers consist in switching the connections of n capacitors between parallel and series. Fig. 1.17 shows a simplified example for $n = 4$. Breaking away from the (g_m/I_D) limit, the performance of those circuits is only limited by kT/C thermal noise and

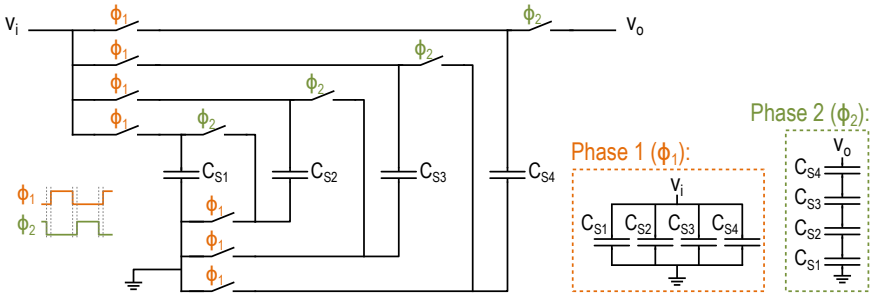


Fig. 1.17 Simplified diagram of a 1:4 series-parallel switched-capacitor amplifier, inspired by [109].

capacitor switching power. Nevertheless, those switched-capacitor amplifiers suffer from different non-idealities such as parasitic capacitances, reduced input impedance, and aliasing due to the discrete-time nature of the circuit. Techniques to overcome these limitations are introduced in [3] but significantly complicate the design, increase the power consumption and require complex non-overlapping clock schemes. It should be noted that the NEF and PEF for the AFE presented in [3] are 0.34 and 0.1, respectively. Those are the best values reported in the literature so far.

1.2.5 Analog-to-Digital Conversion

Analog-to-digital converters (ADCs) are the furthest downstream components in biomedical AFEs, connecting the analog blocks with the digital ones by performing both sampling and quantization of the analog signals. Different types of ADC architectures exist but all are characterized by a sampling frequency f_s, an oversampling rate (OSR), a power consumption, and a signal-to-noise-and-distortion ratio (SNDR). As discussed in [120, 121], successive-approximation register (SAR) and $\Delta\Sigma$ ADCs generally outperform the other architecture types in terms of energy efficiency. Except for the noise-power trade-off, the VENG application does not impose strict constraints on the ADC design, allowing the use of generic ADC architectures and innovations in biomedical applications. However, as presented next, knowledge about the input signal can lead to application-specific optimizations of ADCs.

$\Delta\Sigma$ ADCs are the optimal choice for high-resolution applications [120]. Those consist of an analog $\Delta\Sigma$ modulator working with limited resolution

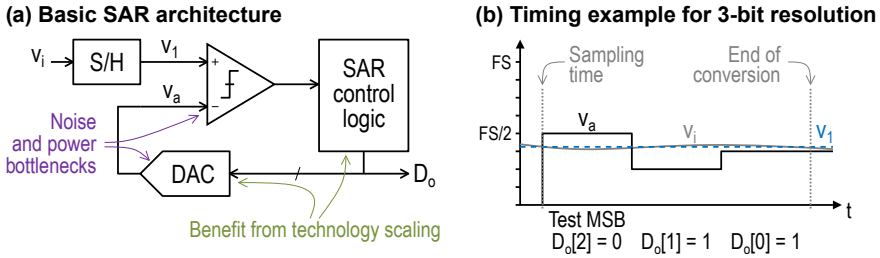


Fig. 1.18 Architecture of a basic SAR ADC (a) and timing overview example (b).

and high sampling rate, followed by a digital decimation filter. The ΔΣ modulator works by integrating the error between the analog input and the digital estimation at its output (i.e., the residue). This results in noise shaping, which pushes most of the quantization noise towards high frequencies. That noise is then filtered out by the digital decimator. Since the ΔΣ modulator works with a large OSR, the specifications on the preceding anti-aliasing filter are relaxed. ΔΣ ADCs are used in biomedical AFEs for high-resolution low-frequency application [12, 122]. However, for VENG recording, the total AFE SNR is limited due to the low signal amplitude and the relatively high noise level in the IA. Therefore, targeting high resolutions in the ADC is not necessary and other architectures such as SAR are more adapted for the moderate-resolution and ULP targets.

A basic SAR ADC is illustrated in Fig. 1.18. The main components are the sample-and-hold (S/H) circuit, the comparator, the control logic and the digital-to-analog converter (DAC). The conversion is done one bit at a time by comparing the analog signal with the DAC output, implementing a binary search algorithm. At the end of the conversion, the DAC output tends to the analog input, as represented in Fig. 1.18(b). Thanks to their design simplicity and good performance, SAR ADCs are widely used in biomedical contexts [123–128].

The SAR control logic is composed of digital gates. It mainly impacts the ADC performance by increasing its power consumption. However, it can significantly benefit from technology scaling. In synchronized ADCs, a master clock at Nf_s is necessary (with N the number of bits). Asynchronous or self-synchronized ADCs on the other hand solely require a clock at f_s, as only the sampling operation is synchronized with the master clock [129].

The comparator is typically designed to only consume dynamic power,

i.e., it only draws current when it performs a comparison operation, and is optimized to reduce that power consumption. It is often composed of a pre-amplifier and a latch. In low-frequency applications, the decision time of the comparator is not a particularly important design constraint [120]. Reducing the power consumption of the pre-amplifier can be done by biasing its transistors in weak inversion or by reducing the voltage variations on the output capacitance [130, 131].

The DAC is a critical component since the performance of the SAR ADC can only be as good as that of the feedback DAC. A popular topology choice consists in implementing the DAC as an array of binary-scaled capacitors. The analog input is sampled on the top plates of the capacitors and the voltage on the bottom plates is controlled by the SAR logic. Capacitors typically have good matching properties and their size scales well in modern CMOS technologies. Additionally, the only power consumption of the capacitive DAC is used for dynamic switching. Innovations on the capacitive DAC mostly consist in acting on the design of the switches, on the switching scheme, or on the capacitor value and layout.

Various implementations of DAC capacitors are presented in [120, 132], going from foundry-available components to custom implementations using metal stripes. Fig. 1.19 shows two custom capacitors implementations presented in [120] that allow to minimize the size and capacitance value while maintaining good matching properties. Custom capacitors in Fig. 1.19(a) can be used for sub-fF capacitance values. To compensate for any edge effect and impact of the interconnect of those devices, delta-length capacitors are introduced in [132] and shown Fig. 1.19(b). Those devices have an effective value that depends on the difference between two capacitances, therefore cancelling the impact of edge effects and interconnects. Both custom implementations in Fig. 1.19 can be drawn using multiple metal layers, improving the density of the DAC. It should however be noted that the capacitance values of those implementations can only be extracted from post-layout parasitic extractions and that no variability model is usually available for those characteristics. Experimental tests on custom capacitors are therefore necessary before integration into an ADC, which strongly limits the ease of use of those implementations.

The main sources of noise in SAR ADCs are (i) quantization noise, (ii) kT/C sampling noise in the capacitive DAC and (iii) noise in the comparator. The relative importance of each source is dependent on the implementation. For DACs with minimum-size capacitors, kT/C noise can be dominant. In [133], a kT/C-noise cancellation technique is proposed, con-

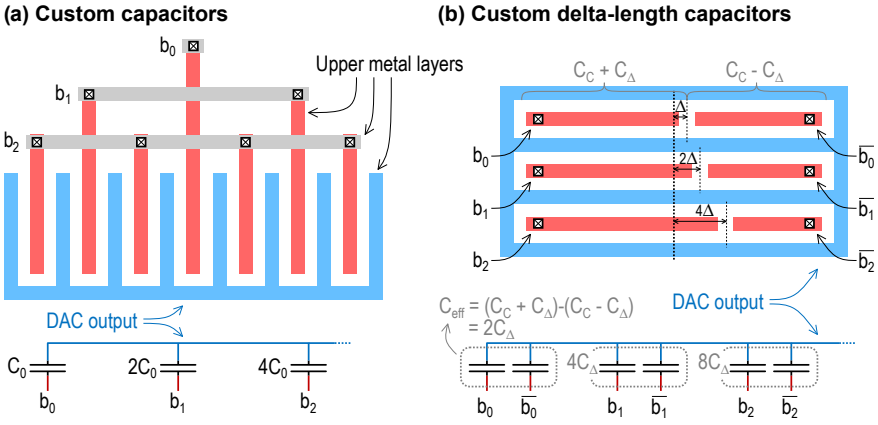


Fig. 1.19 Illustrations of DAC capacitor implementations represented for 3 bits: (a) custom length-based, and (b) custom delta-length. Blue and red colors indicate different nodes. Gray colors designate interconnects. Adapted from [120, 132].

sisting in treating the noise as an offset that is cancelled by an additional capacitor between the comparator pre-amplifier and the latch. The quantization noise can also be reduced by performing oversampling at the cost of higher power consumption. For further noise reduction, noise shaping SAR ADCs are recent innovations that combine the high resolution of the noise shaping properties of ΔΣ ADCs and the power efficiency of SAR architectures [134–136]. Those work by adding a loop filter that integrates the residue before the ADC, thereby performing noise shaping. Compared to ΔΣ architectures, the specifications on the loop filter are relaxed, therefore reaching higher power efficiency.

Innovations in ADC design can also be achieved for a specific applicative context with a good knowledge of the input signal. In [137], a level-crossing ADC is presented for time-sparse applications such as ECG acquisition. In those architectures, digitization is only performed when the input signal exceeds a pre-defined threshold, detected with comparators. Despite the overhead in additional analog blocks and digital synchronization, those structures represent a significant improvement in average power consumption for applications such as ECG, for which the signal is composed of time-sparse pulses. The dynamic reconfiguration of the acquisition circuits for time-sparse signals can be pushed further to the whole AFE, as done in [10]. The AFE switches between low and high-accuracy modes between ECG pulses detected in the digital signal processing module. In the

case of VENG recording, the lower SNR and the higher frequency of pulses (i.e., APs) a priori impacts the feasibility and the benefits of this technique, although quantitative studies could be performed to explore these architectures.

Considering the tremendous performance evolution of ADCs in recent years [121], biomedical ADC-direct front-ends have gained in popularity in the recent years. Those structures consist in feeding the electrode signal directly into a high-performance ADC, without prior amplification and filtering. The ADC should then offer a high resolution with noise shaping and possibly auto-ranging capabilities [19]. The ADC should also be able to subtract an offset or artifacts from the input to maximize the resolution on the useful signal [138,139]. Those structures are particularly useful in multi-channel neural recording applications where silicon area must be minimized. For VENG signal acquisition, the low signal amplitude and the required rejection EMG interference lead to stringent specifications on the operations prior to digitization, such as true tripole summation and accurate filtering. Therefore, ADC-direct architectures are not studied in this work.

1.3 Signal Processing: Seizure Detection Algorithms

The acquisition circuits designed in this work are intended for the recording of VENG signals, which are then be used for seizure detection in a closed-loop VNS system. Detecting seizures is a signal processing task that requires advanced techniques. An understanding of the seizure detection algorithm is therefore necessary to validate the signal acquisition circuits for that specific purpose. If the signal processing algorithm used in the system is well defined, a high-level cross-domain optimization can be performed, combining design variables from the front-end and from the signal processing algorithm. This approach is implemented for ECG-based arrhythmia classification in [140], with the objectives of maximizing classification accuracy while minimizing system power consumption.

The detection of seizures consists in a binary classification between seizure and non-seizure events. Detecting event from the EEG in batch processing is widely used in clinical settings for multiple epilepsy-related tasks such as diagnosis, seizure documentation or the evaluation of the patient's response to medication [141]. Nowadays, the detection is still

generally performed manually by neurophysiologists who visually examine the signals. That task can be long and difficult, and automated seizure detection is therefore actively researched [142]. In the context of closed-loop neuromodulation triggered by epileptic seizures, events must be detected automatically and within a short time delay. The maximum detection delay for good therapeutic effect in closed-loop VNS is unknown so far. However, [91] studies the efficacy of cardiac-based seizure detection with the AspireSR device, and shows that seizures can be stopped when detecting them with a latency up to 35 s. Nevertheless, seizures are shorter if the detection delay is lower, which is beneficial for the patient's health and safety. Seizure detection algorithms should therefore be designed to minimize that delay. In [143], it is shown that EEG-based seizure detection can be performed with delays inferior to 1 s. Since the field of VENG-based seizure detection is narrow, EEG and iEEG-based methods are first reviewed in the next section.

1.3.1 EEG and iEEG-Based Seizure Detection

The field of automated EEG-based seizure detection is spread over the engineering and neuroscience domains and the reported accuracy metrics are often inconsistent, complicating the comparison of new algorithms. Recently, a detailed evaluation framework was proposed in [144]. It suggests several open-source datasets to test the algorithms, the evaluation methodology and the performance metrics that should be reported.

The different categories of seizure detection algorithms are reviewed in [141, 142, 145, 146]. Algorithms can usually be split into two consecutive operations. First, features are extracted from the signal and artifacts are rejected. Second, event classification is performed. Fig. 1.20 shows the main techniques presented in this section. Many state-of-the-art algorithms use combinations of multiple methods for accurate seizure detection.

The EEG is usually measured with a multi-channel setup to have a high spatial resolution. However, the seizure focus in some cases localized in specific brain regions, such that those events are only visible through a limited number of channels. Differently, generalized seizures are visible from a large brain region, limiting the benefits of the large number of channels. To reduce the signal spatial dimensionality and redundancy, principal components analysis is often used [147]. The same type of analysis can be applied to tackle the time-domain scarcity in EEG signals [148]. Inde-

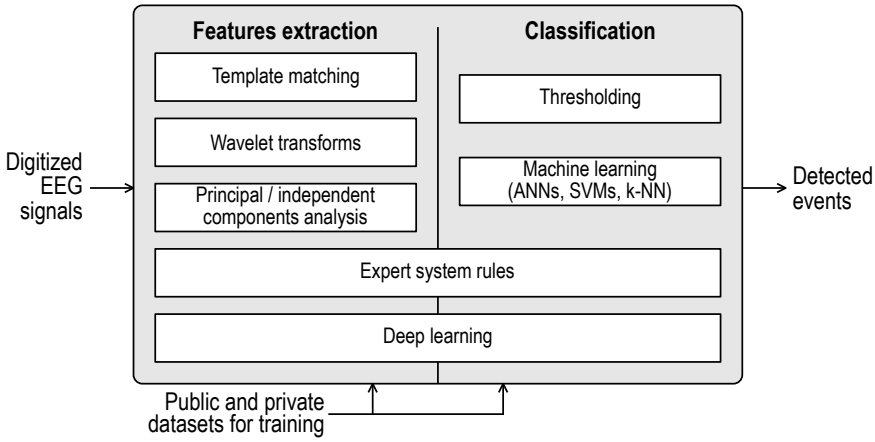


Fig. 1.20 Illustration of algorithm techniques for EEG-based seizure detection, separated in features extraction and classification methods.

pendent components analysis is another technique used to differentiate between motion artifacts and spikes from multi-channel recordings [142,149]. For feature extraction, wavelet transforms are the natural choice to analyze both the division of EEG activity into different frequency bands, and the temporal variations due to seizures. Wavelet transforms are used in each band to extract features such as minimum, maximum, range, mean, median, standard deviation and entropy [150]. Alternatively, seizures can be identified in the EEG by the appearance of high-amplitude spikes. The spike frequency and amplitude indicate the seizure stage. Computing the correlation between the EEG and a spike template allows to identify the spikes, implementing template matching. The spike templates can be derived from observations on the signal to adapt the algorithm to characteristics of the patient and of the recording setup. Finally, expert system rules designate the set of techniques that mimic the methodologies employed by neurophysiologists to identify seizures. For instance, it can detect spikes based on hard-coded amplitude, duration, and sharpness parameters. Those techniques are often less accurate than the others and are sensitive to inter-patient variability.

For the classification of seizures events from pre-extracted features, a threshold is often applied for computational efficiency [141, 151]. That threshold can for instance be based on the frequency of detected spikes or on a statistical metric computed on the signal in a specific EEG band. The

threshold value is either obtained from expert knowledge or inferred from observations on a dataset. For more advanced classification and robustness to inter-patient variability, machine learning (ML) techniques are widely used and benefit from the large number of publicly available epileptic EEG data, such as the CHB-MIT Scalp EEG Database [152]. ML techniques include artificial neural networks (ANNs) with good robustness, support vector machines (SVMs) with high accuracy, and k-nearest neighbor (k-NN) with good explainability. The choice of a specific technique should be done based on desired accuracy, training dataset and available computing resources. Finally, if a large dataset is available for training and the computing resources are not limiting, a deep learning approach can be chosen to detect seizure events directly from the EEG signal, without prior feature extraction. More details and comparisons of deep learning methods for seizure detection can be found in [145].

EEG can only access electrical activity on the surface of the scalp, which is composed of low-frequency signals representing a large neuronal population. iEEG, on the other hand, encompasses recordings with various levels of invasiveness and specificity. Highly invasive iEEG electrodes can record local field potentials (LFPs) (i.e., synaptic processing within a brain region at centimeter scale) and APs (i.e., neural activity travelling through a nerve). In [153], an LFP-based seizure detection framework is proposed. It works by decomposing the LFP signals into different frequency bands up to 250 Hz and extracting statistical metrics in each band. An SVM classifier is then used to detect the seizures. A high-accuracy neural network with 10-kB model parameters is also presented in [154] to detect seizures from iEEG data without any prior feature extraction.

1.3.2 VENG-based Seizure Detection

VENG experiments are scarcer in the literature and no dataset is publicly available, making the development and validation of high-accuracy algorithms more difficult. More specifically, no large ML models can be trained given the low amount of subjects in each experiment.

In [22], the VENG is recorded on rat subjects during seizures induced with PTZ. A cardiac-related VENG profile is then derived, representing the evolution of the VENG power around each heart beat. In that experiment, the analysis of the cardiac-related VENG profile leads to a perfect seizure detection on all rats with no false positive.

[21] studies acute VENG experiments on rats with kainic acid-induced seizures. That rat model mimics human temporal lobe epilepsy and, contrary to PTZ, does not induce hyperexcitability, making seizures harder to detect. The proposed method for seizure detection consists in analyzing VENG bursts synchronized with respiration. Abrupt losses of rhythmicity in the VENG bursts are then used as seizure markers. The experiments include 20 recorded seizures but show that, despite algorithm optimizations, no ictal VENG modifications can be observed in 7 of those seizures. This could be due to a limitation of the kainic acid model, to limitations in the chosen detection mode, or to the absence of VENG seizure markers for some types of seizures.

Experimental VENG recording of acute PTZ-induced seizures is described in [23] and automated seizure detection algorithms based on those recordings are presented in [92, 94, 155]. Contrary to the previously described experiments, those algorithms detect seizures by analyzing each AP in the VENG signal. It works by first detecting those APs, then using variations in their frequency and amplitude to detect seizures, as represented in Fig. 1.21.

The signal is first band-pass filtered with a [0.3-3.0] kHz bandwidth to observe the APs. Then, a template matching algorithm is used to detect APs in the signal. It works by computing the normalized cross-correlation (NCC) between the signal and an AP template in a 1.8-ms sliding window. If the NCC is above a certain threshold (i.e., 80%), a spike is detected. If the spike amplitude is too low compared to the RMS value of the signal, the spike is considered to be noise and is discarded. If it is too high, it is associated with artifacts and discarded as well. The AP templates can either be generic shapes or derived from patient-specific observations. In [94], a first round of AP detection is performed with generic templates. Then, k-means clustering is performed on the detected APs, and the cluster centroids are used as new AP templates for a second round of detection. This technique allows to adapt the AP detection to interpatient and intrapatient variations in AP shapes [156]. The features extracted from the AP detection are the amplitude and time location of each AP. When averaged over a certain time window, those give an indication of the vagus nerve firing rate and of the mean detected AP amplitude.

The second step in the workflow consists in detecting sharp variations in those two features with two connected sliding windows. The amplitude and firing rate variations are then normalized to baseline and combined in a single time-dependent metric. A two-step threshold is applied on that

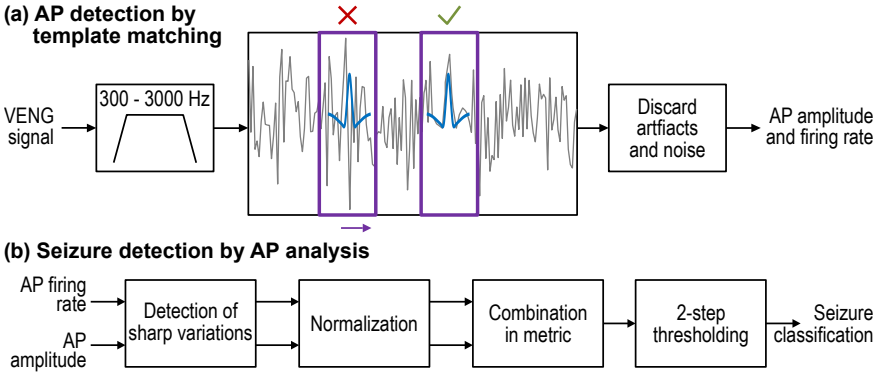


Fig. 1.21 Workflow of the seizure detection algorithm based on AP detection in the VENG signal. (a) Workflow for AP detection, (b) Workflow for seizure detection based on detected APs.

metric: to detect a seizure event, the metric should be kept above a limit value for a certain amount of time. In [92], different algorithm parameters are optimized and a leave-one-out training is used to define the thresholds. The proposed algorithm yields a perfect classification of the 6 seizure events in the experiment.

It should however be noted that the experiments were performed on anaesthetized rats, thus resulting in a low amount of interference. In [92], motion and muscle artifacts were still removed from the raw signal using a wavelet transform. However, in [155], that process was omitted and a perfect classification was still possible on the same VENG data thanks to a true-tripole AFE configuration and to the robustness of the AP detection algorithm. In addition, PTZ induces generalized tonic-clonic seizures that are easier to detect than other types of ictal events [146]. Testing the algorithm on other seizure types in the presence of artifacts is necessary to assess its robustness. Another limitation of the presented experiments is the ideal signal acquisition and processing setups. For signal acquisition, off-the-shelf analog components were used without any strict power limitation, reaching an IRN of 0.5 μV_{RMS} and a sampling frequency of 80 kHz. As discussed in Section 1.2, the performance of the target AFE working within a µW-range power budget would be lower, affecting the SNR and the overall quality of the signal. Similarly, the implementation of the AP detection algorithm proposed in [94] is resource-intensive and needs multiple runs on the same data, making it impossible to run in real time at low

power consumption. Modifications to the algorithm are then necessary, possibly impacting its accuracy. In this thesis, we use the VENG seizure detection algorithm from [92, 94] to validate our proposed front-ends, and to optimize the specifications of the front-end to reach both high detection accuracy and low power consumption.

1.4 Summary

This chapter explored the applicative context of this work, presenting state-of-the-art considerations and adapting them to the case of VENG recording.

To motivate the choice of the application targeted in this thesis, treatment options in drug-resistant epilepsy were presented. Closed-loop VNS was identified as a potentially low-risk medium-gain neuromodulation technique, and VENG-based seizure detection was selected for its low invasiveness and limited dual use potential.

Benefiting from a solid knowledge of the target application, we identified several challenges specific to VENG recording, such as the ultra-low power budget for the front-end (10-15 µW), the low signal amplitude (10-30 μV_{PP}), the large bandwidth (0.3-10 kHz), and the presence of EMG interference and stimulation artifacts. To tackle those challenges, we identified several major AFE design specifications. Due to the low signal amplitude and large bandwidth, noise was singled out as a bottleneck in the front-end. The NEF and PEF metrics were presented to quantify circuit performance in terms of noise and power consumption. Rejecting EMG interference was identified as another major challenge, whereas blanking was presented as a simple solution to stimulation artifacts. Contrary to ECG and EEG recording systems, VENG front-ends do not require MΩ-level input impedances since the series impedance of the electrode is estimated to be around 1.5 kΩ.

Different circuit-level techniques and implementations were presented to achieve high performance and to tackle the aforementioned major challenges. Table 1.3 summarizes the identified signal and system specificities, the related front-end specifications, and the circuit design techniques that were discussed in this chapter. For the attenuation of EMG interference, high-pass filtering before any amplification is necessary. The HPF must therefore be included in noise and power calculations. For reject-

ing in-band interference, a tripolar configuration is necessary, benefiting from the linearization property of the cuff electrode. QT and TT configuration are possible, and one advantage of the TT is the possibility to adapt to cuff asymmetry. To minimize the intrinsic noise of the front-end, different LNA topologies were presented. First, architectures maximizing the equivalent transconductance of the differential pair were presented, including weak-inversion differential pairs, current-reuse topologies, and stacked amplifiers. Second, switched-capacitors amplifiers were also presented, although those are not studied in this thesis due to non-idealities in those circuits. To mitigate flicker noise in the front-end circuits, chopping is not used in this work due to a relatively lower flicker noise contribution compared to sub-kHz applications. We also analyzed different types of ADCs for digitization within an ultra-low power budget and singled out SAR ADCs with custom DAC capacitances as promising architectures.

Finally, our understanding of the VENG application was enhanced with a description of signal processing methods to detect seizures from the VENG signal. We presented a VENG-specific algorithm that works by identifying APs in the signal through template matching, then proceeding to the classification by detecting sharp variations in the features of the detected APs.

Table 1.3 Summary of discussed VENG specificities and the associated circuit specifications and techniques.

Signal and system specificities	Front-end specifications	Analog circuit techniques
Signal amplitude 10-30 μV_{PP}	Low-noise IA	Chopping, **Weak inversion***, **Current reuse***, Stacking, Switched-capacitor amplifiers
Power budget 10-15 µW	Low-power IA	
	Low-power ADC	ΣΔ, **SAR***, **Custom capacitors***, Event-driven operation
Large-amplitude interference	Rejection of stimulation artifacts	Blanking
	Rejection of out-of-band EMG	**Input high-pass filtering*** (passive, active, DSL)
	Rejection of in-band EMG	Tripolar configuration (quasi tripole, **true tripole***)
Bandwidth [0.3-10] kHz	**Conventional low-power analog filtering***	
Signal composed of APs	**Validation with AP waveforms***	

* Analyzed and implemented in this thesis.

2

Optimizing the Noise-Power Trade-Off in Biomedical LNAs

NOISE from the signal acquisition circuitry is often a major bottleneck in biopotential analog front-ends (AFEs) due to the low amplitude of the input signals. The low-noise amplifier (LNA) placed at the input of the front-end is the major source of input-referred noise (IRN). Reducing its noise level typically comes at the price of higher power consumption and/or larger silicon area, which can be out of specifications depending on the target application. In addition, biopotential acquisition may also require the filtering of high-amplitude out-of-band interference, making it more difficult to implement low-noise design techniques. Fig. 2.1 illustrates a biomedical sensing system including an AFE with an input high-pass filter (HPF) and an LNA. Those two blocks are identified as bottlenecks in terms of power consumption, noise, and silicon area.

A wide range of LNA topologies and design techniques exist, as introduced in Chapter 1. Topology selection is usually done based on prior experience or on performance reported in the literature. However, to determine how a specific amplifier performs in a given set of application-driven

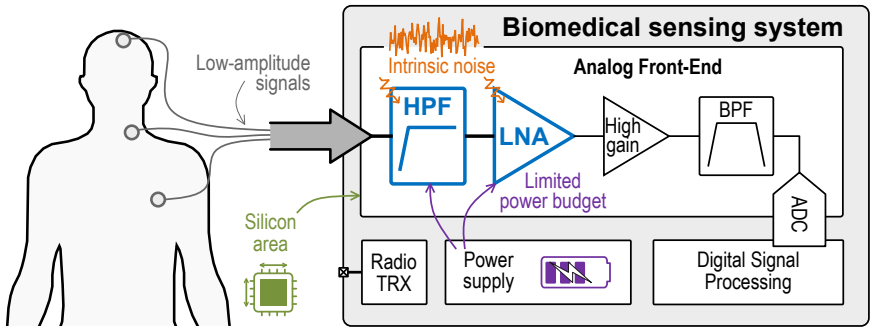


Fig. 2.1 Illustration of a low-power biomedical sensing system including an AFE. The HPF and LNA are bottlenecks in terms of noise, power consumption, and area. The electrodes on different parts of the human body illustrate the various applications that require low-noise AFEs.

specifications, the circuit must be simulated in the target CMOS technology and its sizing must be optimized using expert knowledge and/or automatic optimization algorithms. Comparing topologies based on their noise-power-area performance thus requires time, expertise, and access to analog design environments and optimization routines. The work presented in the first part of this chapter aims to answer the following research question:

> *"How can we estimate the optimal noise-power-area performance of a bio-amplifier with a limited number of numerical simulations?"*

To do so, a semi-analytical methodology is introduced in this chapter to quantify the noise-power-area trade-off in bio-amplifiers. It is based on a limited number of technology-specific parameters that can be extracted from simulations, and it is portable from one amplifier topology to another. The proposed methodology has different purposes: (i) providing a quick estimation of the optimal performance achievable with a given topology, (ii) easily comparing the noise performance of different topologies, and (iii) giving guidelines for the optimal sizing of the transistors and passive components in the amplifiers. In this chapter, the proposed semi-analytical methodology is presented and applied on a current reuse (CR) LNA optimized for the vagus nerve electroneurogram (VENG) bandwidth as a case study. Additionally, an input HPF is included in the discussions to attenuate out-of-band interference. To evaluate the proposed methodology, the performance of the CR LNA is derived analytically, and the results are

compared to numerical optimizations. The optimal sizing of each component in the amplifier is also discussed.

In the second part of this chapter, the previously described methodology is leveraged to propose an innovative LNA topology designed specifically for the acquisition of VENG signals. This part addresses the following research question:

"How can we innovate on the HPF and LNA topologies to reach a low noise efficiency factor within the specifications of the VENG application?"

Compared to other biopotentials such as electroencephalogram (EEG) or electrocardiogram (ECG), the main specificities of VENG signals introduced in Chapter 1 that impact the LNA design are the larger bandwidth, a lower electrode impedance, and the presence of high-amplitude electromyogram (EMG) artifacts. First, the larger bandwidth (i.e., kHz range) increases the integrated noise, strengthening the need for low-noise topologies. It also reduces the relative importance of flicker noise, such that a low noise efficiency factor (NEF) can be achieved without chopping. Second, the implanted cuff electrode used for VENG sensing benefits from a significantly lower series impedance than skin-surface wet or dry electrodes usually used for ECG and EEG. Third, the presence of mV-range EMG artifacts drives the need for an HPF. To avoid saturation due to the artifacts, the filter should be placed upstream of the first amplifier. The design of the LNA is thus inseparable from the HPF. The latter can be implemented with off-chip RC components, but the noise from resistors may degrade the LNA's noise performance. The novel LNA topology presented in this chapter utilizes the well-controlled input impedance of a common-gate (CG) amplifier to replace the off-chip resistors, eliminating the noise from those components. The proposed LNA also features CR to achieve a competitive noise-power trade-off. In this chapter, the CG amplifier topology is presented and its optimal performance is computed analytically. The results are compared to numerical optimizations, confirming the applicability of the semi-analytical methodology on a different LNA topology. A 22-nm FD-SOI prototype of the CG LNA is finally presented and characterized, demonstrating state-of-the-art performance within the constraints of VENG signal acquisition.

This chapter is organized as follows. First, Section 2.1 introduces the noise-power-area trade-offs in bio-amplifiers. Second, Section 2.2 presents the proposed methodology. Next, the case study on the CR LNA is detailed in Section 2.3. The innovative CG LNA topology is presented in Section 2.4,

and the measurements of the prototype chip are shown in Section 2.5. Finally, Section 2.6 concludes this chapter.

2.1 Noise-Power-Area Trade-Offs in Biomedical Amplifiers

The first part of this chapter proposes a methodology to quantify the noise-power-area trade-off in biomedical amplifiers. The novelties of this methodology come in three different goals linked to noise computation, such as illustrated in Fig. 2.2. First, the relationship between the thermal noise power spectral density (PSD) and the current consumption is often discussed in the literature when deriving the input-referred thermal noise of an amplifier [9, 15, 18, 112]. The NEF, introduced in Section 1.2.3, is commonly used to characterize this trade-off [112]. This work proposes to use bias-dependent noise models to enhance the accuracy of the estimation of the thermal noise PSD with regards to current consumption, and to extract design guidelines for optimal performance. The dependence of the noise models on the inversion level of the devices can indeed lead to significant insights for the sizing and biasing of the transistors. Second, once the IRN PSD is known, it is necessary to determine over which bandwidth the PSD must be integrated to compute the total noise power. These integration bounds are often computed by means of the equivalent noise bandwidth (ENBW), based on the upper bound of the useful signal bandwidth. However, many biopotential recording applications such as the VENG also require an attenuation of low-frequency interference and thus include high-pass filtering of the useful signal. To correctly compute the noise referred to the input of the HPF, a formalism must be developed to determine the ENBW in those cases. Finally, the trade-off between flicker noise and area is well known at device level, since the flicker noise is often modeled as inversely proportional to the gate area of the MOSFET. Thus, quantifying the relationship between area and flicker noise at circuit level can lead to an estimation of the required silicon area for a given flicker IRN level, and vice-versa. The impact of limited area on the transistors biasing is also discussed in this chapter. Combining these three contributions allows to fully quantify the interconnections between input-referred noise, current consumption and required area.

The proposed methodology can be used for any biopotential acquisition application where the noise-power-area trade-off is a critical fig-

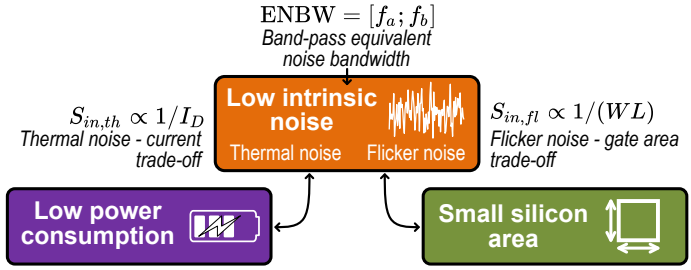


Fig. 2.2 Illustration of the interconnections between current consumption, gate area and input-referred noise. The IRN is computed from the thermal noise PSD (dependent on current consumption) and the flicker noise PSD (dependent on the total gate area). Those PSDs are then integrated on the frequency range given by the ENBW.

ure of merit. In this section, the methodology is illustrated by considering two different biopotential sensing applications: ECG and VENG. The methodology is later validated on a CR amplifier topology optimized for the VENG application. Table 2.1 summarizes the electrode and signal characteristics for both ECG and VENG systems. The noise and bandwidth specifications originate from previous works on ECG [8, 11] and VENG [23, 25] signal acquisition, whereas the signal amplitude depends on the electrode used [23]. The IRN values indicated represent what can be typically achieved in a power-limited system. Given the smaller bandwidth in the ECG case, the noise is lower. The target signal-to-noise ratio (SNR) for each application depends on the digital processing tasks operated on the signal. Heart rate extraction can be performed on noisy ECG signals, while arrhythmia detection requires analyzes of the shape of the QRS complexes and thus necessitates high SNR [8]. The large differences in bandwidth calls for different trade-offs, which enriches and generalizes the discussion of the proposed methodology. Low-noise operation is required in both applications for high-precision signal processing. In the case of ECG signals, the low bandwidth typically makes flicker noise the major noise source whereas for VENG signals with a higher bandwidth, flicker and thermal noise sources can both be dominant, depending on the amplifier design. In this chapter, the impact of flicker noise is discussed for both applications. As the studied circuits are optimized for biomedical applications working in or on the human body, a temperature $T = 37°\text{C}$ is assumed for the numerical results of the presented methodology. In addition to the different applications and to show that the methodology works

Table 2.1 Parameters of the considered applications.

	ECG	VENG
Signal amplitude	1 mV	20 µV
Useful bandwidth	[1 - 250] Hz	[0.3 - 10] kHz
Typical IRN level	$< 1\ \mu V_{RMS}$	μV_{RMS} range
Considered electrode type	Surface	Cuff

with a wide variety of devices, this chapter considers two different CMOS technologies: core transistors in 65-nm bulk CMOS, and IO devices in 22-nm FD-SOI. These choices of transistor types are guided by the fact that 65-nm core devices have better thermal noise performance than the IO devices in the same node, while the opposite is true for the 22-nm node. Detailed technology curves for both nodes are shown Appendix A. No gate leakage effects were observed with either core or IO transistors, despite the thin gate oxide in the case of core devices. Many biomedical AFEs are implemented in older CMOS nodes such as 0.18 µm [9, 12, 113]. In this work, more recent nodes are selected as the sensing system-on-chip for closed-loop vagus nerve stimulation requires fast and low-power digital signal processing functions.

2.2 A Semi-Analytical Noise Quantification Methodology

Fig. 2.3 illustrates the proposed methodology used to quantify the noise-current-area trade-off of biomedical amplifiers. The starting point of the methodology is divided into three different axes. First, the technology node and transistor flavors are selected. Bias-dependent noise models are extracted from simulations of those components. In the second axis, the bioamplifier topology is defined and its small-signal model in the signal bandwidth is computed based on conventional methods. In the third axis, the useful signal bandwidth is defined based on the target application and the ENBW is derived. From the amplifier's small-signal representation and the bias-dependent noise models of the devices, the thermal and flicker IRN PSDs are computed analytically. Thanks to the analytical expressions representing the thermal and flicker IRN, the sizing of the amplifier is optimized through the inversion level of the transistors and the

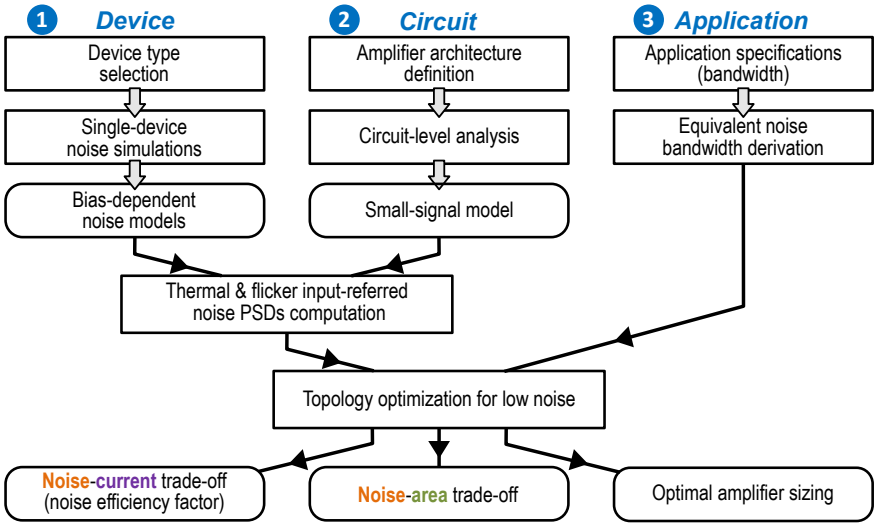


Fig. 2.3 Flow chart illustrating the proposed methodology with its three axes (device, circuit and application), and its outputs.

(g_m/I_D) methodology [157]. The impact of other types of devices such as resistors is also quantified, completing the analytical expressions representing the noise performance of the amplifier. Next, those analytical results are used to optimize the sizing of the circuit. This process gives both the optimal performance that can be reached, and the components sizing giving that optimal performance. The minimum noise level is thus obtained as a function of the current consumption and of the required gate area. The noise-current-area trade-off is then quantified for the amplifier in a certain technology implementation. Finally, the input-referred noise power and voltage are computed from given current and area budgets. In this section, the (g_m/I_D) methodology, the device-level noise models, and the computation of the ENBW are described.

2.2.1 g_m/I_D Design Methodology

The (g_m/I_D) methodology, presented in [157] and extended to short-channel CMOS technologies in [158], is based on the ratio between the transistor transconductance g_m over its DC drain current I_D, expressed in S/A or in V^{-1}. As detailed in [159], (g_m/I_D) is an indicator of the inversion level of the transistor. This approach, widely used for transistor sizing in analog

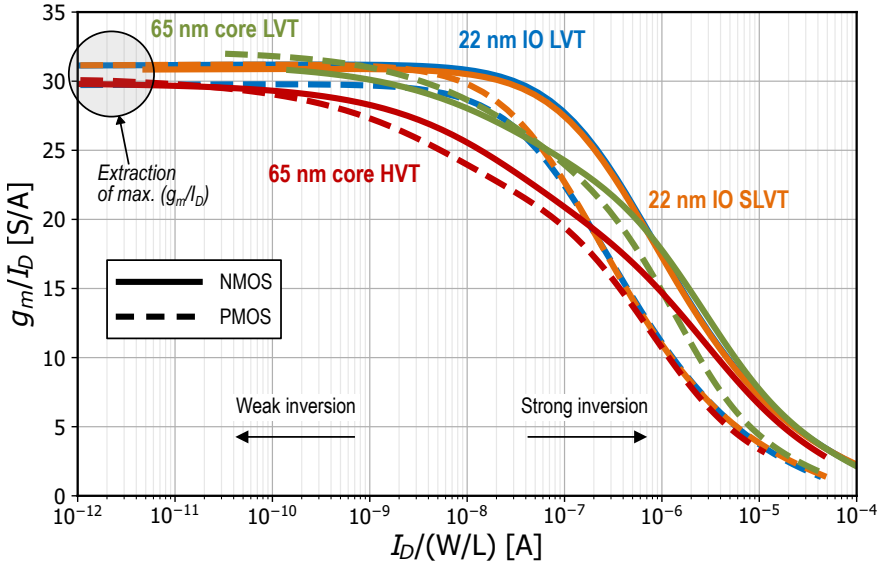


Fig. 2.4 (g_m/I_D) vs drain current normalized to the transistor aspect ratio, for N-type (solid) and P-type (dashed) MOSFETs in different nodes and threshold voltage flavors (65-nm core: LVT, HVT; 22-nm IO: LVT, SLVT). Curves extracted for $W = 100$ µm, $L = 1$ µm and $V_{DS} = 1.2$ V.

design, exploits the link between the drain current of a device normalized to its aspect ratio (W/L), and its (g_m/I_D). Fig. 2.4 depicts the (g_m/I_D)-$I_D/(W/L)$ curves for N and P-type devices in different threshold voltage flavors and in both of the technology nodes used in this work. This study is conducted for low-V_t (LVT) and super-low V_t (SLVT) IO transistors in 22 nm, and low-V_t (LVT) and high-V_t (HVT) core devices in 65 nm. The curves are only shown for $W = 100$ µm and $L = 1$ µm, but the dimensions do not significantly impact the results in case of long-channel devices. Short-channel effects are observed for lengths below 200 nm and 100 nm in 65-nm core and 22-nm IO devices, respectively. However, in analog amplifiers, transistor lengths larger than the minimum length of the technology are usually preferred to improve the matching of the devices, reduce the flicker noise, avoid short-channel effects, and maximize the intrinsic gain of the MOSFETs. Therefore, gate lengths around 1 µm are assumed in this work, neglecting most short-channel effects. Indeed, it is shown in this chapter that, in the absence of strict area constraints, the optimal sizing only includes lengths in the µm range. The maximum (g_m/I_D) that can

be achieved in the exponential subthreshold regime with a given transistor flavor in the absence of short-channel effects can be extracted from Fig. 2.4. As detailed in [157], it is expressed as

$$\left(\frac{g_m}{I_D}\right)_{\max} = \frac{1}{nV_T}, \tag{2.1}$$

where n is the body factor of the transistor and V_T is the thermal voltage. Hence, the $(g_m/I_D)_{\max}$ extracted from Fig. 2.4 can be used to compute the body factor of the device which is a necessary parameter for noise modeling that mostly depends on the transistor's oxide capacitance. It is however important to keep in mind that this value of the body factor is only valid in weak inversion and varies slightly with bias conditions. Additionally, Fig. 2.4 shows that there is a plateauing trend in the (g_m/I_D)-$I_D/(W/L)$ curve toward weak inversion. In this regime, it is therefore possible to vary I_D at constant dimensions by at least a decade without affecting much the (g_m/I_D) of the device. This effect is used in the rest of this chapter to sweep over different values of current while maintaining transistors in weak inversion.

2.2.2 Bias-Dependent Noise Modeling

In order to fully describe the noise-current-area trade-off in an amplifier, it is necessary to develop a model for the noise originating from each device. This section presents a model of the noise sources in resistors (thermal) and MOSFETs (thermal and flicker) that only rely upon circuit-level quantities available to the designer, upgraded with technology-dependent and bias-dependent parameters obtained from simulations.

Regarding resistors, only thermal noise is considered. It is modeled as a current source in parallel with the resistor. The noise PSD is given by

$$S_{i_R} = 4kT/R, \tag{2.2}$$

where k is Boltzmann's constant, T the absolute temperature, and R the resistance value.

Circuit designers often model the thermal current noise in MOSFET channels as

$$S_{i_d} = \frac{8}{3}kTg_m. \tag{2.3}$$

However, this model only holds for long-channel devices in saturation and

in the strong inversion regime [118, 160]. For a more complete model over different levels of inversion, we propose to use

$$S_{i_d} = 4kT\gamma g_m, \tag{2.4}$$

where γ is a technology-dependent and bias-dependent parameter. This model is valid for transistors in the saturation regime [118], which is often the case of transistors used in amplifiers. In this work, we thus use the model from (2.4) and consider variations of γ with the inversion level. To this end, MOSFETs are simulated with fixed V_{BS} and V_{DS}, sweeping V_{GS} to cover different inversion levels. The drain current and the transconductance g_m are evaluated, and the channel thermal noise PSD is obtained from NOISE AC simulations based on well-established foundry models. The γ parameter is then extracted from the noise PSD. The simulation results are shown in Fig. 2.5(a)-(b), where the γ coefficient is plotted as a function of the inversion level, quantified by the (g_m/I_D) ratio of the transistor. These curves were extracted at different transistor dimensions and at different V_{DS} (not shown), yet no significant differences could be observed. Fig. 2.5(a)-(b) shows that γ always remains between 0.25 and 1.0 for these transistors. It is generally lower in weak inversion than in strong inversion. For the 65-nm node, the γ coefficient slightly increases in very weak inversion due to body effect.

Modeling flicker noise, on the other hand, is a more complicated task since its PSD can span over multiple orders of magnitude depending on the transistor bias and dimensions, and on the frequency [161, 162]. While the flicker noise can be modeled accurately with physical equations, this work proposes to represent it with quantities easily available to the analog designer. In [162] it is shown that the flicker noise of a MOSFET can be modeled as a voltage source at its gate with a PSD given by

$$S_{v_g}(f) = \frac{\alpha}{(WL)f^{1+\xi}}, \tag{2.5}$$

where α and ξ are parameters that generally depend on the technology, bias conditions, and dimensions. ξ is expected to be close to 0 to approach the $1/f$ behavior. In this methodology, a similar approach to that of thermal noise modeling is conducted for flicker noise to estimate the curves for α and ξ. The V_{GS} of the transistor is swept in simulation while the other bias voltages are maintained constant. The flicker noise PSD is then extracted and the α and ξ coefficients are derived from the PSD. Fig. 2.5(c)-(d)

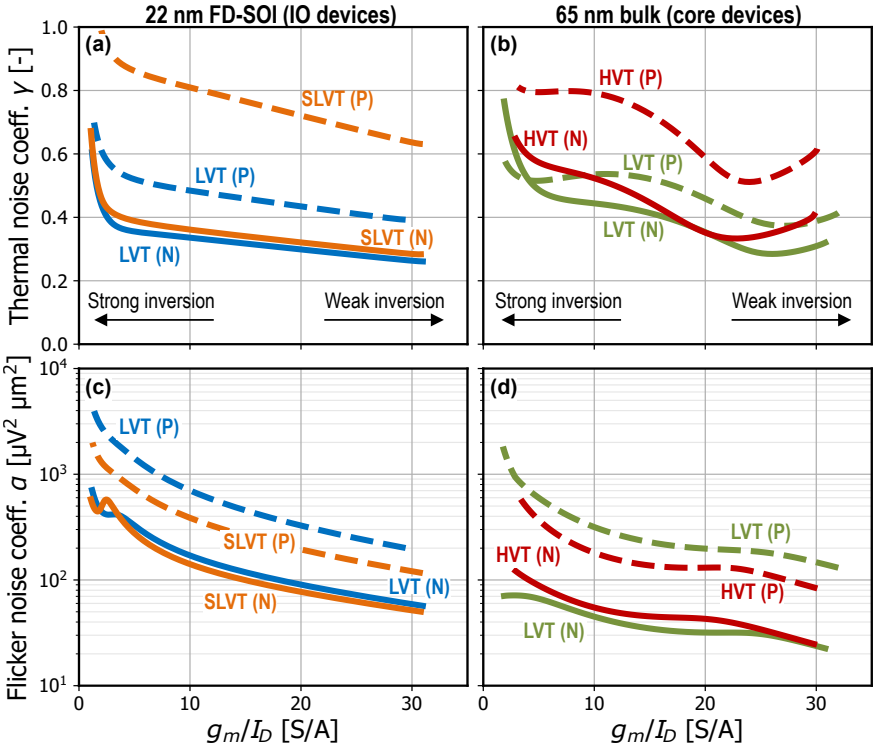


Fig. 2.5 Noise coefficients in 65-nm bulk core transistors (LVT, HVT) and 22-nm FD-SOI IO transistors (LVT, SLVT) at the device level for N-type (solid) and P-type (dashed) MOSFETs. Dependencies of the termal (a), (b) and flicker (c), (d) noise coefficients on (g_m/I_D) are shown. Curves extracted for $W = 100$ µm, $L = 1$ µm and $V_{DS} = 1.2$ V.

show the dependency of the α coefficient on (g_m/I_D), for both considered technology nodes. No significant dependency of α on W and V_{DS} is observed. However, α can decrease by a factor up to 2 when the length L is below 1 µm due to the dependency of the mobility on the gate length, such as described in [163]. These variations could be taken into account in our methodology by using different mappings for the α coefficients, depending on the gate length. However, our designs do not use lengths below 1 µm for the input transistors of high-precision amplifiers, except in case of strict area constraints. Simulations show that the flicker noise coefficient α decreases as the device goes to weak inversion, which is confirmed by [161]. For gate lengths above 1 µm, carrier number fluctuations dominate the

flicker noise, resulting in lower variations of the α coefficient with (g_m/I_D) in weak inversion [162, 164]. Fig. 2.5 also shows that P-type devices have a higher flicker noise coefficient than N-type transistors, meaning that at identical dimensions and (g_m/I_D), the gate-referred flicker noise at 1 Hz is higher in P-type transistors for the considered deep submicron technologies. This conclusion is similar to [164, 165]. Finally, the exponent ξ (not represented) is found to be constant with bias and dimensions, and to only depend on the transistor flavor, which may be a limitation of the foundry models. Its absolute value is lower than 0.2 in all studied cases.

The dependencies of the noise coefficients γ and α on (g_m/I_D), shown in Fig. 2.5, could be analytically represented by nonlinear models or look-up tables (LUTs) to accurately predict the noise at every possible (g_m/I_D) value. However, analytical nonlinear curve fitting or LUT search would complicate the models with technology-dependent parameters. Analytical developments and optimizations of low-noise circuits would then become more challenging. Moreover, low-noise amplifiers tend to contain transistors either in weak or strong inversion, avoiding the need for an accurate curve fitting over the whole range of (g_m/I_D). Instead, this methodology suggests to extract upper and lower bounds of the γ and α curves from Fig. 2.5, and to use those for circuit-level noise modeling. It should be noted that the accuracy of the proposed approach is dependent on foundry models. Effects not represented in the latter are thus also neglected in the proposed analytical models.

2.2.3 Equivalent Noise Bandwidth

The noise efficiency factor is a widely used metric to quantify the trade-off between current consumption and circuit-level thermal noise immunity. In Section 1.2 of this work, the NEF is defined as

$$\mathrm{NEF} \triangleq v_{\mathrm{in,RMS}} \sqrt{\frac{I_{\mathrm{tot}}}{4kTV_T f_H \pi/2}}, \tag{2.6}$$

where $v_{\mathrm{in,RMS}}$ is the IRN voltage, I_{tot} is the total current consumption, V_T is the thermal voltage, and f_H is the upper bound of the signal bandwidth. A lower NEF thus indicates better performance in terms of the noise-current trade-off. In this definition, the IRN is assumed to be integrated from DC to f_H. However, this assumption does not hold when the signal bandwidth also has a lower limit. This section proposes a formalism for the bandwidth

to consider in this case. Also, as the noise normalization in the definition of the NEF considers that flicker noise is negligible, the general impact of $1/f$ noise on the NEF should be discussed.

The equivalent noise bandwidth is commonly used to describe the bandwidth over which noise must be integrated to obtain the noise power. Fig. 2.6(a) represents this ENBW in the case of an amplifier with an in-band gain A and an output white noise PSD N_W, expressed in V/V and V^2/Hz, respectively. To compute the NEF, a virtual first-order low-pass filter (LPF) with cut-off frequency f_H is assumed at the amplifier output [112]. This virtual filter emulates the behavior of the subsequent elements in the signal chain. The intrinsic low-pass filtering of the amplifier is neglected in comparison with the virtual LPF at the output. Equation (2.7) computes f_b, the cut-off frequency of the rectangular filter whose integrated output power is equivalent to the noise power at the output of the virtual LPF:

$$f_b = \frac{1}{N_W}\int_0^\infty N_W \frac{1}{1+(f/f_H)^2} df = \frac{\pi}{2} f_H, \tag{2.7}$$

which is a well-known result for first-order low-pass filtering and thermal noise only. The IRN power $\overline{v_{\text{in}}^2}$ is then computed by integrating the IRN PSD from 0 to f_b, hence the $(\pi/2)f_H$ expression in (2.6).

When $1/f$ noise and input high-pass filtering are added to the signal chain, the above analysis is no longer sufficient to describe the IRN, such as shown in Fig. 2.6(b). To describe how noise affects the signal in its useful bandwidth, we propose to assume a virtual first-order band-pass filter (BPF) at the amplifier output, with cut-off frequencies $[f_L; f_H]$ where f_L is the lower limit of the signal bandwidth. The noise PSD at the output of this virtual filter becomes

$$\text{PSD}_{\text{out,filt}}(f) = N_W \left(1+\frac{f_c}{f}\right) \frac{1}{1+(f/f_H)^2} \frac{(f/f_L)^2}{1+(f/f_L)^2}, \tag{2.8}$$

where f_c is the noise corner frequency at which the thermal and flicker noise PSDs are equal. Assuming $f_H \gg f_L$, the integral of this PSD from $f = 0$ to $f = +\infty$ is equivalent to the integral of the noise PSD at the output of the amplifier from f_a to f_b, where

$$f_a = \frac{\pi}{2} f_L; \qquad f_b = \frac{\pi}{2} f_H. \tag{2.9}$$

The expression for f_a can be visualized with a non-asymptotic PSD such as

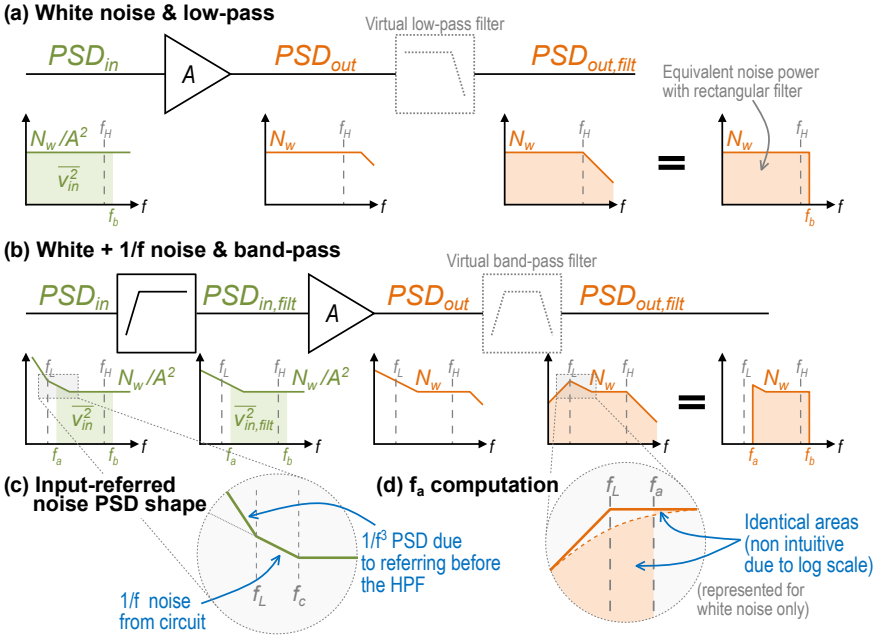


Fig. 2.6 Representation of the asymptotic noise PSDs and bandwidths with (a) white noise and low-pass filtering at f_H only and (b) additional $1/f$ noise and input high-pass filtering at f_L. A white noise PSD value of N_W is assumed at the output of the amplifier with gain A. Green-filled areas indicate the integrals to evaluate the IRN power. (c) and (d) provide details on the shape of the IRN PSD at low frequency and on the computation of f_a, respectively.

in Fig. 2.6(d), which shows that f_a is higher than f_L due to the attenuation in the signal band beyond f_L. In this figure, it is shown for white noise but the same principle holds when adding $1/f$ noise. The IRN power can then be computed by integrating the IRN PSD over the $[f_a; f_b]$ bandwidth. The shape of the IRN PSD is illustrated in Fig. 2.6(c), which shows that it tends to a $1/f^3$ shape below f_L. This work proposes to extend the definition of the NEF to the case of a BPF with the following expression:

$$\mathrm{NEF} \triangleq v_{\mathrm{in,RMS}} \sqrt{\frac{I_{\mathrm{tot}}}{4kTV_T\mathrm{ENBW}}}, \tag{2.10}$$

where the ENBW is defined with

$$\mathrm{ENBW} \triangleq f_b - f_a \tag{2.11}$$

in the case of band-pass filtering. The definition of NEF in (2.10) is used in the rest of this thesis.

With these analytical tools developed, it is possible to describe how $1/f$ noise affects the total noise power and the NEF for both ECG and VENG applications. Fig. 2.7 shows the impact of $1/f$ noise with a sweep on the noise corner frequency f_c at constant thermal noise level. The ratio of $1/f$ noise power over total noise power is shown in Fig. 2.7(a), and the impact on the NEF can be seen in Fig. 2.7(b). Three conclusions can be drawn from these graphs. First, the impact of $1/f$ noise is strongly dependent on the useful signal bandwidth. Second, even if f_c is below the signal bandwidth, $1/f$ noise can be non-negligible. Finally, if f_c lies in the signal bandwidth, the NEF is quickly degraded. These conclusions highlight the need to push the noise corner frequency f_c below the signal bandwidth by minimizing $1/f$ noise, emphasizing the importance of a quantification of the noise-area trade-off including $1/f$ noise. The strong impact of $1/f$ noise in the case of ECG signals even at relatively low f_c demonstrates the necessity of implementing $1/f$ noise mitigation techniques such as chopping in low-frequency applications. For VENG, a corner frequency close to 1 kHz can be tolerated, thus relaxing the $1/f$ noise specifications. As discussed in this chapter, chopping is therefore not indispensable in VENG AFEs.

2.3 Case Study: Current-Reuse Amplifier

This section proposes to apply the noise characterization methodology on a current reuse amplifier topology designed for use in the VENG bandwidth. Based on the analytical formulation, we obtain the optimal biasing for the circuit leading to the lowest possible NEF. Then, multiple numerical optimizations based on transistor-levels simulations are performed on the amplifier to validate the analytical results. The thermal noise is first derived analytically and validated in simulations with unlimited area. Then, the flicker noise is added to the analytical model and multiple optimizations are presented with different area constraints, highlighting the noise-area trade-off. Finally, the area requirements for low thermal noise are also discussed. A simple, well-known amplifier topology is selected for this case study for ease of generalization. The proposed methodology can however be applied to more complex topologies, as demonstrated in Section 2.4.

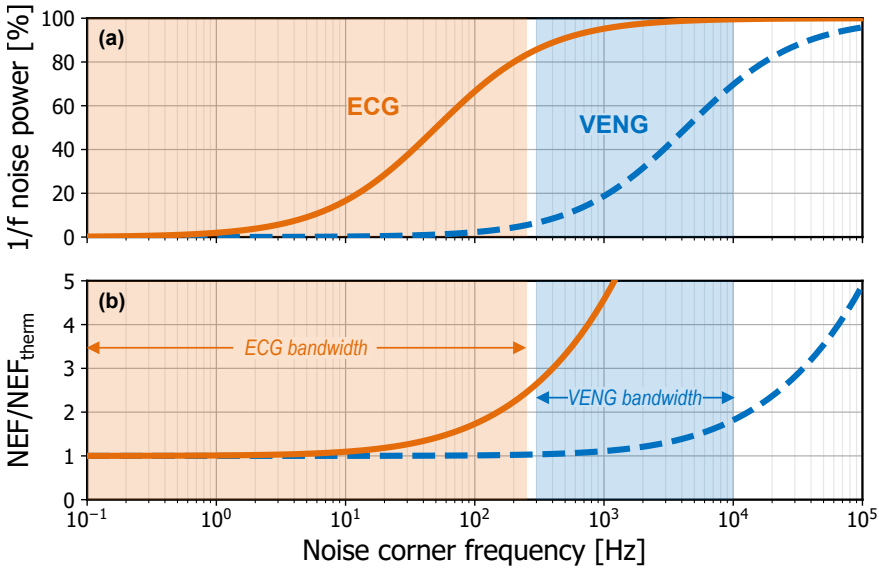


Fig. 2.7 Impact of $1/f$ noise on (a) the $1/f$ IRN power normalized to the total IRN power, and (b) the resulting NEF normalized to the NEF considering only thermal noise. Signal bandwidths are indicated by shaded areas.

2.3.1 Current-Reuse Amplifier Topology

Among the architectures achieving the lowest NEF, CR principle is often implemented [9,113]. The core idea is to duplicate the input voltage to the gates of two differential pairs, doubling the transconductance of the input branch. If the same current biases both differential pairs, that current is *used* twice, hence the name of the technique.

Fig. 2.8 shows a fully-differential amplifier implementing the CR technique. The differential input voltage is applied on the gates of M_{P1}/M_{P2} and M_{N1}/M_{N2} transistors, increasing the total transconductance G_m. Without the R_{O1}/R_{O2} resistors, the gain would be given by

$$A_v = G_m R_{out} = \frac{g_{mN} + g_{mP}}{g_{dN} + g_{dP}}. \tag{2.12}$$

The CR technique thus roughly doubles the transconductance but also decreases the output resistance, leaving the voltage gain A_v approximately unchanged compared to architectures with single current use. However, increasing G_m affects the noise transfer function. Considering a drain cur-

rent constant noise PSD of S_{i_d} for N and P transistors, the input-referred voltage noise PSD S_{in} in the amplifier bandwidth becomes

$$S_{in} = 2\frac{S_{i_d,N} + S_{i_d,P}}{(g_{mN} + g_{mP})^2}. \tag{2.13}$$

The IRN PSD is thus approximately halved compared to LNA topologies with single current use.

Coming back to the schematic of the amplifier in Fig. 2.8, the bias transistors M_T and M_B are used as matched current sources. The common-mode (CM) output voltage is sensed through the R_{O1}/R_{O2} resistors and compared to an external DC reference $V_{REF} = V_{DD}/2$. The difference is amplified by a single-stage operational transconductance amplifier (OTA) and applied on the gate of M_T. The common-mode feedback (CMFB) OTA consumes a constant current of 50 nA that is not taken into account in the following analytical and simulation results. The R_O resistors degrade the output resistance and thus the gain. With resistors in the MΩ range or lower, the in-band gain is given by

$$A_v = \frac{g_{mN} + g_{mP}}{g_{dN} + g_{dP} + 1/R_O} \approx R_O(g_{mN} + g_{mP}). \tag{2.14}$$

MΩ-range resistors can be implemented with high-density polyresistors in both considered technology nodes, benefiting from a higher linearity than MOSFET-based pseudo-resistors.

An HPF is added at the inputs of the CR amplifier. Applied to ECG or EEG applications, it would only be used to reject the electrode DC offset (EDO) and have a cut-off frequency of any value below the signal bandwidth. In the case of VENG sensing, the HPF rejects the EDO and the out-of-band EMG interference. Since the EMG has a significant amount of power at low frequencies, the HPF should have a precisely defined cut-off frequency slightly below 300 Hz to attenuate the EMG power. The off-chip HPF is composed of on-chip kΩ-range resistors R_i, and off-chip nF-range capacitors C_i. The DC voltage $V_{IN,DC}$ generated externally allows to set the input DC voltage. The presence of off-chip components is not an issue in the case of a biomedical implant with a low number of input channels. As discussed in Section 1.2, large off-chip series capacitors must be placed anyway to avoid leakage current to the nerve. Moreover, the total system volume is dominated by other bulky components (i.e., connectors and battery).

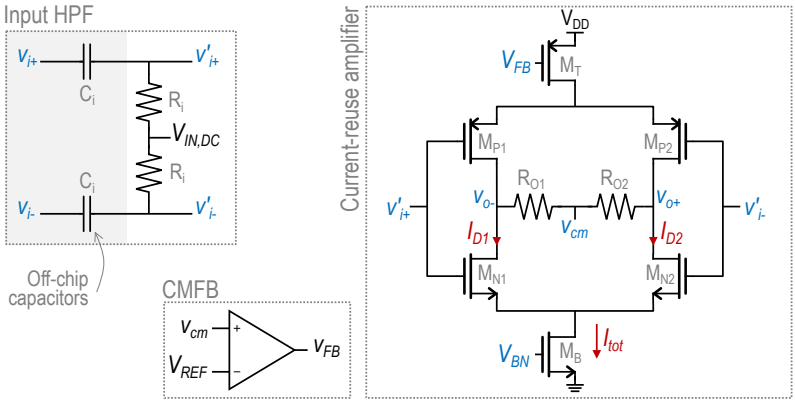


Fig. 2.8 Schematic of the considered current-reuse amplifier, including an input high-pass filter and a CMFB loop. The body terminals of N-type and P-type devices are connected to ground and V_{DD}, respectively.

The presented amplifier topology can be used in a wide range of applications. The low number of stacked transistors makes it possible to function at low supply voltage V_{DD} and no technology-specific techniques (e.g., back-biasing in FD-SOI) are used, making this amplifier easily portable from one CMOS technology to another.

2.3.2 Analytical Thermal Noise - Current Trade-Off

As shown in (2.5), flicker noise decreases with transistor gate area. If a large area is allowed for the total amplifier, flicker noise becomes negligible compared to thermal noise. This section therefore only discusses the impacts of thermal noise, whereas the trade-off between flicker noise and area is taken into account in the following sections.

The CR amplifier has different thermal noise sources that impact its output noise: (i) transistors in both differential pairs, (ii) output resistors R_O, and (iii) input resistors R_i.

i) ***Differential pairs:*** using (2.4) for the thermal noise of the transistors, their IRN PSD is the following:

$$S_{\text{in,tr}} = \frac{8kT}{(g_{mN} + g_{mP})^2}(\gamma_N g_{mN} + \gamma_P g_{mP}). \tag{2.15}$$

To emphasize the noise-current trade-off and the regime of inversion of

each transistor, (2.15) can be rewritten as

$$S_{\text{in,tr}} = \frac{16kT}{I_{\text{tot}}} \frac{\left(\gamma_N \left(\frac{g_m}{I_D}\right)_N + \gamma_P \left(\frac{g_m}{I_D}\right)_P\right)}{\left(\left(\frac{g_m}{I_D}\right)_N + \left(\frac{g_m}{I_D}\right)_P\right)^2}, \tag{2.16}$$

where I_{tot} is the total DC current drawn from the supply for the main amplifier. From (2.16), it can be seen that the transistors forming the differential pairs should be pushed towards weak inversion, maximizing both (g_m/I_D) values and minimizing the noise coefficients γ. Assuming that it is possible to reach $(g_m/I_D)_{\text{max}}$ for each transistor, (2.1) can be substituted into (2.16). The IRN PSD then becomes

$$S_{\text{in,tr}} = \frac{4kTV_T}{I_{\text{tot}}} n_{\text{eq}}^2 \left(\frac{\gamma_N}{n_N} + \frac{\gamma_P}{n_P}\right), \tag{2.17}$$

where n_N and n_P are the values of the body factor in weak inversion extracted from $(g_m/I_D)_{\text{max}}$. The equivalent body factor n_{eq}, combining characteristics from N and P devices, is given by

$$n_{\text{eq}} = \frac{2}{1/n_N + 1/n_P}. \tag{2.18}$$

Equation (2.17) highlights the noise-current trade-off of the amplifier by showing that the thermal noise PSD is inversely proportional tot the supply current. As all parameters are constant in a given technology except for I_{tot}, (2.17) provides the theoretical minimum thermal noise from the MOSFETs for a given bias current.

ii) ***Output resistors:*** the IRN PSD due to R_O can be computed as

$$S_{\text{in,R}_O} = \frac{32kT}{\left(\left(\frac{g_m}{I_D}\right)_N + \left(\frac{g_m}{I_D}\right)_P\right)^2} \frac{1}{R_O I_{\text{tot}}^2}. \tag{2.19}$$

Assuming maximum (g_m/I_D) for all transistors, (2.19) becomes

$$S_{\text{in,R}_O} = \frac{8kTV_T^2 n_{\text{eq}}^2}{R_O I_{\text{tot}}^2}. \tag{2.20}$$

iii) ***Input resistors:*** the noise from R_i is modulated by the input HPF. The frequency-dependent IRN PSD due to the thermal noise of R_i is given

by

$$S_{\text{in,R}_\text{i}}(f) = \frac{8kTR_i}{(2\pi f R_i C_i)^2}. \tag{2.21}$$

If the input HPF is only used to remove the DC offset from the electrode, such as for the ECG application, its cut-off frequency does not need to be precisely set as long as it is below the signal bandwidth. In that case, (2.21) can be written as

$$S_{\text{in,R}_\text{i}}(f) = \frac{8kT}{(2\pi f C_i)^2 R_i}. \tag{2.22}$$

Maximizing the value of R_i thus minimizes the noise. MOSFET-based pseudo-resistors can be used to reach the GΩ range. However, in other applications such as VENG signals acquisition, the input HPF is also used to attenuate out-of-band low-frequency interference. In that case, a value of the cut-off frequency is fixed by specification, with

$$R_i C_i = 1/(2\pi f_L). \tag{2.23}$$

As a result, the IRN PSD from R_i becomes

$$S_{\text{in,R}_\text{i}}(f) = 8kT \left(\frac{f_L}{f}\right)^2 R_i. \tag{2.24}$$

Two observations can be made from (2.24): (i) the IRN from R_i is modulated by the input HPF, and (ii) increasing the input resistance of the HPF results in a higher noise level. To easily combine the frequency-dependent noise PSD from R_i, the average PSD over the ENBW can be used:

$$S_{\text{in,R}_\text{i},\text{avg}} = \frac{1}{f_b - f_a} \int_{f_a}^{f_b} 8kT \left(\frac{f_L}{f}\right)^2 R_i df = \frac{32kTR_i}{\pi^2} \left(\frac{f_L}{f_H}\right). \tag{2.25}$$

The total IRN PSD $S_{\text{in,tot}}$ can then be obtained by summing the results from (2.17), (2.20) and (2.25). The NEF is computed as

$$\text{NEF} = \sqrt{S_{\text{in,tot}} \frac{I_{\text{tot}}}{4kTV_T}}, \tag{2.26}$$

which corresponds to (2.10) when $S_{\text{in,tot}}$ is constant over the whole ENBW.

Fig. 2.9 shows the analytical optimal NEF that can be achieved with the CR topology, as a function of the supply current and for different values of input resistance R_i. The technology-dependent parameters of weak-

inversion IO LVT transistors in 22-nm FD-SOI are considered and the noise coefficients γ are extracted at $(g_m/I_D)_{\max}$. When considering only MOSFET thermal noise, the NEF is constant. At low current values, the noise from the output resistors is dominant. At higher current levels, the noise from R_i dominates as it does not scale down with I_{tot}, as expressed in (2.25). It can be seen that selecting large values of R_i with the aim of maximizing the input impedance significantly degrades the NEF, showing an intrinsic limit of the RC input filter topology.

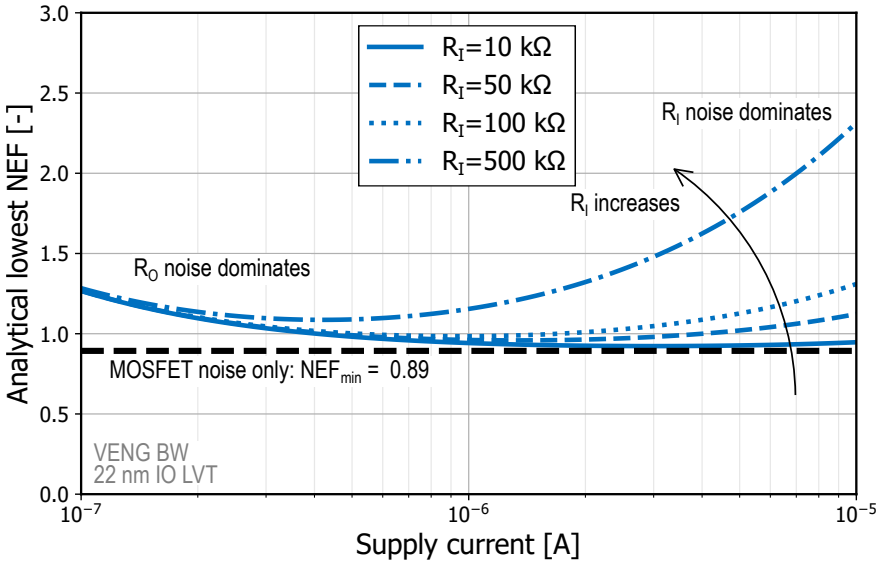


Fig. 2.9 Analytical optimal NEF that can be reached with the CR amplifier with IO LVT transistors in 22-nm FD-SOI considering thermal noise only and $R_O = 1\,\text{M}\Omega$.

2.3.3 Simulation-Based Optimizations

To challenge the analytical noise results developed in the previous section, the circuit is implemented in schematic in the 65-nm and 22-nm nodes for simulation with Cadence Spectre. The simulator is then integrated in a multiple-objective optimization routine such as the one introduced in [111]. Table 2.2 summarizes the optimization objectives, constraints and variables. The dimensions of the bias transistors and the design of the CMFB OTA are fixed. Similarly, the input HPF has constant component

values of $R_i = 50$ kΩ and $C_i = 15$ nF, giving an estimated f_L of 212 Hz. All resistors are implemented as ideal noisy resistors to focus the discussion on the noise performance of the MOSFET devices. The total area is not constrained in this optimization, allowing the algorithm to minimize the flicker noise by choosing large transistor dimensions. LVT devices are chosen in both nodes for their thermal noise performance, based on Fig. 2.5. V_{DD} is set to 1.2 V for the 65-nm implementation and $V_{DD} = 1.8$ V for the IO transistors in 22 nm. As supply voltage does not impact noise performance at first order, using different V_{DD} values between the two implementations has no influence on the results. To test all objectives and constraints, DC, AC and NOISE AC simulations are performed, in this order. At the end of each simulation, potential designs failing to respect the constraints are discarded to save computation time, as discussed in [111]. After DC simulations, the designs for which transistors are not in saturation are also rejected. To further speed up the optimization process, insights from the analytical design could be used to reduce the search space. For instance, as weak inversion is targeted for the transistors, their aspect ratio (W/L) must be maintained high. However, this first optimization targets the comparison between analytical and numerical results. Therefore, no analytical insights are used to reduce the optimization search space.

Fig. 2.10 presents the optimization results for both considered technology nodes. Analytical optima are highlighted for comparison. Those are approximately identical in the two nodes, such that the curves cannot be distinguished in the figure. While the choice of technology is known to influence the speed, power and area of digital circuits, it can be seen that the noise-current trade-off of the amplifier only presents marginal differences between 65-nm and 22-nm implementations. At high current levels, the analytical and simulation results deviate from an iso-NEF curve due to the impact of R_i noise. At lower current levels, the impact of R_O noise can also be seen although it is marginal thanks to R_O reaching 10 MΩ for those designs.

Some differences still exist between the analytical estimations and the simulation-based Pareto fronts, especially for the high-current designs in 22 nm. Those deviations can be explained by reduced (g_m/I_D) values compared to $(g_m/I_D)_{\max}$. Fig. 2.11 shows the (g_m/I_D) value of N and P transistors in the Pareto-optimal designs in 22 nm. It can first be seen that all designs have $(g_m/I_D) > 20$ V^{-1} for both transistors, meaning that N and P devices are biased in weak inversion, as anticipated analytically. Second, Fig. 2.11 shows that (g_m/I_D) decreases as the supply current in-

Table 2.2 CR amplifier optimization objectives, constraints and variables.

Objective	**Direction**
Supply Current	min.
RMS IRN	min.
Constraint	**Threshold**
In-band gain	> 35 V/V
Lower frequency limit	< 300 Hz
Upper frequency limit	> 10 kHz
Variable	**Range**
Bias current	[0.1 - 20] µA
R_O value	[0.1 - 10] MΩ
NMOS width W_N	[1.0 - 900] µm
NMOS length L_N	[0.1 - 20] µm
PMOS width W_P	[1.0 - 900] µm
PMOS length L_P	[0.1 - 20] µm

creases. This can be explained through the (g_m/I_D)-$I_D/(W/L)$ characteristic in Fig. 2.4, which shows that maintaining a constant (g_m/I_D) level can only be done at constant $I_D/(W/L)$. When the supply current increases, to maintain a high (g_m/I_D), the aspect ratio (W/L) should increase as well. As the transistor dimensions are limited during the optimization by the variable range and by the bandwidth constraints, (W/L) is actually bounded. Consequently, (g_m/I_D) decreases. Among all designs on the Pareto fronts, gate lengths are between 2.1 and 20 µm, and widths are between 39 and 900 µm. The (W/L) ratio is between 2.5 and 82 for the N-type transistors and between 19 and 110 for P-type devices.

Several conclusions can be drawn from this simulation-based optimization and its comparison with analytical optima. First, the proposed analytical models allow the accurate prediction of the optimal noise-current trade-offs that can be achieved with the CR topology. Transposing this analytical study to other topologies could be used to quickly estimate the optimal NEF achievable in a certain application, without requiring heavy implementations of simulation-based optimizations. Next, the technology-dependent parameters used in the analytical design have a marginal influ-

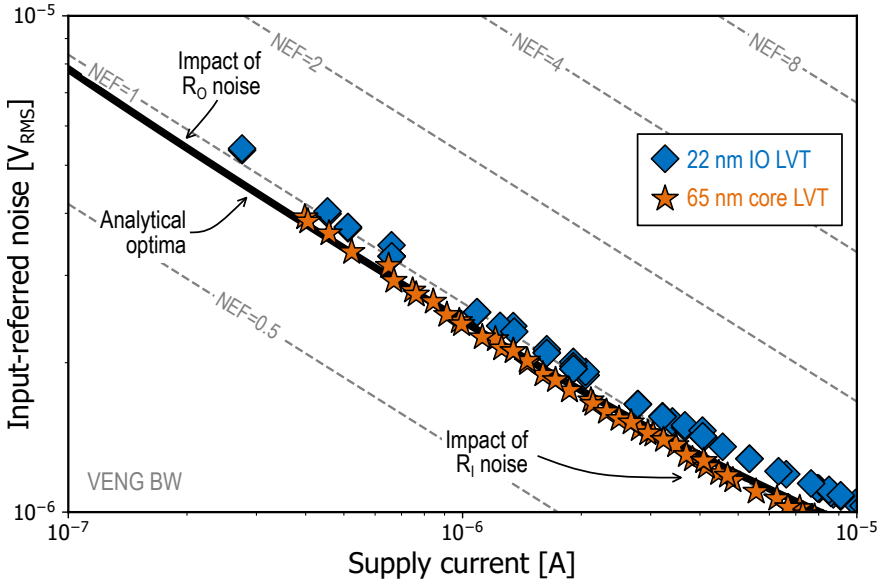


Fig. 2.10 Optimization results for the CR amplifier without any area constraint. Analytical optima are shown as solid curves. The scatter plots indicate the simulation-based Pareto fronts for the 22-nm implementation (blue diamonds) and the 65-nm one (orange stars). Iso-NEF lines are indicated with light dashes. Flicker noise is excluded from the analytical model but included in the simulations.

ence on the overall estimations. Small errors on the value of the thermal noise coefficients are thus not critical, such that raw estimations of γ can lead to accurate results. Finally, as the analytical models are shown to be accurate, analytical insights can be used to limit the search space of the optimization process if one is implemented. For instance, in the case of the CR amplifier, the (W/L) ratio of N and P transistors can initially be limited to high values to reach the weak inversion regime.

2.3.4 Analytical Flicker Noise-Area Trade-Off

Two techniques exist to reduce the flicker noise contribution: chopping and large areas. As discussed in Section 1.2.4 of this work, chopping is efficient and widely used but has a few downsides, notably an impact on input impedance and stricter bandwidth requirements for the amplifiers. While those effects can be mitigated with topology adaptations, flicker noise reduction can also be tackled by allowing a large area for the amplifier. In

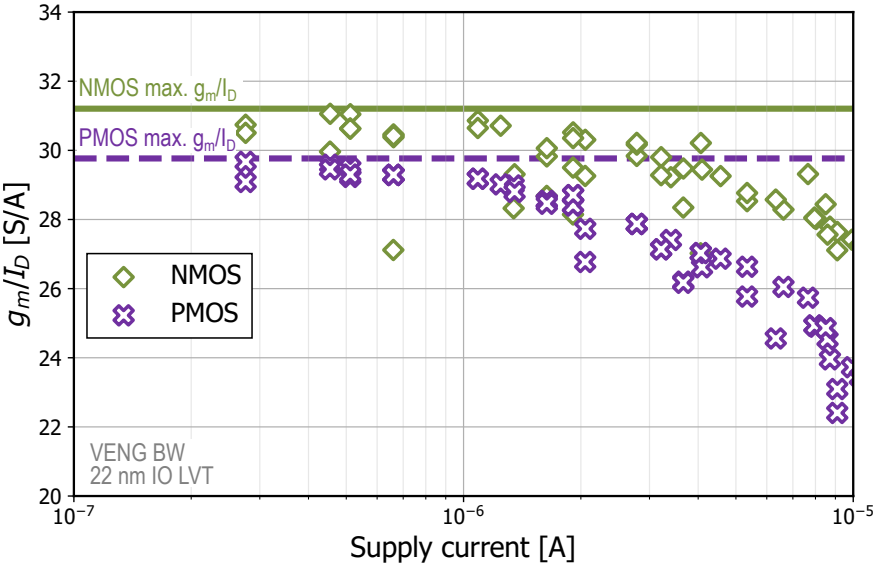


Fig. 2.11 (g_m/I_D) value for N (blue circles) and P (orange diamonds) type transistors in 22 nm from the Pareto-optimal designs. The $(g_m/I_D)_{\max}$ values, obtained from simulations of a single transistor, are indicated as dashed lines.

the VENG application, where a noise corner frequency around 1 kHz is targeted and area is not a major constraint, the latter technique is appropriate.

The results in Fig. 2.10 were obtained by minimizing the flicker noise thanks to an unconstrained area. As a result, the sum of the gate areas of the N and P transistors in the differential pairs reaches up to 70,000 µm^2 for the 22-nm results. However, chip area is not unlimited. For instance, a complete VENG AFE is presented in [25] with a silicon area of 77,000 µm^2 in a 22-nm FD-SOI technology, including a 25,000-µm^2 LNA. An ECG amplifier presented in [9] and implemented by stacking three CR amplifiers occupies a silicon area of 157,500 µm^2 in 0.18 µm CMOS. Finally, the configurable amplifier for ECG monitoring presented in [111] occupies a silicon area of 55,000 µm^2 in 65-nm CMOS. No exact comparison can be made between the gate areas computed in this thesis and the silicon areas reported in other works, but it shows that the total area is often constrained. In addition, obtaining an estimation of the area taken by analog parts early in the design phase significantly helps with chip-level floorplanning.

In the present chapter, we therefore propose to quantify the area requirements to achieve a target flicker noise level. This section derives an

analytical model for the flicker IRN of the CR amplifier. In the next sections, the analytical results are compared to simulation-based optimization results with different area constraints.

The flicker noise from the main N and P transistors is computed based on (2.5):

$$S_{\text{in,fl}}(f) = 2\frac{\left(\frac{g_m}{I_D}\right)_N^2 \frac{\alpha_N / f^{1+\xi_N}}{W_N L_N} + \left(\frac{g_m}{I_D}\right)_P^2 \frac{\alpha_P / f^{1+\xi_P}}{W_P L_P}}{\left(\left(\frac{g_m}{I_D}\right)_N + \left(\frac{g_m}{I_D}\right)_P\right)^2}. \tag{2.27}$$

No absolute optimal choice of (g_m/I_D) values stands out from that expression. However, the α parameters are lower in weak inversion. In addition, the low thermal noise design from (2.17), as well as the optimization results from Fig. 2.11, indicate that high (g_m/I_D) values should be preferred. Hence, N and P transistors are assumed to be optimally biased in weak inversion. The input-referred flicker noise PSD thus becomes:

$$S_{\text{in,fl}}(f) = \frac{n_{\text{eq}}^2}{2}\left(\frac{\alpha_N}{n_N^2 W_N L_N f^{1+\xi_N}} + \frac{\alpha_P}{n_P^2 W_P L_P f^{1+\xi_P}}\right). \tag{2.28}$$

Since the PSD is not constant, analytical optimizations should be done on the noise power $\overline{v_{\text{in,fl}}^2}$ integrated over the $[f_a; f_b]$ bandwidth as defined in (2.9). The integration yields:

$$\overline{v_{\text{in,fl}}^2} = \frac{n_{\text{eq}}^2}{2}\left(\frac{\alpha_N/\xi_N}{n_N^2 W_N L_N}\left(\frac{1}{f_a^{\xi_N}} - \frac{1}{f_b^{\xi_N}}\right) + \frac{\alpha_P/\xi_P}{n_P^2 W_P L_P}\left(\frac{1}{f_a^{\xi_P}} - \frac{1}{f_b^{\xi_P}}\right)\right), \tag{2.29}$$

provided that $\xi_{N/P} \neq 0$. The sum of the gate areas of the transistors in the differential pairs is given by

$$A_{\text{tot}} = 2\left(W_N L_N + W_P L_P\right). \tag{2.30}$$

Considering (2.29) and (2.30), it is possible to analytically optimize the area allocation between N and P transistors. It gives

$$W_N L_N = \frac{\sqrt{\frac{\beta_N}{\beta_P}}}{1+\sqrt{\frac{\beta_N}{\beta_P}}}\frac{A_{\text{tot}}}{2}; \tag{2.31}$$

and

$$W_P L_P = \frac{1}{1+\sqrt{\frac{\beta_N}{\beta_P}}} \frac{A_{\text{tot}}}{2}; \tag{2.32}$$

with β_N and β_P parameters defined as

$$\beta_{N,P} = \frac{\alpha_{N,P}/\xi_{N,P}}{n_{N,P}^2} \left(\frac{1}{f_a^{\xi_{N,P}}} - \frac{1}{f_b^{\xi_{N,P}}} \right). \tag{2.33}$$

Assuming the proposed optimal area allocation, the flicker noise power is given by

$$\overline{v_{\text{in,fl}}^2} = n_{\text{eq}}^2 \frac{\left(\sqrt{\beta_N} + \sqrt{\beta_P}\right)^2}{A_{\text{tot}}}. \tag{2.34}$$

If $\xi_{N/P} = 0$, the flicker noise power with optimal area allocation becomes

$$\overline{v_{\text{in,fl}}^2} = n_{\text{eq}}^2 \log\left(\frac{f_b}{f_a}\right) \frac{\left(\sqrt{\alpha_N}/n_N + \sqrt{\alpha_P}/n_P\right)^2}{A_{\text{tot}}}. \tag{2.35}$$

From (2.34) and (2.35), it can be observed that the flicker noise power does not depend on the bias current as long as the N and P transistors remain at constant (g_m/I_D) values. Thus, contrary to thermal noise, increasing the supply current does not result in a reduction of the flicker IRN. As a consequence, there is no flicker noise-current trade-off but rather a flicker noise-area one. On a noise-current curve, dominant flicker noise results in a constant-noise plateau with a noise value inversely proportional to the summed gate area.

2.3.5 Area-Constrained Optimizations

To challenge the previous analytical results, the CR amplifier is optimized for the VENG application in the 22-nm node with different area constraints, including only the gate area of the differential pairs. Fig. 2.12 shows the resulting Pareto fronts. The analytical flicker noise plateau is indicated for each area constraint. For the most constrained optimization with a maximum gate area of 50 µm^2, the optimizer converges to gate lengths around 0.5 µm and widths up to 60 µm, reaching both good analog performance (long-channel devices) and weak inversion (high aspect ratio). As the permitted area increases, so do L and (W/L).

For the displayed flicker noise plateaus, a comparison between analyt-

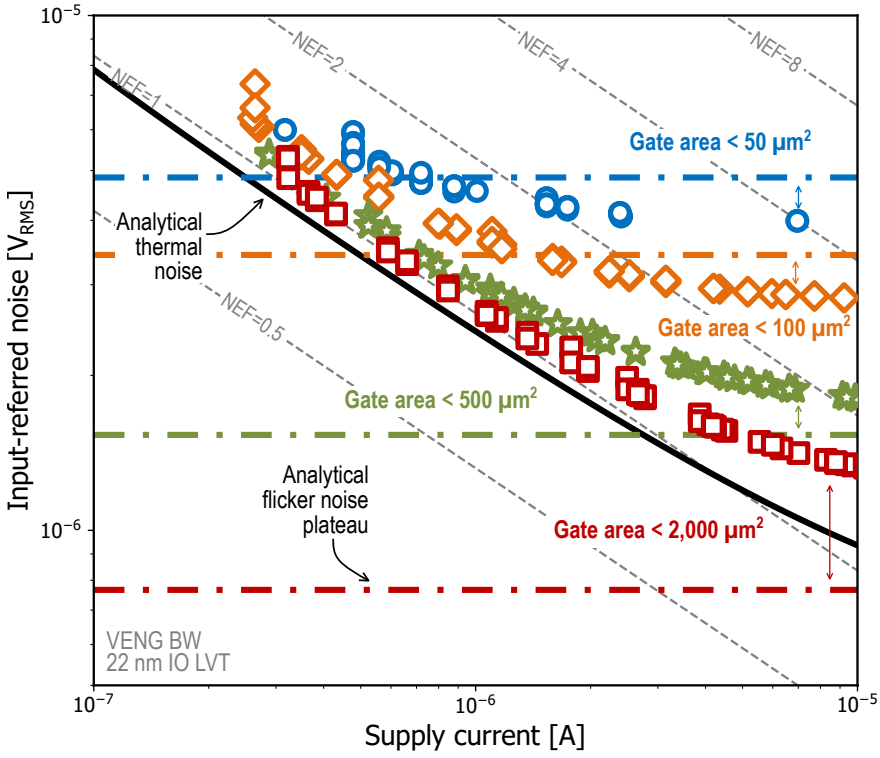


Fig. 2.12 Optimization results of the CR amplifier for different area constraints, assuming a VENG bandwidth and 22-nm FD-SOI LVT IO devices. The area indicated is the sum of the gate area of the four transistors forming the differential pairs. The analytical thermal noise, independent from any area constraint, is shown in a solid black line. For each area constraint, the analytical flicker noise plateau is indicated with a horizontal dash-dotted colored line. Iso-NEF curves are indicated as gray dashed lines.

ical and simulation results can be made. It can be seen that for the cases with small dimensions, the analytical estimation tends to over-estimate the flicker noise by up to 20%. That can be attributed to the variations of α with the gate length, as discussed in Section 2.2.2. For the optimizations with large allowed area, the flicker noise plateau is slightly under-estimated due to limited (g_m/I_D) and (W/L) values. To reduce the uncertainty, the flicker noise model could be improved with (g_m/I_D)-dependent values of α coefficients. However, such improvements would require technology-dependent curve fitting and analytical optimizations taking into account

thermal and flicker noise combined. These additional layers of complexity are in opposition to our approach that target simple models. Still, the analytical flicker noise model developed in the previous section accurately determines the order of magnitude of the flicker noise plateau. The model can also be used the other way around: for a specified flicker noise level, the minimum required gate area can be computed analytically, giving a first estimate of the minimum area required for the amplifier.

2.3.6 Analytical Thermal Noise-Area Trade-Off

Beside flicker noise, thermal noise is also impacted by a reduction in gate area. As highlighted in Fig. 2.4, there exists a plateau in the (g_m/I_D) curve that allows to sweep the normalized current at almost constant (g_m/I_D). But for the range of drain currents considered in this work, the plateau is not sufficient to keep a constant (g_m/I_D) at high current values. As a result, when the drain supply current increases, the gate area required to maintain a constant (g_m/I_D) also increases, adding a trade-off between thermal noise and gate area. Fig. 2.13 presents analytical results for this trade-off. The supply current is swept from 0.1 to 10 µA, reducing thermal noise. It is assumed that the transistors are biased at $(g_m/I_D) = 0.8\,(g_m/I_D)_{\max}$ for all values of the supply current. For different values of the gate length L identical for all transistors, the sum of the widths required to maintain $(g_m/I_D) \geq 0.8\,(g_m/I_D)_{\max}$ are shown. That sum of widths increases with the supply current, indicating that limited dimensions result in lower (g_m/I_D) and thus higher thermal noise levels.

However, for the VENG application with a bandwidth in the kHz range, the design should be optimized to make flicker noise negligible compared to thermal noise, such that no specific flicker-noise reduction techniques such as chopping need to be implemented. Fig. 2.13 also presents the sum of minimum widths required to keep the flicker noise power at 10% of the thermal noise power. As the thermal noise decreases with the supply current, the targeted flicker noise level is reduced, leading to an increase in the required gate area. It can also be seen that the sum of widths required to keep the flicker noise negligible is much higher than the sum of widths required to maintain a high (g_m/I_D) level. Under those assumptions, flicker noise thus dominates the noise-area trade-off.

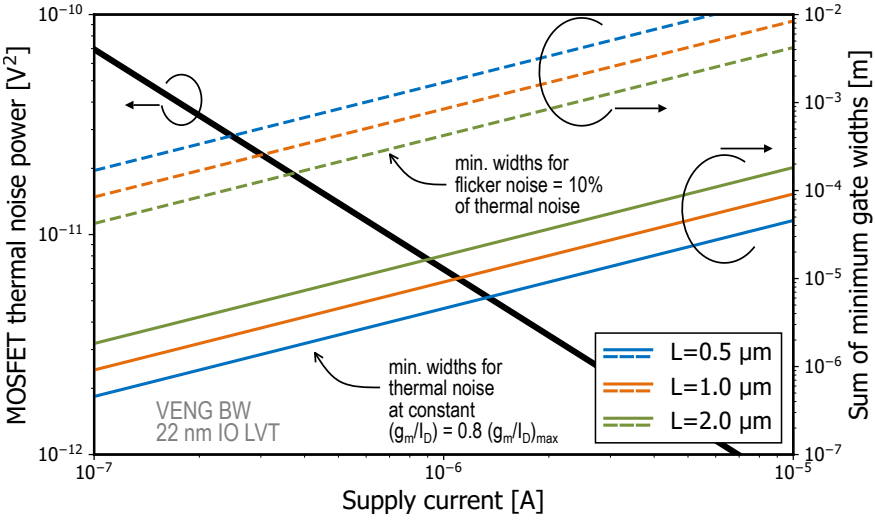


Fig. 2.13 Analytical noise-current-area trade-off for the CR amplifier designed for a VENG bandwidth with 22-nm LVT IO devices. On the left y-axis (solid black line), the evolution of the thermal noise power with the supply current, assuming N and P transistors biased at 80% of their $(g_m/I_D)_{\max}$. On the right y-axis (solid colored lines), the sum of the minimum gate widths $W_N + W_P$ to maintain the (g_m/I_D) values as the current increases. On the right y-axis (dashed colored lines), the sum of the minimum gate widths required to maintain a flicker noise power lower than 10% of the thermal noise power. The results on the right y-axis are shown for different gate lengths, assuming the same length for N and P devices.

2.3.7 Evaluation of the Proposed Methodology

The proposed analytical models for thermal and flicker noise sources can be combined to obtain a full model of the noise of an amplifier topology with a only four technology-dependent parameters for each transistor: the body factor n in weak inversion extracted from the $(g_m/I_D)_{\max}$ value, the thermal noise coefficient γ, and the flicker noise coefficients α and ξ. All parameters can be obtained from simple simulations of single devices. It should however be noted that the final noise results only have little dependence on the thermal noise coefficients. The flicker noise model has more variations due to the parameter α depending on many parameters, but approximate values of the flicker noise plateau can still be estimated. In the example of the CR amplifier, only transistors in weak inversion were characterized, such that the noise coefficients were only extracted in that regime. If the considered amplifier also uses amplifiers in strong inversion,

two values should be extracted for each noise coefficient.

To apply the proposed methodology to other amplifier topologies, the IRN PSD must be re-computed analytically. The bias-dependent noise coefficients can be reused as those do not depend on the amplifier topology, leading to quick computations of the noise-current-area trade-off. For an additional validation, we apply the proposed methodology to LNA topologies presented in published works after reverse-engineering their sizing and bias choices. The neural recording amplifier from [18] gives an analytical NEF of 3.7 according to the proposed methodology, very close to the reported NEF of 3.8 in simulations. Similarly, analytical developments on the amplifier from [111] give an NEF of 1.7 compared to the reported value of 1.93 in measurements.

2.4 A Common-Gate Low-Noise Amplifier

The previous sections have shown that the off-chip RC HPF could be a bottleneck in terms of input-referred noise. For instance, the 4-µA current-reuse amplifier design in Fig. 2.10 has a total IRN power of 1.71 μV^2, 19% of which come from the input HPF with $R_i = 50$ kΩ. In [25], the 50-kΩ off-chip resistors account for 28% of the IRN power. As the HPF IRN power is proportional to R_i, this limits the input impedance to the kΩ range and fixes a lower bound for the IRN. This section studies an alternative architecture combining input HPF and LNA to perform resistorless high-pass filtering of out-of-band interference. The proposed amplifier is studied analytically and in simulations with LVT IO devices in the 22-nm FD-SOI technology node.

2.4.1 Common-Gate Architecture

The proposed amplifier topology is shown in Fig. 2.14. The input HPF is obtained by the combination of off-chip capacitors C_i in the nF range and the impedance seen at the v_i' nodes. That impedance is dominated by the transconductance of the CG differential pair $M_{1,2}$. The filtering operation is thus achieved without any resistor, thus eliminating that source of noise. The input signal is also buffered through $M_{5,6}$ that act as DC-level shifters. A common-source differential pair $M_{3,4}$ is placed on top using the same bias current as the CG pair. The principle of CR is thus also implemented in

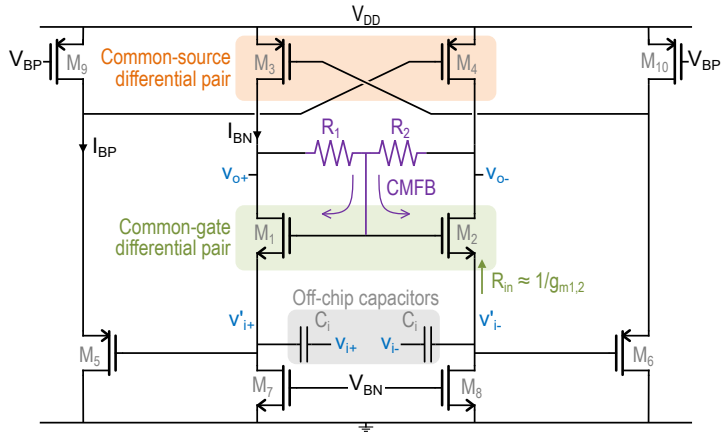


Fig. 2.14 Schematic of the proposed common-gate amplifier implementing resistorless high-pass filtering and current reuse.

this topology. Finally, resistors $R_{1,2}$ are placed at the output nodes for CM output sensing. The sensed voltage is then applied on the gates of the CG pair, providing internal CMFB without any additional circuitry. The body of the N-type (resp. P-type) devices is connected to ground (resp. V_{DD}). The bias currents I_{BN} and I_{BP} have different functions. I_{BN}, in the main branch, is used to provide gain and reduce the noise of the devices in that branch. I_{BP}, on the other hand, is mainly used to ensure the functioning of the level shifter. However, a very low I_{BP} increases the noise contribution of the level shifter. An optimum should thus be found.

To analytically describe the behavior of this CG LNA, the in-band gain is given by

$$A_{v0} = \frac{g_{m1} + g_{m3}}{g_{d1} + g_{d3} + 1/R_1} \approx R_1 \left(\left(\frac{g_m}{I_D} \right)_1 + \left(\frac{g_m}{I_D} \right)_3 \right) I_{BN}. \tag{2.36}$$

The approximation holds for R_1 in the MΩ range. The upper and lower limits of the bandwidth of the CG amplifier are given by

$$f_{L,CG} \approx \frac{(g_m/I_D)_1}{2\pi C_i} I_{BN}; \quad f_{H,CG} \approx \frac{1}{2\pi R_1 C_L}, \tag{2.37}$$

where C_L is the load capacitance.

2.4.2 Design for Low NEF

The methodology presented in Section 2.2 is applied on the CG architecture to analytically optimize its noise-power trade-off and understand its limitations. The total thermal IRN PSD of the CG amplifier is given by

$$S_{\text{in}} = \frac{8kT/I_{BN}}{\left(\left(\frac{g_m}{I_D}\right)_1 + \left(\frac{g_m}{I_D}\right)_3\right)^2}\left[\gamma_1\left(\frac{g_m}{I_D}\right)_1 + \gamma_3\left(\frac{g_m}{I_D}\right)_3 + \frac{1}{R_1 I_{BN}} + \left(\frac{(g_m/I_D)_3}{(g_m/I_D)_5}\right)^2\left(\gamma_9\left(\frac{g_m}{I_D}\right)_9 + \gamma_5\left(\frac{g_m}{I_D}\right)_5\right)\frac{I_{BN}}{I_{BP}}\right], \tag{2.38}$$

where γ represents the noise coefficient from (2.4). Assuming a large resistance value for R_1 (MΩ range), the noise from that component is neglected. The effects of CR can be observed in (2.38) with the sum of the (g_m/I_D) values on the denominator. Flicker noise is not studied in this topology as gate area is not strictly limited.

Some design choices can be made through an analytical optimization based on (2.38) that minimizes the noise PSD assuming a given total current consumption.. First, the DC current allocation between I_{BN} and I_{BP} is optimized, giving

$$\rho = \left(\frac{I_{BP}}{I_{BN}}\right)_{\text{opt}} = \frac{(g_m/I_D)_3}{(g_m/I_D)_5}\sqrt{\frac{\gamma_9\left(\frac{g_m}{I_D}\right)_9 + \gamma_5\left(\frac{g_m}{I_D}\right)_5}{\gamma_1\left(\frac{g_m}{I_D}\right)_1 + \gamma_3\left(\frac{g_m}{I_D}\right)_3}}. \tag{2.39}$$

At optimal current allocation, the noise PSD in (2.38) is rewritten as

$$S_{\text{in}} = \frac{16kT(1+\rho)/I_{\text{tot}}}{\left(\left(\frac{g_m}{I_D}\right)_1 + \left(\frac{g_m}{I_D}\right)_3\right)^2}\left[\gamma_1\left(\frac{g_m}{I_D}\right)_1 + \gamma_3\left(\frac{g_m}{I_D}\right)_3 + \left(\frac{(g_m/I_D)_3}{(g_m/I_D)_5}\right)^2\left(\gamma_9\left(\frac{g_m}{I_D}\right)_9 + \gamma_5\left(\frac{g_m}{I_D}\right)_5\right)\frac{1}{\rho}\right], \tag{2.40}$$

where $I_{\text{tot}} = 2\,(I_{BN} + I_{BP})$ is the total current consumption of the LNA.

The optimal choices of (g_m/I_D) values for each transistor can also be evaluated. To minimize the amplifier noise, $M_{1,2}$ should be pushed toward very weak inversion. To minimize the noise contribution of the level shifter branch, $M_{5,6}$ should also be biased in weak inversion. $M_{9,10}$ act as loads to the level shifter branch and are optimally biased in strong inversion, as

indicated by (2.40). The case of $M_{3,4}$ is more complicated since increasing $(g_m/I_D)_3$ decreases the noise from the main branch but increases the noise from the level shifters. If $M_{3,4}$ are biased in weak inversion, the total transconductance is increased and the noise performance fully benefits from CR. However, those transistors also amplify the signal and the noise from $M_{5,6}$ and $M_{9,10}$. Given the low bias current in that branch, $M_{3,4}$ are optimally pushed toward strong inversion with the values of the noise coefficients in 22-nm FD-SOI. In those conditions, (2.39) gives $\rho \approx 0.2$. The theoretical minimum NEF is 1.25. Given the presence of strong-inversion transistors, the noise models depend on the minimum (g_m/I_D) that can be achieved in the circuit. $(g_m/I_D)_{\max}$ can be expressed from a standard technology parameter in (2.1) whereas $(g_m/I_D)_{\min}$ mostly depends on the maximum V_{GS} that can be reached in an amplifier given a supply voltage V_{DD}. Here, the amplifier uses LVT transistors and a V_{DD} of 1.8 V, allowing large V_{GS} values. $M_{9,10}$ can have a large V_{SG} as long as the biasing circuit generating V_{BP} is designed appropriately. $M_{3,4}$ can be pushed to strong inversion provided that

$$V_{DS,8,\min} + V_{SG,6} + V_{SG,3} \leq V_{DD}. \tag{2.41}$$

Given that $M_{5,6}$ are biased in weak inversion, $V_{SG,3}$ can be large. For this amplifier, $(g_m/I_D)_{\min} = 3\ \mathrm{V}^{-1}$ is assumed.

Simulation-based optimizations are performed on the CG amplifier to validate the analytical results and define an optimal sizing of the amplifier. The optimizations objectives, constraints and variables are similar to those used for the CR amplifier and are given in Table 2.3. The simulations are performed with $V_{DD} = 1.8$ V, $C_i = 30$ nF, and $C_L = 1$ pF. The range of dimensions for the transistors is limited taking into account the analytical optimal inversion regimes. While the input impedance of the LNA is not explicitly fixed, the constraint $f_L < 300$ Hz with fixed C_i enforces a minimum input resistance of 17.7 kΩ. From (2.37), it can be deducted that at maximum $(g_m/I_D)_1$, I_{BN} is limited to about 1 µA.

The optimization results are shown in Fig. 2.15. It can be seen that the simulated outputs closely follow the analytical optima. Potential designs with a total current larger than 4 µA necessitate to reduce $(g_m/I_D)_1$ or to increase I_{BP}/I_{BN} to respect the lower frequency limit given by (2.37) and are therefore not following the analytical iso-NEF trend.

Fig. 2.16 shows different design parameters of the optimization Pareto front. In Fig. 2.16(a), it can be seen that the current ratio reaches low values,

Table 2.3 CG amplifier optimization objectives, constraints and variables.

Objective	**Direction**
Supply Current	min.
RMS IRN	min.
Constraint	**Threshold**
In-band gain	> 35 V/V
Lower frequency limit	< 300 Hz
Upper frequency limit	> 10 kHz
Variable	**Range**
I_{BN} value	[0.05 - 4] µA
I_{BP} value	[0.05 - 1] µA
$R_{1,2}$ value	[0.1 - 20] MΩ
$M_{1,2}$ dimensions $W_{1,2}$ and $L_{1,2}$	[1.0 - 1000] and [0.1 - 50] µm
$M_{3,4}$ dimensions $W_{3,4}$ and $L_{3,4}$	[0.5 - 50] and [0.1 - 200] µm
$M_{5,6}$ dimensions $W_{5,6}$ and $L_{5,6}$	[0.5 - 1000] and [0.1 - 50] µm
$M_{7,8}$ dimensions $W_{7,8}$ and $L_{7,8}$	[2.0 - 200] and [2.0 - 100] µm
$M_{9,10}$ dimensions $W_{9,10}$ and $L_{9,10}$	[0.5 - 20] and [0.1 - 100] µm

as anticipated analytically. However, some values tend to be higher than expected, probably due to non-idealities at very low current values and a higher $(g_m/I_D)_3$ than expected. It shows that some deviations from the analytical model have little impact on the optimal results. In Fig. 2.16(b), the total gate area of each optimal design is higher than 15,000 µm^2, showing that large areas are always preferred to maintain high (g_m/I_D) values (shown in Fig. 2.16(c)) and low flicker noise. The regimes of inversion anticipated analytically are verified. $M_{1,2}$ and $M_{5,6}$ are pushed to their maximum (g_m/I_D) in most cases. $(g_m/I_D)_{9,10}$ is close to the minimum value of 3 V^{-1}. At low I_{BP}, the $(W/L)_{9,10}$ ratio required to reach $(g_m/I_D)_{\min}$ is very low, such that the dimension limits from Table 2.3 are reached. $M_{3,4}$ tend to have (g_m/I_D) values slightly above the anticipated minimum. Compared to the analytical expectations, designs with higher $(g_m/I_D)_{3,4}$ and I_{BP}/I_{BN} ratio are thus also optimal. For the designs with a supply current close to 10 µA, I_{BN} is limited due to the the constraint on f_L (2.37), reaching new optima that drift away from the iso-NEF curve.

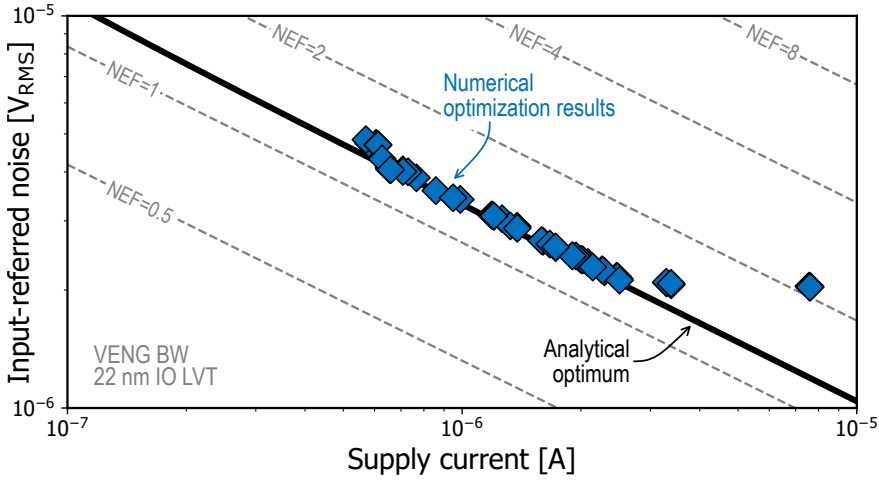


Fig. 2.15 Optimization results for the CG amplifier. The analytical optimum is shown as a solid black curve. The scatter plot indicates the simulation-based Pareto front. Iso-NEF lines are indicated with light dashes. Flicker noise is included in the simulations but minimized thanks to the unlimited gate area.

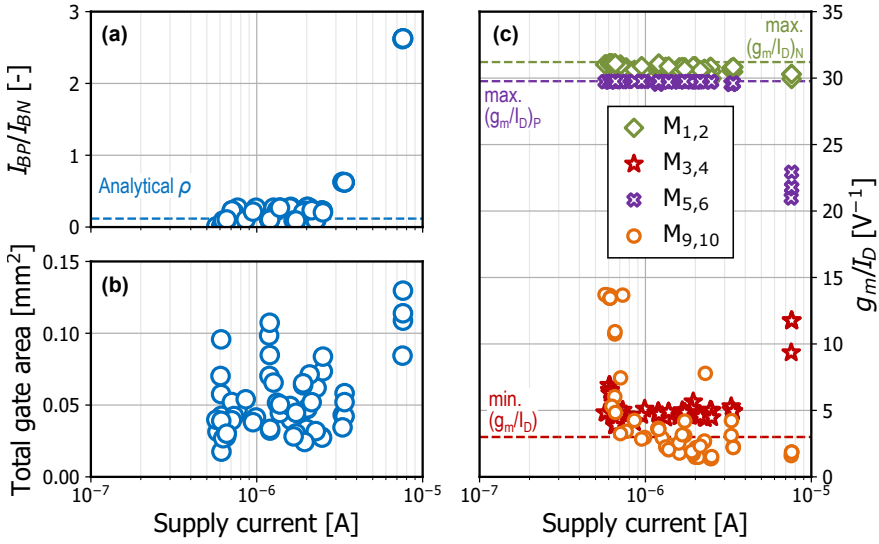


Fig. 2.16 Parameters of the simulation-based Pareto front. (a) Optimal I_{BP}/I_{BN} ratio compared to ρ derived analytically. (b) Total gate area. (c) (g_m/I_D) values for the main transistors, compared to the values assumed analytically.

Table 2.4 Transistor sizes selected for the CG LNA.

Device	$M_{1,2}$	$M_{3,4}$	$M_{5,6}$	$M_{7,8}$	$M_{9,10}$
W/L [µm/µm]	640/4.5	2.0/16	150/0.15	112/6.0	1.0/8.0

The optimization results highlight the weaknesses and strengths of the proposed LNA topology. Compared to a simpler CR amplifier topology such as the one in Fig. 2.8, the main disadvantages of the CG structure come from the addition of the level shifter branch. It increases the current consumption and forces to bias $M_{3,4}$ in strong inversion, which impacts the noise performance. Given that noise performance and input impedance both directly depend on the I_{BN} current, the CG topology has one less degree of freedom compared to the CR amplifier where the value of the off-chip resistor can be tuned independently. However, the CG LNA has the advantage of not requiring auxiliary components such as the off-chip resistors in the HPF and the auxiliary OTA for CMFB.

Given the optimization results, a sensitivity analysis is performed to reduce the total gate area and the layout of the proposed LNA is drawn. The selected transistor sizes are summarized in Table 2.4. The $R_{1,2}$ devices are implemented with narrow polyresistors with a 40-nm width and a value fixed at 1.7 MΩ to ensure a high $f_{H,CG}$ despite a large output capacitance. A biasing branch is added to generate V_{BP} from V_{BN} to generate the bias currents with a fixed ratio $\rho = 0.33$. The biasing branch allows to sweep the current consumption with V_{BN} as single tuning knob. The targeted range of supply current is from 1 to 4 µA. The current consumption of the biasing branch is not accounted for in the reported power.

The layout of the CG is presented in Fig. 2.17(a). The simulated post-layout performance is shown in Fig. 2.18 for different bias currents values, obtained by adapting V_{BN} at constant ρ. As I_{BN} increases, the in-band gain and the lower cut-off frequency increase. The higher cut-off frequency is roughly unchanged. Regarding the IRN, the thermal noise floor is approximately inversely proportional to the bias current. This approximation holds at constant dimensions in a limited current range thanks to the weak-inversion plateau in Fig. 2.4.The flicker noise is approximately constant with current variations. However, the input-referred representation of that noise is modulated by the HPF at low frequency. Given that the lower cut-off frequency increases with I_{BN}, so does the input-referred flicker noise PSD.

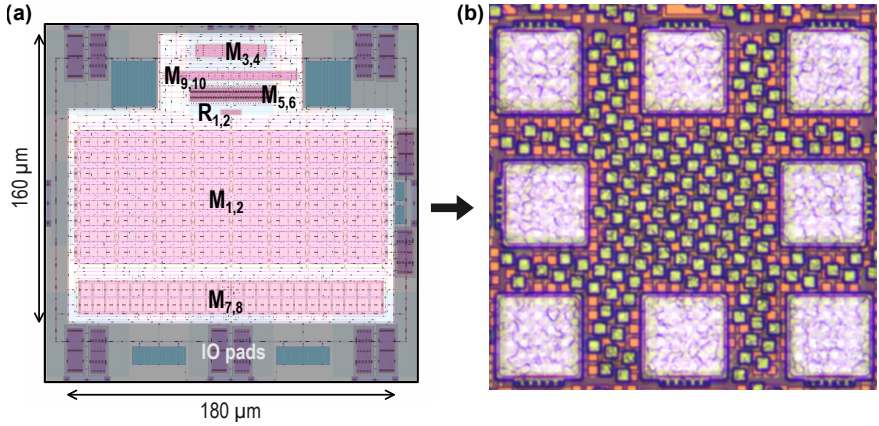


Fig. 2.17 CG amplifier implementation: (a) layout and (b) microphotograph.

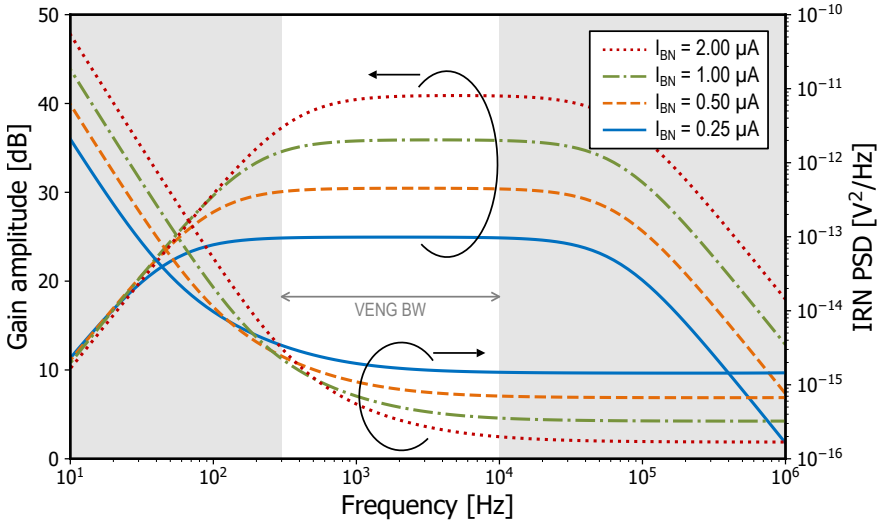


Fig. 2.18 Post-layout simulation results for the frequency response and the IRN PSD. Results shown for different values of the I_{BN} current with fixed I_{BP}/I_{BN} ratio.

2.5 Measurement Results

The proposed CG amplifier was prototyped as a stand-alone circuit on a chip in 22-nm FD-SOI from GlobalFoundries. The microphotograph of the

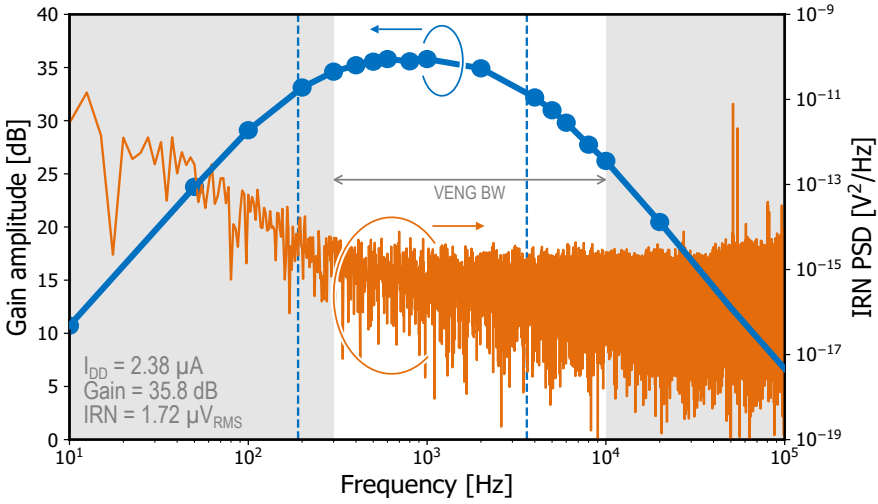


Fig. 2.19 Measured frequency response and IRN PSD of the CG amplifier for a 2.38-µA supply current. The -3 dB frequency limits are indicated as dashed vertical lines.

amplifier with its test pads is shown in Fig. 2.17(b). Due to metal filling, the main components cannot be distinguished. The amplifier occupies a silicon area of 30,000 µm^2. Transistors $M_{1,2}$ are the largest devices, taking about 63% of the total area. The measurements were performed at ambient temperature, hence $T = 25°C$ is assumed for the analytical comparisons.

The amplifier was tested in open loop using a custom printed circuit board, and the measurements were performed with a Scope Tek MSO 2024B oscilloscope. Fig. 2.19 shows measurement results combining the frequency response and the IRN PSD. It can first be seen that the upper frequency limit at 3.6 kHz is lower than the specified 10 kHz. This is due to a larger load capacitance than expected due to wire bonding and oscilloscope input. However, [94, 95] indicate that a [0.3-3.0] kHz bandwidth is sufficient for the observation of action potentials from a peripheral nerve. For the measurements of the proposed CG amplifier, the bandwidth of interest is thus limited up to 3.0 kHz. The flicker noise power is negligible in that frequency band and the IRN integrated in the $\pi/2 \times [0.3 - 3.0]$ kHz bandwidth gives a value of 1.72 µV$_{\text{RMS}}$.

The CG amplifier was measured for different V_{BN} values, sweeping the supply current at almost constant NEF. Fig. 2.20 shows those measurement results and compares them to state-of-the-art LNA or AFE designs. Ta-

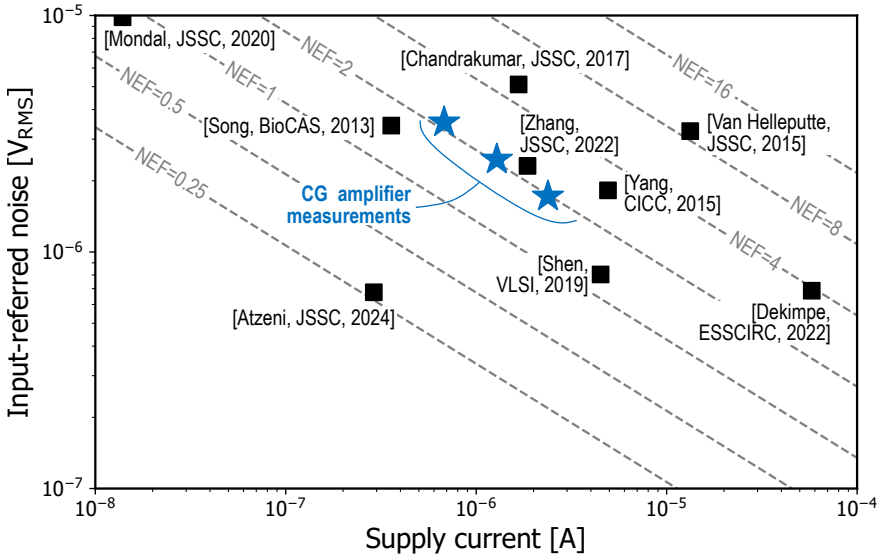


Fig. 2.20 Measurement results of the supply current and IRN for three different operating conditions (blue stars) and state-of-the art reference designs (black squares) ([2, 3, 9, 12, 25, 113, 119, 166, 167]). All noise results are rescaled to a [0.3-3.0] kHz bandwidth assuming a constant NEF.

ble 2.5 compares the proposed amplifier measurements in the lowest-noise configuration with other low-NEF designs. Compared to the only previous integrated VENG-specific amplifier [25], the NEF is approximately divided by 2. Table 2.5 shows that, beyond the competitive noise efficiency results, the proposed CG amplifier also reaches good performance in terms of harmonic distortion, common mode and power supply rejection, and output swing. The low input impedance is inherent to the proposed CG topology and is necessary for the high-pass filtering function. The impact of a low input impedance is further discussed in Chapter 3.

2.6 Conclusions

In this chapter, we introduced a hybrid methdology combining analytical and simulation-based models to easily estimate the optimal noise-power-area performance of bio-amplifiers. The noise models have the benefit of only requiring a few technology-dependent parameters that can be ob-

Table 2.5 Performance summary and comparison to state-of-the-art biomedical amplifiers.

	This work	Atzeni [3]	Dekimpe [25]	Mondal [9]	Shen [119]	Song [113]
Application	**VENG**	-	**VENG**	ECG	-	Neural recording
Technology	22 nm	22 nm	22 nm	180 nm	180 nm	180 nm
Area [mm^2]	**0.03**	0.21	0.077	0.24	0.14	0.16
Supply [V]	1.8	0.6/1.0	1.8	1.35	0.6	1.2
Power [µW]	4.29	0.24	104	0.02	2.7	0.43
Gain [dB]	35.8	47.6	91.5	36	46	26
Bandwidth [kHz]	[0.3-3.0]	10	[0.5-16]	0.24	8	[0.08-15]
IRN [μV_{RMS}]	1.72	1.30	1.4	-	1.4	8.1
NEF	1.97	**0.27**	3.87*	**0.86**	1.26*	1.52
PEF	6.99	**0.06**	27	**0.99**	**0.96**	2.77*
Input impedance [MΩ]	0.028	389	-	93	-	-
THD [%] (mV_{PP})	0.13 (1.0)	0.2 (10)	-	0.16 (16)	0.4 (3)	0.05 (10)
CMRR [dB]	>60	70	-	>95	84	>60
PSRR [dB]	>81	78	-	>68	78	>80
Output swing [V]	1.21†	-	-	-	-	-
Techniques	**CG**, CR	SC	Cascode	Stacking, chopping	Stacking, chopping	CR, cascode
Considered blocks	**HPF** + LNA	Multi-stage amp.	**HPF** + Amp. + ADC	Amp.	Multi-stage amp.	Closed-loop amp.

† Defined as output amplitude with -3 dB gain. * Computed from reported V_{DD} and NEF or power efficiency factor.

tained from simulations of a single transistor. The rest of the computations and optimizations can be done analytically. When applied to a current-reuse architecture, the proposed methodology demonstrates excellent agreement with simulation-based optimizations. For thermal noise, no significant differences are observed. Discrepancies up to 20% are present for flicker noise estimations due to the large ranges of variations of the technology-dependent parameters in the models. The proposed methodology facilitates the analysis of bio-amplifiers. It can help designers compare topologies, estimate the minimum area required for a certain level of noise, and provide insights on the optimal sizing of a circuit.

The CG amplifier presented in this chapter offers an innovative solution for input high-pass filtering. It features a CG input and an additional common-source differential pair, thus implementing CR. The main weaknesses of the CG LNA are its low input impedance inherent to the high-pass filtering function, and the noise in the DC-level shifter, that needs to be attenuated by biasing the common-source pair in strong inversion. Nevertheless, the prototype LNA achieves an IRN of 1.7 μV_{RMS} for a current consumption of 2.38 µA, thus reaching a competitive NEF of 1.97 in measurements.

Conclusions and Perspectives

THIS thesis targeted the design of an application-specific analog front-end (AFE) for use in a closed-loop neuromodulation system featuring seizure detection from vagus nerve activity. To achieve this objective, we proposed several methodologies and circuit-level techniques adapted to the acquisition of vagus nerve electroneurogram (VENG) signals. This well-defined application presents three major constraints: (i) ultra-low-power (ULP) operation for the entire front-end, (ii) low input-referred noise (IRN) in the low-noise amplifier (LNA), and (iii) rejection of in-band and out-of-band electromyogram (EMG) interference. This conclusion first summarizes the contributions of this thesis, then presents perspectives for further research in circuit design and seizure detection algorithms, and completes this work by taking a step back from the technical discussions to evaluate the objectives and conclusions of this thesis.

⋆ Summary of Contributions

The research question established in the introduction of this thesis proposes to leverage a solid knowledge of the VENG application and various circuit design techniques for the implementation and validation of an AFE that tackles the three aforementioned major technical challenges. This section summarizes those contributions by first synthesizing the exploration of the application context, then describing how the noise, power, and interference challenges are addressed in this work.

Definition of specifications: Specifications for the design of a VENG-specific front-end were derived by exploring the applicative context in Chapter 1. This analysis revealed quantified specificities of the VENG signals and requirements for the associated sensing system. First, VENG signals have a bandwidth from 0.3 to 10 kHz and are composed of action potentials (APs) of amplitudes from 10 to 30 μV_{PP}. As a result, noise should be minimized to the µV range to ensure a sufficient signal-to-noise ratio for signal processing. Second, it was observed that the EMG and stimulation artifacts interfere with the useful signal and have an amplitude several orders of magnitude greater than that of the VENG. Finally, by analyzing the batteries used to supply existing commercial vagus nerve stimulation (VNS) devices, a power budget of 50 µW was defined for the entire closed-loop stimulation system, and 10-15 µW for the front-end circuits. To conclude, the main technical challenges linked to VENG front-end are: (i) rejection of in-band and out-of-band EMG interference, (ii) minimization of the intrinsic noise in the acquisition circuits, and (iii) ultra-low power consumption.

Rejection of EMG interference: Dominating the useful VENG signals by multiple orders of magnitude, the EMG must be accurately rejected to ensure readability of VENG features. First, low-frequency (< 300 Hz) interference is filtered out at the very input of the circuits to avoid any saturation or distortion due to the EMG. A high-pass filter (HPF) is therefore placed at the input, before the LNA. For that filtering function, we propose to use off-chip capacitors in the nF range. Those can also be used for the DC-blocking capabilities required in implantable electronics. To complete the input HPF, we explored in Chapter 2 the use of passive resistors versus common-gate (CG) differential pairs, the choice between those two architectures being guided by noise optimizations. In the complete AFE in Chapter 3, analog and digital HPFs were added further in the acquisition chain to provide a stronger attenuation of low-frequency interference.

Second, in-band EMG is tackled by tripolar instrumentation amplifier (IA) architectures, leveraging the differences in propagation between VENG and EMG signals. Through behavioral simulations, it was shown in Chapter 3 that true tripole IAs strongly reject the EMG but fail in case of electrode imbalance. Then, imbalance compensation methods from previous works were simulated, showing good efficiency but suffering from gain mismatch in the IA. An inter-channel chopping technique was therefore proposed to minimize the impacts of gain mismatch on interference rejec-

tion by dynamic element matching. Given that the addition of a chopping scheme in the AFE represents a low cost in terms of power consumption, inter-channel chopping should be integrated in all tripolar IAs targeting EMG rejection. A chopping scheme working at 160 kHz was implemented in the AFE from Chapter 3, and on-silicon measurements demonstrated an effective gain mismatch of 0.35% and an interference rejection ratio of 55 dB.

Noise and power trade-off: Noise and power are highly interdependent design constraints. Reducing thermal noise comes at the cost of additional power consumption. Conversely, flicker noise can be minimized with other techniques that do not require increased current (e.g., chopping). In Chapter 2, large device areas are preferred over chopping to minimize flicker noise, mainly to avoid other effects of chopping such as low input impedance and higher required amplifier bandwidth. In that same chapter, it was shown that accurate LNA noise estimations could be made analytically based on device-level bias-dependent noise models. For the VENG application, noise from the input HPF was included in the estimations, requiring a formal definition of the equivalent noise bandwidth.

An innovative LNA topology was proposed to replace resistors in the input HPF by the input impedance of a CG input, achieving better noise performance. The proposed LNA additionally implements current reuse for noise and power efficiency. Prototyped in a 22-nm FD-SOI chip, the proposed LNA achieves a noise efficiency factor of 1.97. Next, in Chapter 3, the CG LNA was integrated in an entire ULP front-end. Weak inversion biasing was used in the analog filters and custom capacitors were implemented in the analog-to-digital converter (ADC), in order to minimize the power consumption of those circuit blocks. The proposed front-end was characterized in a 65-nm CMOS chip and demonstrated an IRN of 1.80 μV_{RMS} for a power consumption of 13.3 μV_{RMS}, resulting in a power efficiency factor of 5.9. The AFE was additionally validated for the acquisition of AP waveforms of amplitudes higher than 20 μV_{PP}.

Finally, with a system-level perspective, Chapter 4 targeted the optimization of front-end specifications to minimize total power consumption while ensuring accurate seizure detection. The sensitivity of the power-accuracy trade-off was computed with respect to noise, common-mode rejection, dynamic range, ADC resolution, and ADC oversampling rate. It was first observed that noise has a significant impact on both power consumption and algorithm performance, encouraging precise optimiza-

tions of the tolerated noise level. Limiting the dynamic range also reduces seizure detection accuracy. Next, given the high IA noise level, quantization noise in the ADC is negligible. Since ADC resolution and oversampling impact the ADC and the neighboring circuits, the number of bits and sampling rate should be selected for minimum power consumption. Finally, seizure detection can be performed accurately even with poor accuracy in detecting low-amplitude APs. As a result, a high noise level can be tolerated. Potentially optimal front-end specifications were proposed, achieving perfect seizure detection on the VENG dataset for a power consumption of only 2.1 µW and an IRN of 3 μV_{RMS}. It should also be noted that, while the silicon measurements of the CG LNA showed a borderline input impedance of 28 kΩ and 40 kΩ in Chapters 2 and 3 respectively, the higher LNA noise tolerance in the optimal design proposed in Chapter 4 results in a simulated input impedance of 235 kΩ, which is sufficient to interface a VENG cuff electrode.

⋆ Perspectives

While this thesis presented what we believe are significant advances toward ULP VENG sensing, more research is necessary in different areas to reach a complete implantable closed-loop VNS system. Similarly, alternative circuit-level advances can be investigated further for performance improvement and application in other contexts.

The biomedical application targeted in this thesis is still novel and under research. While the superior efficacy of closed-loop VNS has been proven compared to the open-loop counterpart [54], no VENG-triggered VNS device has ever been tested in human subjects. Further investigations are necessary to determine system specifications such as the maximum latency from seizure onset to stimulation, and the stimulation current amplitude required for therapeutic effect. Additionally, the feasibility of using VENG as a biomarker for multiple types of seizures still has to be demonstrated. While vagus nerve has been proven to vary between baseline and PTZ-induced tonic-clonic seizures in rat subjects [22, 23], another experiment on VENG-based detection of kainic acid-induced seizures mimicking temporal lobe epilepsy failed to achieve accurate classification [21]. To improve seizure detection accuracy, multi-modal approaches represent a potential solution. For instance, the sensing part of a closed-loop VNS sys-

tem could include tachycardia detection and VENG sensing to enhance sensitivity and precision.

The circuits proposed in this thesis present significant performance enhancement compared to the state-of-the-art. However, several alternatives and improvements are still possible. First, the performance of the CG LNA was demonstrated in simulations and measurements. However, the presence of a level-shifter branch significantly affects the noise performance, which limits the benefits of that architecture for high-pass filtering and low-noise amplification as discussed in Chapter 2. To overcome that limitation, alternative topologies could be investigated. In [106], a closed-loop LNA is introduced, featuring high-pass filtering based on active feedback through a DC servo loop. Although the gain mismatch in that topology has yet to be evaluated, its noise performance and high input impedance are proven. Second, as introduced in Chapter 3, a VENG AFE requires an imbalance compensation scheme for EMG rejection. Since that functionality was the focus of a previous work [25] and showed excellent results, it was considered a solved issue in this thesis and was not included in the prototype AFE. For the integration of a complete system, imbalance compensation can be added to the proposed AFE without architectural modifications by acting on the LNA gains. Next, while the AFE proposed in Chapter 3 showed good performance, Chapter 4 demonstrated that modifications to the specifications and performance were possible to reduce power consumption while improving seizure detection accuracy. To validate those results, the 2.1-µW front-end proposed in Chapter 4 should be implemented and tested on silicon with VENG inputs. Finally, the proposed circuits were validated for the identification of APs in Chapter 3 and for seizure detection in Chapter 4. However, those validations are based on strong assumptions regarding the signal generation setup and on the generalization of the selected signals. In-vivo experiments would further validate the proposed AFE. Nevertheless, in-vivo validation of peripheral nerve interface circuits targeting implanted applications is more difficult than validating skin-surface acquisition circuits due to practical and legal complications.

Regarding seizure detection algorithms and their implementations, few works are based on VENG biomarkers. As a result, the template matching approach from [94] is the only open-source VENG-specific algorithm available. Alternative approaches should be researched, using intracranial EEG (iEEG)-based algorithms as inspiration, as discussed in Section 1.3. Using the template matching algorithm, it has been shown in Chapter 4 that the

detection metric varies strongly between baseline and seizure intervals, indicating clear markers of ictal events. However, the seizure sensitivity and precision results are less encouraging, presumably due to the small dataset used for classifier training and to the simplicity of the classification stage of the algorithm. That part of the system could thus benefit from a larger set of VENG data and more advanced machine learning techniques for classification. To that end, more acute experiments could be performed on rats, using pentylenetetrazol or kainic acid to induce seizures. However, the data resulting from those experiments would still be limited by the rat models. Some differences with human recordings exist, such as the electrode size, the type of seizures, and the importance of motion artifacts. Chronic human recordings would therefore be more beneficial to the research on seizure detection algorithms. However, animal or human experiments require ethical approval, time, expertise, and adequate signal acquisition systems. Building large datasets is thus a complicated task that has not yet been conducted for the niche application of VENG recording. To overcome these limitations, synthetic (i.e., artificially generated) data could be used to train seizure detection classifiers. However, generating synthetic biopotential signals requires advanced algorithms [188, 189] and a large high-quality and diverse non-synthetic original dataset [190]. Hence, a larger number of real VENG recordings is currently necessary to build synthetic datasets.

Another possible research axis related to VENG-based seizure detection is the low-power implementation of the algorithms. Current versions are executed on large servers whose resources are not a limiting factor. In an implanted system, however, the back-end performing seizure detection in real time is restricted in terms of available memory, power consumption, and execution time. To fit into those specifications, algorithm modifications such as fixed-point representations are necessary, which could affect seizure detection accuracy. In terms of implementation, different efficient techniques should be researched, such as hardware acceleration of some processing tasks, and custom instructions in the CPU. Preliminary studies in that direction were conducted as Master theses at UCLouvain [191, 192].

Finally, several challenges remain at the level of the implantable system. First, the stimulator and the sensing system must be co-integrated, possibly on two different systems-on-chip, with the stimulator implemented in a high-voltage tolerant technology. The stimulator must additionally include blanking switches to disconnect the sensing chip during stimulation to protect it from stimulation-related voltage spikes. Next, in this thesis, we

assumed the use of the same battery as in the AspireSR VNS device. However, other batteries and other supply technologies could be investigated to increase the power budget of the system. At last, biocompatible casings must be selected, and specific electrode materials might be necessary to ensure patient safety during magnetic resonance imaging procedures.

⋆ Final Words

To conclude this thesis, let us take a step back to reflect on the choices and motivations that guided the definition of this research topic.

First, the research was oriented toward application-specific circuit design to optimize the performance of the system. It allowed the identification of application-specific constraints (e.g., filtering of EMG interference), and the discard of other generic requirements (e.g., MΩ-level input impedance). Although the performance improvements thanks to this approach were not quantified, this application-driven approach facilitates the calibration of circuit performance to system requirements.

Second, this thesis follows a top-down approach for Chapter 1, then switches to bottom-up for the remaining Chapters. Indeed, Chapters 2-4 follow the chronological order of the conducted research. In fact, the findings from Chapter 4 (e.g., noise tolerance and optimal ADC configuration) would significantly affect the LNA and AFE designs, were those results obtained earlier. If a top-down approach had been selected for that research, the complete AFE presented in Chapter 3 would have been designed to meet the specifications of the optimal 2.1-µW front-end. However, the system-level approach chosen in Chapter 4 requires a good knowledge of both the major challenges at circuit level and the application specificities. In the case of this work, developing that knowledge was achieved progressively and working at a higher level of abstraction from the beginning was therefore not possible. If those are known at the start of a project, research should start with a high-level study similar to the one presented in Chapter 4.

VENG-based seizure detection systems were preferred over iEEG devices due to concerns about the dual-use potential of the latter, notably the risk of facilitating the development of non-medical brain-computer interfaces (BCIs). Although VENG systems were targeted in every part of this thesis, there was no intention of limiting the use of the proposed cir-

cuits and methodologies in other applications. For instance, the proposed methodology for the accessible comparison of LNA topologies in Chapter 2 is portable to any application with noise, power, and area specifications. Similarly, inter-channel chopping can be used in other contexts for gain mismatch mitigation. In this thesis, however, we chose to address technical challenges that are specific to the VENG application. While the rejection of EMG is central to this work, it is not a relevant field of study for iEEG recording. Similarly, minimizing flicker noise with large device areas is efficient in this work but would not be adapted to lower-frequency applications. Still, dual use of the research presented in this thesis is possible by re-using methodologies and transistor-level designs presented in this work. The direct application of the proposed circuits to BCIs is however presumably complicated due to the very different specifications between VENG and iEEG front-ends. For example, the relatively low input impedance of the CG LNA topology makes it impossible to use for electroencephalogram sensing that has to deal with higher levels of electrode impedance. Additionally, the VENG application tolerates a large LNA silicon area thanks to a limited number of channels (2). Such large area would not be appropriate for iEEG front-ends that require hundreds to thousands of channels.

Understanding the application context of an engineered system does not only facilitate performance improvements, it is also a catalyst for developing technologies that contribute to a specific benefit. At a time when innovations should be evaluated through the lenses of sustainability and socio-economic impact, we also encourage engineers and innovators to reflect on what societal needs are addressed by their products or services. In this regard, we believe that demands for new technologies in the healthcare sector constitute excellent examples of useful products and services that generally target genuine medical needs.

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Appendix

A Technology Curves

The goal of this appendix is to provide more details about the transistor flavors in 22-nm FD-SOI and 65-nm bulk CMOS used for noise analysis in Chapter 2. Section A.1 shows (g_m/I_D) curves, and Sections A.2 and A.3 presents thermal and flicker noise performance, respectively.

A.1 (g_m/I_D) Curves

Fig. A.1 depicts the (g_m/I_D)- normalized drain current curves for different transistor flavors in 22-nm FD-SOI. It can be seen that core devices generally achieve a higher (g_m/I_D) than IO transistors, indicating a lower body factor n for core devices. Fig. A.2 shows the same curves for different flavors in 65-nm bulk and also demonstrates higher (g_m/I_D) for core devices.

A.2 Thermal Noise Coefficients

The thermal noise coefficient γ for transistors is defined as

$$\gamma = \frac{S_{i_d}}{4kTg_m}, \tag{13}$$

where S_{i_d} is the drain current noise power spectral density (PSD) in A^2/Hz, k is Boltzmann's constant, T is the temperature, and g_m is the transistor's transconductance.

Fig. A.3 shows the γ values extracted from simulations of various devices in 22-nm FD-SOI. It can be seen that despite higher (g_m/I_D) values,

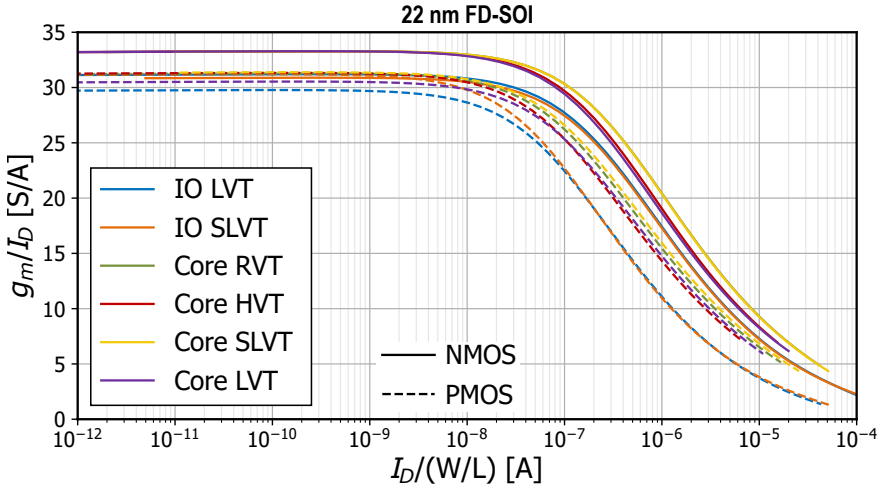


Fig. A.1 (g_m/I_D) vs drain current normalized to the transistor aspect ratio, for N-type (solid) and P-type (dashed) MOSFETs in 22-nm FD-SOI for different flavors (IO: LVT, SLVT, Core: RVT, HVT, SLVT, LVT). Curves extracted for $W = 100$ µm and $L = 1$ µm. $V_{DS} = 1.2$ V for IO devices, $V_{DS} = 0.8$ V for core devices.

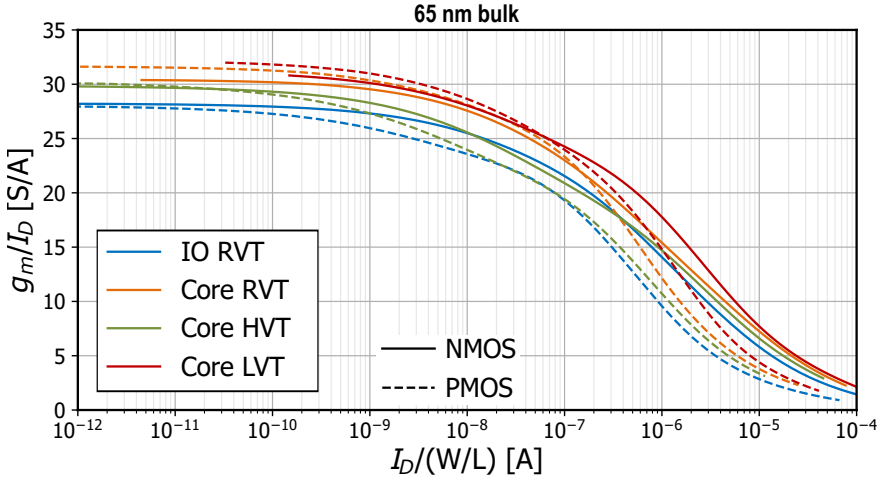


Fig. A.2 (g_m/I_D) vs drain current normalized to the transistor aspect ratio, for N-type (solid) and P-type (dashed) MOSFETs in 65-nm bulk for different flavors (IO: RVT, Core: RVT, HVT, LVT). Curves extracted for $W = 100$ µm and $L = 1$ µm. $V_{DS} = 1.8$ V for IO devices, $V_{DS} = 1.2$ V for core devices.

core transistors tend to show worse noise performance than IO devices. Fig. A.4 shows results of the same simulations in 65-nm bulk. In this second node, core transistors display better thermal noise performance.

A.3 Flicker Noise Coefficients

Our gate-referred flicker noise model for MOSFETs is given by

$$S_{v_g}(f) = \frac{\alpha}{(WL)f^{1+\xi}}, \tag{14}$$

where S_{v_g} is the voltage noise PSD in V^2/Hz, f is the frequency, α and ξ are bias- and technology-dependent parameters, and W and L are the device's width and length, respectively. In all simulations with 22-nm and 65-nm foundry models, ξ is bias-independent and its absolute value is lower than 0.2.

Figs. A.5 and A.6 show the α values extracted from simulations of various devices in 22-nm FD-SOI and 65-nm bulk, respectively. In both technology nodes, core transistors present better flicker noise performance.

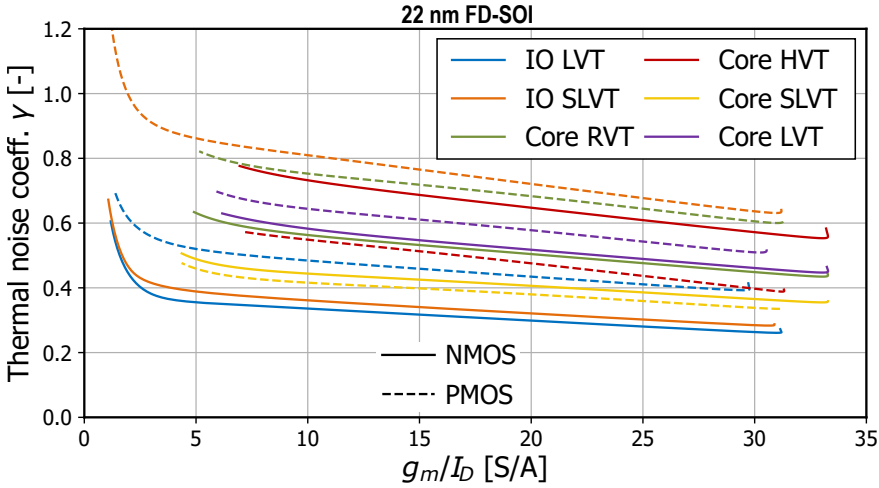


Fig. A.3 Thermal noise coefficients for N-type (solid) and P-type (dashed) MOSFETs in 22-nm FD-SOI for different flavors (IO: LVT, SLVT, Core: RVT, HVT, SLVT, LVT). Curves extracted for $W = 100$ µm and $L = 1$ µm. $V_{DS} = 1.2$ V for IO devices, $V_{DS} = 0.8$ V for core devices.

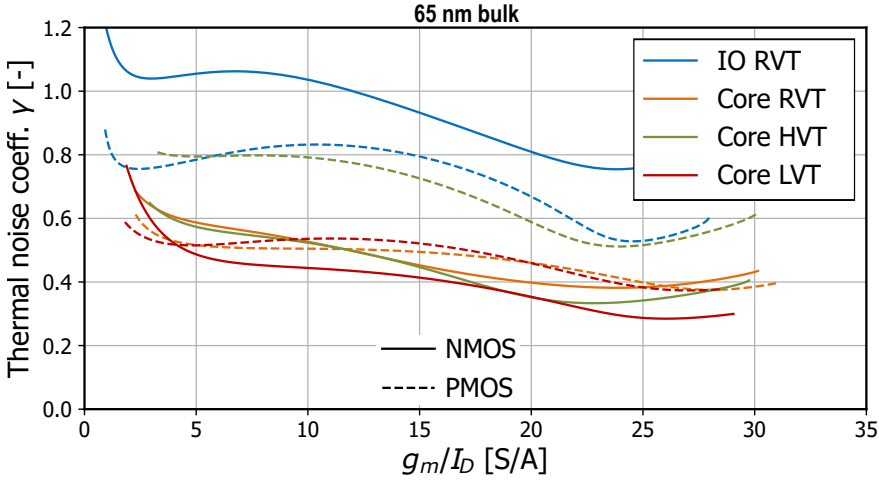


Fig. A.4 Thermal noise coefficients for N-type (solid) and P-type (dashed) MOSFETs in 65-nm bulk for different flavors (IO: RVT, Core: RVT, HVT, LVT). Curves extracted for $W = 100$ µm and $L = 1$ µm. $V_{DS} = 1.8$ V for IO devices, $V_{DS} = 1.2$ V for core devices.

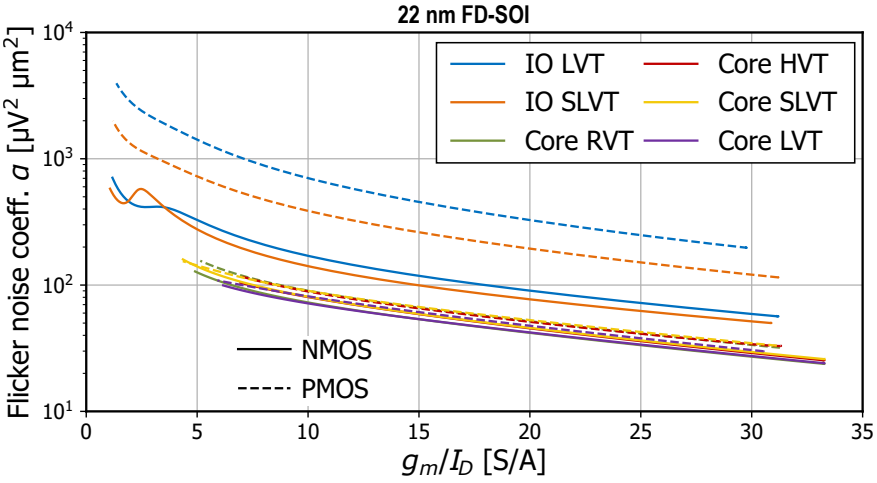


Fig. A.5 Flicker noise coefficients for N-type (solid) and P-type (dashed) MOSFETs in 22-nm FD-SOI for different flavors (IO: LVT, SLVT, Core: RVT, HVT, SLVT, LVT). Curves extracted for $W = 100$ µm and $L = 1$ µm. $V_{DS} = 1.2$ V for IO devices, $V_{DS} = 0.8$ V for core devices.

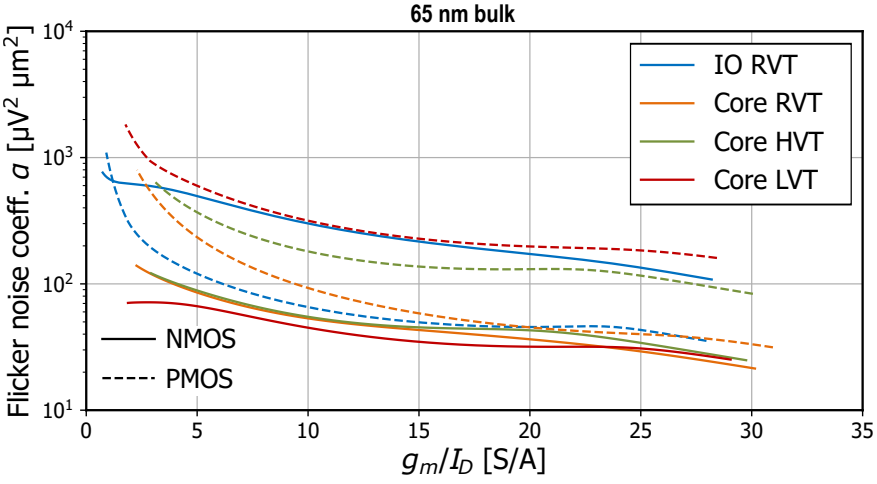


Fig. A.6 Flicker noise coefficients for N-type (solid) and P-type (dashed) MOSFETs in 65-nm bulk for different flavors (IO: RVT, Core: RVT, HVT, LVT). Curves extracted for $W = 100$ µm and $L = 1$ µm. $V_{DS} = 1.8$ V for IO devices, $V_{DS} = 1.2$ V for core devices.