Origin of Low-Temperature Negative Transconductance in Multilayer MoS_2 Transistors

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In this paper, negative transconductance (NTC) behavior in molybdenum disulfides (MoS_2) field effect transistors (FETs) is investigated. Combining experimental observation and numerical analysis, we demonstrate that, positive shift in the device transfer curves results from the electron trapping/de-trapping processes, where the defects densities at the MoS_2/SiO_2 interface are reduced when the temperature T decreases from 300 to 200 K. Moreover, the main types of defects that affect the device electrical performance are the interface defect and bulk sulfur vacancy V_S, in which V_S induces the p-type doping effect. While decreasing T below 100 K, NTC occurs when their active layer thickness t (= 41 and 35 nm) is larger than the Debye length λ (28 nm). Considering the n-type doping effect induced by the interface defects and the p-type doping caused by the bulk S vacancies, these two opposite doping regions are carefully implemented into simulation at T = 70 K. A vertical barrier induced by the inhomogeneous electron distribution enlarges with the increased gate bias V_{GS}, and thereafter leads to the unconventional increase of the contact and total resistances with $t > \lambda$. While $t \leqq \lambda$, the barrier and NTC behavior disappear. The current I_{DS} and transconductance g obtained from the simulation confirm the low-temperature NTC mechanism related to the defects, as discussed above. The material defects and physical origin of NTC discussed in the multilayer MoS_2 transistors, provide the theoretical foundation for designing and realizing novel structures of functional devices via defect engineering in the two-dimensional FETs.

Two-dimensional semiconductors (2DSC) are materials with a layered structure, where electrons can move freely in the 2D plane but are restricted in the out-of-plane direction [1,2]. Molybdenum disulfide (MoS_2), as a 2DSC, has been intensively investigated for its novel characteristics such as thickness-dependent bandgap (E_g = 1.2-1.9 eV), relative high mobility μ and stability *etc.*, and thus used as the semiconductor channel in high-speed 2DSC field-effect transistors (FETs) [3-7]. However, the defects that intrinsically exist in the MoS_2 material system [8] and are introduced by the process of fabrication [9], can affect the device electrical performance and need to be further clarified. For example, based on first-principle calculations, several types of bulk defects have been discussed in the multilayer MoS_2, such as sulfur vacancy (V_S) and Mo interstitial (Mo_I) [8]. Among them, V_S has a lowest value of formation energy and is found to be the most abundant defect [8]. In both the theoretical calculations and the experimental characterizations, V_S is either in a neutral or negative charge state [8,10,11], *i.e.* acts like the acceptor. Hence, in this work the acceptor-like V_S is considered. Moreover, the MoS_2-based FETs are inevitably affected by the defects at the semiconductor/insulator (S/I) interface and display different n- and p-type electrical characteristics [6,12,13]. For example, from monolayer to multilayer, MoS_2 transistors using common HfO_2 or SiO_2 dielectric show n-type doping [4,14]. And the p-type MoS_2 devices are fabricated with extra efforts such as using high work function metal [15], intentional doping [16]. In addition, the ambipolar MoS_2 transistors made by W. Bao *et al*. [6] exhibit more significant p-type behaviors than n-type by using defect-free polymer dielectric. Herein, what the intrinsic conduction type of the multilayer MoS_2 is, and how the defects affect the device performance from the perspective of semiconductor device physics, remain to be explored.

On the other hand, in the MoS_2 FETs, the negative transconductance (NTC) phenomenon has been observed when the operation temperature decreases from room temperature (300 K) to low temperature (40 K). Unlike the conventional NTC theories, *e.g.*, quantum tunneling [17] and mobility degradation [18] which are confined to the dual-gated and degenerately doped devices, a vertical barrier arising from inhomogeneous carrier distribution has been proposed to explain the NTC phenomenon [14]. However, the in-depth device physics related to the temperature T, the device geometry (such as thickness of the multilayer MoS_2), and the material property in term of defects, was not clearly justified to demonstrate the NTC mechanism.

Therefore, in this work, combining theoretical study and experimental observation we use the simulation methodology to investigate the defects inside the multilayer MoS_2 transistor and reveal the underlying mechanism of NTC, for its potential in circuit design of many different possible applications, such as frequency doubler and phase shift keying circuit [14].

Figure 1(a) illustrates the types of defects involved in our

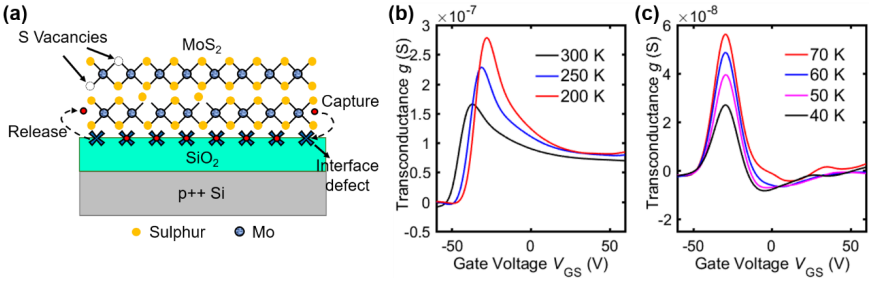

FIG. 1. (a) Schematic description of the interface and bulk defects (S vacancies) inside the MoS_2/SiO_2 material system. (b-c) transconductance g extracted from the experimental transfer curves as a function of gate voltage V_{GS} in the MoS_2 transistor, at temperature of (b) 200-300 K and (c) 40-70 K.

work, including the MoS_2/SiO_2 interface defects and the bulk point defects (V_S), *i.e.*, the most abundant defect intrinsically existing inside the multilayer MoS_2 [8]. It is also worth noting that other bulk defects have much higher formation energies than V_S (1.66 eV), *e.g.*, the formation energies of Mo vacancy and Mo interstitial are 7.24 and 4.02 eV [8], and hence insignificant effect on electrical performance of the MoS_2-based transistor. They are therefore not considered in this work. The interface defects of the MoS_2 transistor include the intrinsic structural defects and the extrinsic impurities, which are introduced by the device fabrication process, *e.g.* the dangling bonds [19] and Re impurities [8]. Depending on the electron trapping/de-trapping (capture/release in Fig. 1(a)) processes, the interface defects and the V_S can affect the electrical characteristics of the MoS_2 FETs.

Figures 1(b) and (c) illustrate the transconductance g (= dI_{DS} / dV_{GS}) extracted from the experimental transfer curves (I_{DS}-V_{GS} curves at V_{DS}= 10 mV and with T decreasing from 300 to 40 K) of the multilayer MoS_2 FETs with a semiconductor thickness t of 41 nm and a channel length L of 10 μm [14]. When T is decreasing from 300 to 200 K (Fig. 1 (b)), there is a positive shift in the g curves (as well in the transfer characteristics I_{DS}-V_{GS} of Ref. [14]). However, the g tends to sharply increase with V_{GS} at first, then decrease, and always keeps a positive value over the whole gate voltage V_{GS} range. Under the low-temperature conditions (T ranging from 70 to 40 K in Fig.1 (c)), the values of g get to be negative while increasing V_{GS}, *i.e.*, NTC behaviors are displayed (the current decreases when the gate voltage increases). As a negligible potential barrier within vertical direction has been observed from the linear I_{DS}-V_{DS} curve at the low temperature [14], *i.e.*, Ohmic contacts are formed, the NTC phenomenon may not be related to the impact of the front interface and the metal/semiconductor contacts.

Therefore, to deeply interpret the electrical performances of the MoS_2 transistors with decreased temperature, we implement the device simulations in Atlas/SILVACO [20] and set the multilayer MoS_2 bulk and the MoS_2/SiO_2 interface defects as schematically shown in Fig. 1(a) and the device geometry used in Figs. 1(b) and (c) [14]. Basically, the band gap E_g is 1.2 eV for eight or more layers of MoS_2 [21], with an affinity of 4.2 eV [22,23]. Volume carrier mobility is set as 100 cm^2 V^{-1} s^{-1} [24], and the relative dielectric permittivity of multilayer MoS_2 used in the simulation is 15 [25].

Figure 2(a) shows the transfer characteristics (obtained from Atlas [20]) of the multilayer MoS_2 transistor within the T range of 300 to 200 K, the transconductance g is correspondingly extracted in the inset. Also, the linear output curves (I_{DS}-V_{DS}) are shown in the inset to Fig. 2(a), validating the formation of Ohmic contacts. A positive shift of transfer curves occurs when the temperature decreases, *i.e.*, V_{TH} is getting larger, that

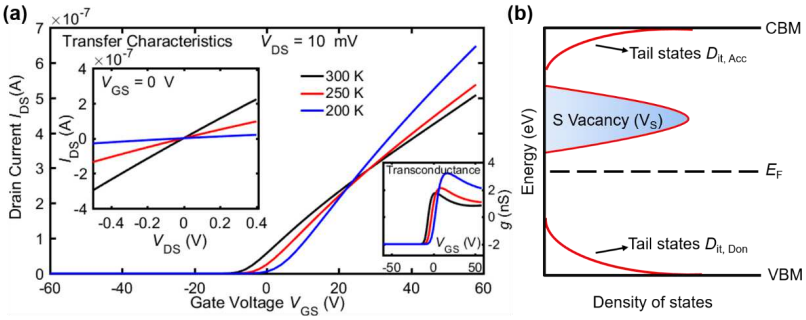

FIG. 2. (a) Simulated transfer characteristics at V_{DS} = 10 mV (T = 200-300 K). The insets depict the corresponding transconductance g and the output curves at V_{GS} = 0 V. (b) Defects distributions in the MoS_2 energy band.

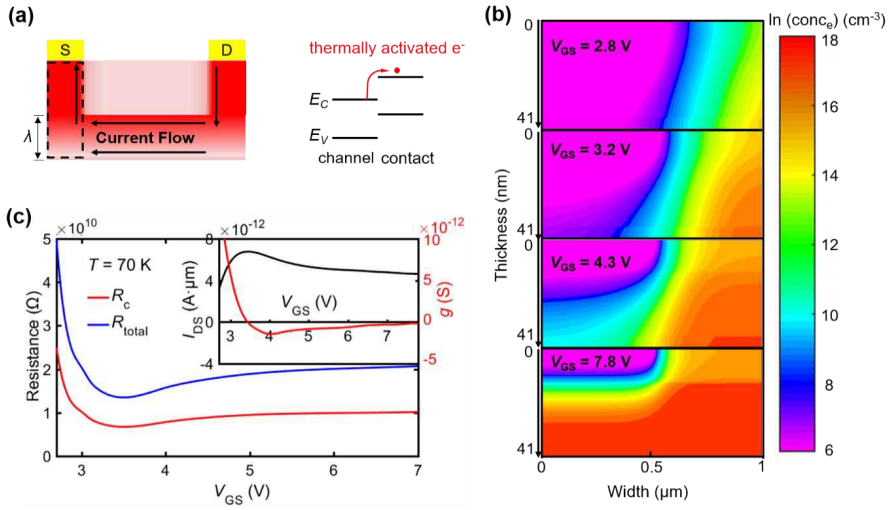

FIG. 3. (a) Current flow in a MoS_2 FET, with the multilayer MoS_2 thickness (t = 41 nm) larger than the Debye length ($t > \lambda$ = 28 nm). (b) Distribution of the electron concentration (the dotted box region in (a)) at the varied gate bias V_{GS} (from 2.8 to 7.8 V). (c) Contact and total resistances R_C, R_{total} as functions of V_{GS}. The inset shows the corresponding g and I_{DS}. Here V_{DS} = 10 mV, T = 70 K.

originates from the electron trapping/de-trapping processes occurring at the MoS_2/SiO_2 interface [13,26,27]. However, the interface defects were often discussed as the cause of hysteresis in transfer characteristics of the MoS_2 transistors [26,28,29]. Furthermore, a positive V_{TH} could occur under lower temperature and thereafter lead the transistor into an enhancement-type device. Figure 2(b) illustrates the distributions of the tail-distributed interfacial acceptors $D_{it,\,Acc}$ and donors $D_{it,\,Don}$ lie near CBM and VBM [30]. CBM and VBM separately represent the conduction band minimum and the valence band maximum, E_F is the symbol of Fermi level. Electron in the interface defect level probably has enough thermal energy to jump into the conduction band as the temperature increases, whereas it will be constrained by the defect at low temperature. Therefore, as the temperature drops, the positive charges obtained by ionization of donor-type defects $D_{it,\,Don}$ decreases, while the negative charges obtained by electrons trapping of acceptor-type defects $D_{it,\,Acc}$ increases, thus leading to the positive shift of V_{TH}. As a consequence, the initial densities of $D_{it,\,Don}$ and $D_{it,\,Acc}$ at 300 K are 3×10^{14} cm^{-2} eV^{-1} and 1×10^{15} cm^{-2} eV^{-1}, respectively [8,31], and are reduced to be 2×10^{14} (1×10^{14}) cm^{-2} eV^{-1}, 9×10^{14} (7.5×10^{14}) cm^{-2} eV^{-1} at 250 (200) K, in the simulations.

Figure 2(b) also illustrates the distributions of the bulk defect V_S. The V_S is located at 0.31 eV lower than the CBM, with a density of 10^{13} cm^{-3} [32]. From another side, MoS_2 transistors with a polymer dielectric (free of interface trap states) and SiO_2 dielectric display different electrical characteristics [6]. Typically, the MoS_2 on SiO_2 dielectric shows a unipolar n-type behavior with low mobility, whereas a pronounced p-type behavior with increased mobility is observed while MoS_2 lying on polymer [6]. Based on the interface defects in the MoS_2/SiO_2 material system as discussed above and the acceptor-like S vacancy (V_S) in the multilayer MoS_2, we believe that the MoS_2 is intrinsically p-type doped due to V_S while the typical n-type behavior of the MoS_2 transistor would result from the MoS_2/SiO_2 interface defects, in difference to the previous reports where MoS_2 is intrinsically n-type doped [33,34].

As T is decreasing below 100 K, the negative transconductance (NTC) starts to occur in the 41 nm-thick MoS_2-based transistors, *i.e.*, the device total resistance (R_{total}) decreases markedly first and then increases with V_{GS} in Ref. [14]. To explain the NTC behavior in details, the device simulation is conducted at a representative low temperature (70 K) and thereafter analyzed. Considering the screening effect and interlayer coupling in multilayer MoS_2, Fig. 3(a) shows the schematic of the drain-source current flow inside the MoS_2 transistor, including the vertical transport under the contacts and the planar transport in the channel [14,35,36]. The Debye length λ in Fig. 3(a), which is the maximum distance that the gate voltage can control in the semiconductor channel [36,37]. The Debye length λ can be expressed as [38]

$$\lambda = \sqrt{-\frac{kT\varepsilon_S^2}{2q}\frac{d(1/C^2)}{dV_g}}, \quad (1)$$

where k is the Boltzmann constant, T is the temperature, ε_s is the dielectric constant of the semiconductor, C is the total capacitance of the semiconductor layer and q is the electron

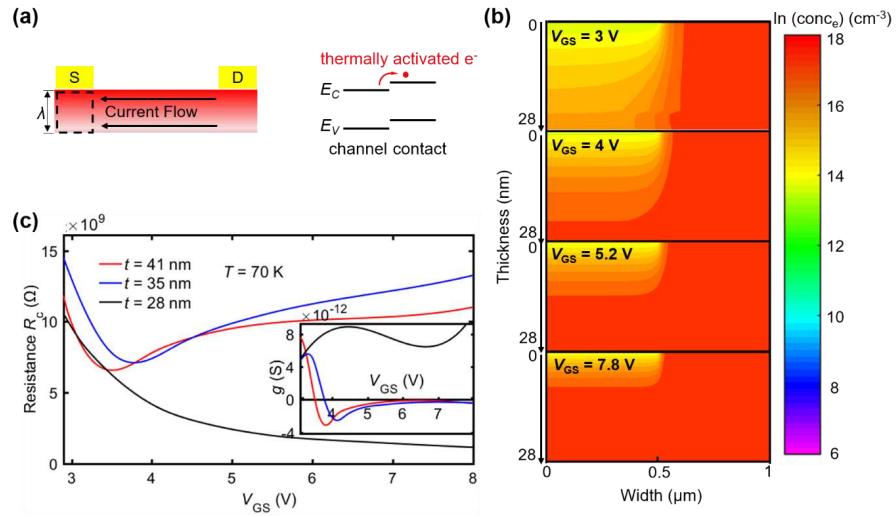

FIG. 4. (a) Current flow in a MoS_2 FET, with the multilayer MoS_2 thickness (t = 28 nm) smaller than the Debye length ($t \leqq \lambda$). (b) Distribution of the electron concentration (the dotted box region in (a)) at the varied gate bias V_{GS} (from 2.8 to 7.8 V). (c) Contact and total resistances R_C, R_{total} as functions of V_{GS}. The inset shows the corresponding g and I_{DS}. Here V_{DS} = 10 mV, T = 70 K.

charge. According to equation (1), the Debye length λ can be calculated from the capacitance-voltage (C-V) results of a typical metal-oxide-semiconductor (MOS) capacitor, which can be made from the multilayer MoS_2 [14]. The Debye length λ is set to be 28 nm here for the multilayer MoS_2 FET [14]. Because of the opposite doping effect from the interface defect (n-type) and the bulk defect V_S (p-type), there is a potential barrier between the n-type region near the substrate and the intrinsic p-type body (introduced by the V_S). Consequently, the carriers that flow in the channel must transport across the barrier, to reach the contacts (Fig. 3 (a)). At a higher temperature, electrons have enough thermal energy to cross the barrier, but this is getting limited as the temperature T decreases. The detailed distribution of the electrons below the contact region (the dotted box area in Fig. 3(a)) is depicted in Fig. 3(b), illustrating how the inhomogeneous carrier distribution is changed with V_{GS}. The low electron density under the contact mainly results from the acceptor-like V_S. The range of V_{GS} where the NTC appears in the experiment, *i.e.*, from 2.8 to 7.8 V, is highlighted. The electron concentration close to the back interface of the semiconductor channel is increased from ~10^{14} to ~10^{18} cm^{-3}, when V_{GS} increases from 2.8 to 7.8 V in Fig. 3(b). Since the intrinsic carrier concentration in MoS_2 is calculated to be around 10^{13} cm^{-3} [39,40], it means that the bottom region of the MoS_2 is n-type doped by the V_{GS} field effect. However, the electron concentration close to the metal contact remains unchanged, keeping around 10^6 cm^{-3}, *i.e.*, the p-type, with the increase of V_{GS}. In a word, the concentration difference between the two regions becomes larger, as well the barrier height increases. Furthermore, the boundary between the n- and p-type regions keeps moving upward, as shown in Fig. 3(b), which means that the position of vertical potential barrier keeps moving upward until it reaches the farthest distance that the gate voltage can control, namely, the Debye length. The contact resistance R_C (Fig. 3(c)) of the multilayer MoS_2 transistor are probed in the simulations to verify the barrier change. In the MoS_2 FETs, the contact resistance does not only include the resistance at the metal/semiconductor interface, but also the resistance of vertical current transport between the metal contact and the semiconductor channel (the dotted box area in Fig. 3(a)). As shown in Fig. 3(c), R_C (red curve) decreases at first (V_{GS} < 3.5 V) and then increases (V_{GS} > 3.5 V), consistent with the multi-terminal measurement in Ref. [14]. The low V_{GS} has a weak doping effect on the device, so the vertical barrier dependence on the difference of carrier concentration in the MoS_2 (as shown at V_{GS} = 2.8 V of Fig. 3(b)) is not high. Then the device resistance decreases with increasing V_{GS}, just like the traditional MOSFETs. And as V_{GS} continues to increase, the barrier gets higher, as well the resistance. The total resistance R_{total} (blue curve), which is obtained by probing the whole MoS_2 layer, shows in the similar trend with R_C, while the channel resistance R_{CH}, given by

$$R_{CH} = L/[W\mu C_{OX}(V_{GS} - V_{TH})], \quad (2)$$

decreases continuously with increasing V_{GS}. Considering the linear output curve under small gate voltage and low temperature in the MoS_2 transistor [14], the drain-source current I_{DS} of the MoS_2 transistor (T = 70 K and V_{DS} = 10 mV) is obtained using the equation $I_{DS} = V_{DS} / R_{total}$ and thereafter

the transconductance g is extracted, as depicted in the inset. The I_{DS}-V_{GS} curve displays an obvious NTC behavior and the g is smaller than zero (V_{GS} > 3.5 V), which proves that the modelling of the defects we set up in the simulation is reasonable.

Practically, the Debye length λ determines the boundary of the conductive channel [35,36,37], as well the position of the vertical barrier. Therefore, it is essential to investigate the impact of the multilayer MoS_2 thickness t on NTC. Fig. 4(c) illustrates the contact resistance as a function of V_{GS}, which is probed in the device simulations, with the MoS_2 thickness t = 41, 35, and 28 nm. As shown, when $t > \lambda$, the contact resistance R_C decreases first and then increases with the increase of V_{GS}. When $t \leqslant \lambda$, the contact resistance R_C always decreases with the increase of V_{GS}. Correspondingly, the calculated g in the insert of Fig. 4(c) confirms that when the MoS_2 thickness decreases down to 28 nm, the g keeps a positive value, *i.e.*, negative transconductance disappears while decreasing the MoS_2 thickness t below the Debye length λ.

The diagram in Fig. 4(a) shows the current flow inside the planar channel without an obvious vertical transport, where $t \leqslant \lambda$. The gate voltage can vertically control the entire region of the MoS_2 semiconductor channel. Hence, the whole multilayer MoS_2 keeps in the n-type condition with the increased gate voltage, and thus no p-n junction barrier forms in the semiconductor channel. Correspondingly, the distribution of the carrier concentration (the dotted box area in Fig. 4 (a)) is illustrated in Fig.4 (b), with t = 28 nm and 3 V $\leqslant V_{GS} \leqslant$ 7.8 V. Obviously, regardless of the gate voltage, the electron concentration in the entire region is larger than 10^{14} cm^{-3}, namely, n-type doping. A slightly low electron density under the contact occurs due to the semiconductor/metal contact effect. Therefore, the thermally activated electron can easily transport from the channel to the contact crossing a negligible n-n^- barrier. In this case, the NTC does not occur.

On the basis of the experiment and simulation results discussed above, it is worth pointing out that the existence and the corresponding effect of the defects (including the interface and bulk defects) in the 2D material system should not be ignored, while understanding the device performance. And the NTC mechanism, in which a barrier is formed by the inhomogeneous carriers' distribution induced by the defects, can open up a new way for the design of next electronics, *i.e.*, we can intentionally induce the NTC phenomenon through defect engineering in the 2DSC field-effect transistors to realize the specific functionality.

To summarize, the negative transconductance (NTC) phenomenon in MoS_2-based FETs has been investigated in this work, regarding the bulk and interface defects, the semiconductor thickness t, and the temperature effect. By combining the theoretical and experimental works and analyzing the device transfer I_{DS}-V_{GS} curves in Atlas/SILVACO, we clarified that the MoS_2/SiO_2 interface defects induce the n-type doping effect into the MoS_2 transistors, and result in the V_{TH} positive shift in the transfer curves while decreasing the temperature T. Additionally, the bulk S vacancies introduce the intrinsic p-type doping in the MoS_2 material. Decreasing T below 100 K, the probed device resistance firstly decreases and then increases with V_{GS}, because a vertical barrier forms between the p-type upper region and the n-type bottom region is electrically controlled by the gate bias, and the electrons have not enough thermal energy to cross the barrier under the low-temperature condition. In opposition, the barrier and NTC disappear when the multilayer MoS_2 thickness is smaller than the Debye length λ for the whole MoS_2 semiconductor channel is effectively controlled by the gate bias. This paper systematically analyzes low-temperature NTC phenomena in the multilayer MoS_2 transistor and elucidates the corresponding physical mechanisms, which opens the door to the realization of specific functionality in the two-dimensional semiconductor devices while considering the defects impact, and contributes to the development of numerical simulation studies for deeply interpreting the device physics of 2D-based FETs.

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DATA AVAILABILITY

The data that support the findings of this study are available from the corresponding author upon reasonable request.

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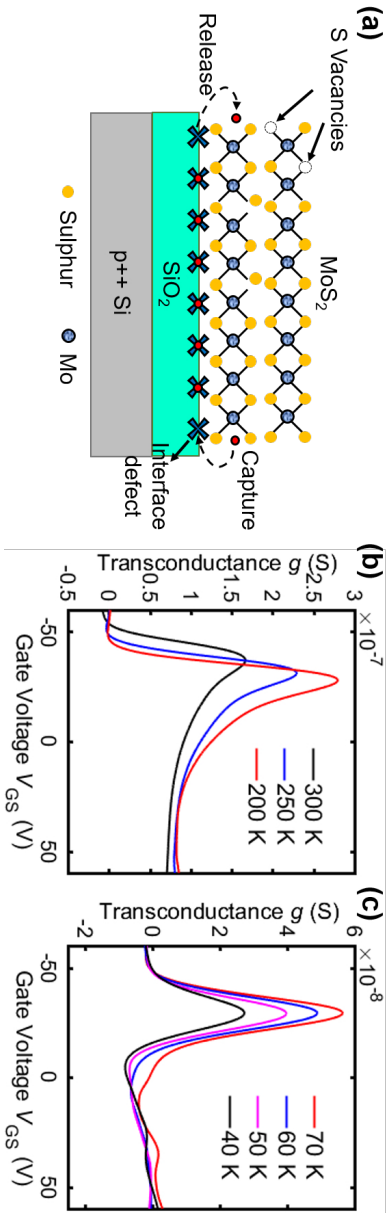

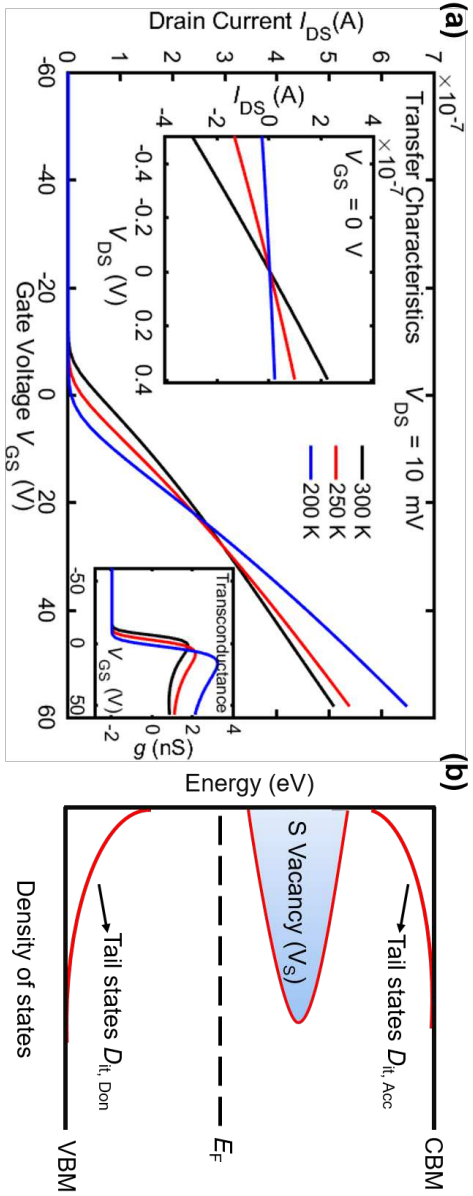

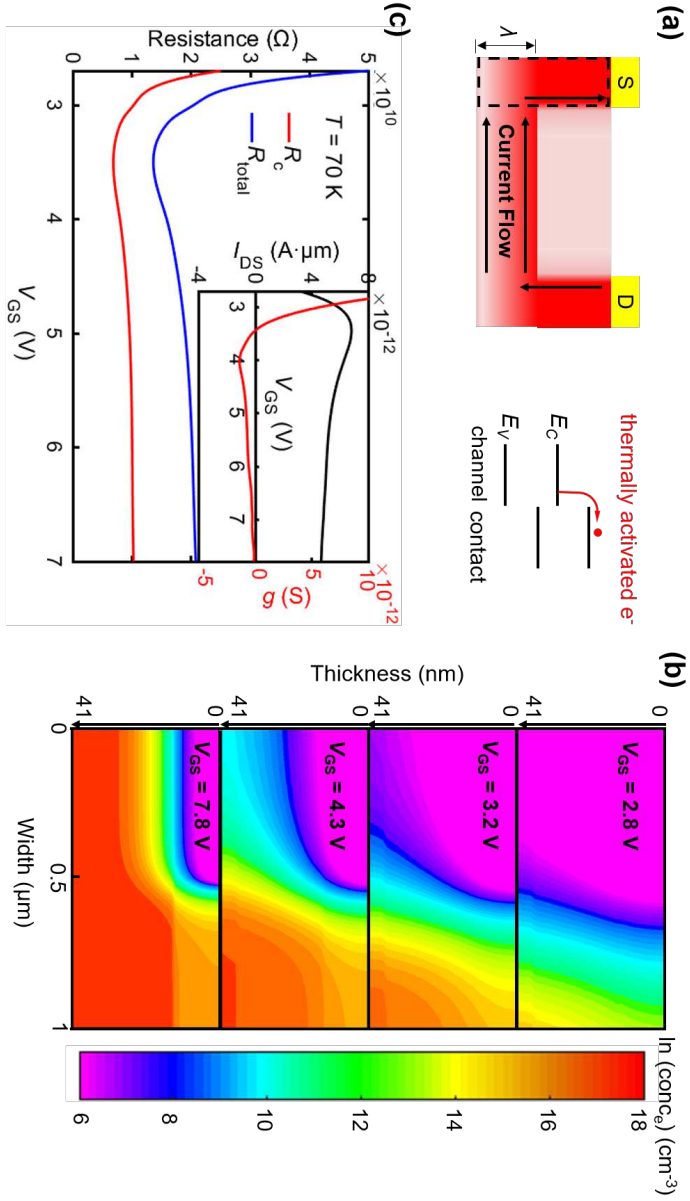

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