

Chapter 2

Nanofabrication and measurement techniques

2.1 Introduction

The first part of this chapter (sections 2.2 and 2.3) is dedicated to the presentation of all the techniques involved in the fabrication of the InGaAs billiards and nanojunctions (discussed in chapters 3 and 5, respectively) and the processing of bismuth films and cavity, analyzed in chapter 4. We concentrate on the general procedures applicable for the full set of samples, even though specific details of the fabrication process differ from one sample to another. Indeed, some process parameters depend on the wafer structure, and/or on the device layout geometry. Several techniques were used in the fabrication of both Bi and InGaAs samples (e-beam evaporation, e-beam lithography, ...), although the parameters were somewhat different in each case. The rationale behind the choice of the parameters is given for each process. At the beginning of sections 2.2 and 2.3 we also introduce the main physical properties of the starting materials. Some of these properties, such as the layer structure, or the crystallography, have an influence on the fabrication process.

In the second part of this chapter, we give details about the measurement techniques. We begin with an overview of the cooling system. Then, we explain issues related to the electrical measurements of our samples. Many aspects are involved here, as we are dealing sometimes with very small effects in very small devices, in extreme conditions (large magnetic fields, ultralow temperatures, very small electrical currents and voltages). More specifically, we are interested here in magnetoconductance measurements,

at temperatures ranging from 0.3 K up to room temperature. Note that we only present here the technique used for the measurement of the magnetoconductance. The details of the nonlinear measurements on the InGaAs nanojunctions are presented at the beginning of chapter 5 (section 5.3).

2.2 InGaAs samples

	A	B & C
Cap (doped)	In _{0.52} Al _{0.48} As 15 nm	In _{0.52} Al _{0.48} As 15 nm
Schottky	In _{0.52} Al _{0.48} As 15 nm	In _{0.52} Al _{0.48} As 15 nm
δ - doping	Si $4.5 \cdot 10^{12}/\text{cm}^2$	Si $5 \cdot 10^{12}/\text{cm}^2$
Spacer	In _{0.52} Al _{0.48} As 10 nm	In _{0.52} Al _{0.48} As 5 nm
Channel	In _{0.70} Ga _{0.30} As 15 nm	In _{0.70} Ga _{0.30} As 15 nm
Buffer	In _{0.52} Al _{0.48} As 400 nm	In _{0.52} Al _{0.48} As 400 nm
Substrate	InP	InP

← 2DEG

Figure 2.1: Schematic layer structure of our heterostructures.

The InGaAs/InAlAs heterostructures were produced by molecular beam epitaxy (MBE) in the IEMN cleanrooms. Fig. 2.1 shows the layer structures of the three heterostructures substrates (A,B,C) used in this thesis. At first, in section 2.2.1, we detail some important parameters of the alloys composing them. Then, the wafer growth procedure is described in section 2.2.2. In this section, we also discuss the influence of the layer structure on the 2DEG properties. All the following fabrication steps were performed in the DICE cleanrooms in UCL. We present in Table 2.2 the succession of technological operations performed after the wafer growth in order to fabricate a working device. The most critical steps of this process are detailed in sections 2.2.3 to 2.2.7. Our fabrication procedure is based on Ref. [56], which describes the realization of High Electron Mobility Transistors (HEMTs) on similar substrates at IEMN. Transposing the IEMN process in the UCL cleanrooms

was not as straightforward as it could seem, due to large differences in fabrication facilities. Note that a list of all the samples produced and analyzed in this thesis (with their main characteristics) is provided in appendix A.

Table 2.1: Standard process sheet for InGaAs nanodevices fabrication. Steps no. 23-31 are optional (gate process, see section 2.2.6).

Step	Description	Parameters
1	sample cutting	size $\simeq 3 \times 3$ mm
2	standard cleaning	acetone - methanol - DI water 5 min each, w/ ultrasound (acetone)
3	glueing on 2" Si wafer	glue : carbon paint
4	baking on hot plate	100°C - 5 min
5	drying in oven	140°C - 24h (at least)
6	resist spin coating	PMMA 3% in chlorobenzene 5000 rpm; 5000 rpm/s; 60 s
7	resist baking (hot plate)	160°C - 5 min
8	SEM lithography (mesa)	see section 2.2.3
9	resist development	MIBK:Isopropanol (3:1) 90 s - Isopropanol 20 s - DI water 10 min
10	mesa etching	H ₃ PO ₄ : H ₂ O ₂ : H ₂ O (5:1:40) 30 s DI water 10 min (see 2.2.4)
11	resist removal	boiling acetone 5 min
12	standard cleaning	same as step no. 2
13	glueing on 2" Si wafer	same as step no. 3
14	baking on hot plate	same as step no. 4
15	resist spin coating	PMMA 6% in chlorobenzene 5000 rpm; 5000 rpm/s; 60 s
16	resist baking (hot plate)	160°C - 5 min
17	SEM lithography (ohmic)	see section 2.2.3
18	resist development	same as step no. 9

Continued on next page

Step	Description	Parameters
19	metal deposition	see section 2.2.5
20	lift-off	boiling acetone 5 min or acetone w/ ultrasound 2 min methanol 5 min - DI water 5 min
21	rapid thermal annealing	see section 2.2.5
22	cap layer removal	see section 2.2.4
23	standard cleaning	same as step no. 2
24	glueing on 2" Si wafer	same as step no. 3
25	baking on hot plate	same as step no. 4
26	resist spin coating	same as step no. 15
27	resist baking (hot plate)	same as step no. 16
28	SEM lithography (gate)	see section 2.2.3
29	resist development	same as step no. 9
30	metal deposition	5 nm Ni; 100 nm Au
31	lift-off	same as step 18
32	bonding	see section 2.2.7

2.2.1 Material aspects

Several materials enter in the composition of our samples. All of them belong either to column III or V of the Mendeleev table. The most common crystal structure of the solid alloys of these elements (III-V compounds) is the sphalerite, or Zinc-Blend structure (an idealized view is shown on Fig. 2.2). It consists of two face-centered cubic lattices (with a lattice parameter a) of each element, offset with respect to each other by a distance $a/4$. In this structure, each atom of column III (respectively V) has four nearest neighbours belonging to column V (respectively III), forming a regular tetrahedron. The bonds in these III-V compounds are partially ionic and partially covalent: they are primarily covalent, with some residual excess charge about the ion cores [13].

At first, we concentrate on the physical properties of the binary compounds GaAs, InAs, InP, and AlAs, which will be useful to derive the properties of the ternary compounds of our heterostructures using interpolation

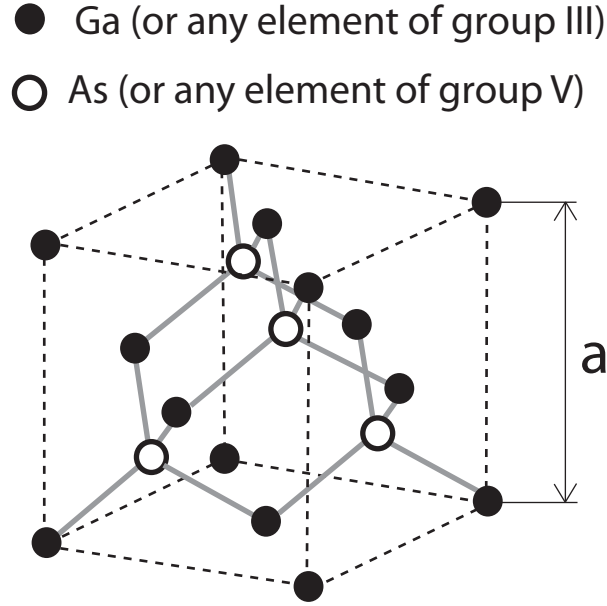


Figure 2.2: Scheme of a Zinc-Blend crystal structure. Grey lines are the chemical links. Dashed lines correspond to the limits of the unit cell.

methods. In Table 2.2, we gathered the main parameters of these compounds: their lattice parameter (a), the band gap at 300 K (E_g) and the effective mass (m^* , in units of the free electron mass m_0). Below, we briefly comment on these data, and concentrate on their implications in our work. We refer to the reference works of Sadao Adachi [1, 2] for detailed discussions about these parameters, and for additional data on these materials and their related ternary and quaternary alloys.

Crystal parameters

The lattice parameter $a_{A_xB_{1-x}C}$ of a ternary material $A_xB_{1-x}C$ can be directly deduced by a linear interpolation from the lattice parameters of the related binaries a_{BC} and a_{AC} [1]:

$$a_{A_xB_{1-x}C} = a_{BC} - x(a_{BC} - a_{AC}) \quad (2.1)$$

This law is very useful to determine the conditions to obtain lattice-matched heterostructures of InAlAs and InGaAs on InP. Indeed, one can infer from Eq. (2.1) that $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ and $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ have the same

Table 2.2: Lattice parameter, band gap (at 300 K), band gap (at zero temperature) and effective mass for GaAs, InP, InAs and AlAs (from [1, 2]).

Compound	GaAs	InP	InAs	AlAs
$a[\text{\AA}]$	5.6533	5.8688	6.0584	5.6611
E_g at 300 K [eV]	1.424	1.35	0.36	2.168
$E_g(0)$ [eV]	1.519	1.421	0.42	2.239
m^*/m_0	0.067	0.08	0.03	0.15

lattice parameter as InP. Therefore, these alloys will grow on InP wafers without strain.

Of particular interest here is the possibility of growing defect-free lattice-*mismatched* heterostructures on InP substrates ('pseudomorphic' InGaAs films), with a higher In content in the InGaAs layer ($\text{In}_x\text{Ga}_{1-x}\text{As}$, with $x > 0.53$), in order to obtain lower electron effective mass (see section 2.2.1). In this case, the lattice mismatch is accommodated by strain in the InGaAs film. The lattice parameter of the InGaAs layer in the growth plane becomes equal to the (smaller) lattice parameter of InP substrate, so that the crystal structure is under compressive strain and becomes tetragonal. Such a process implies that elastic energy (E_e) is stored in the lattice. This energy is proportional to the thickness of the InGaAs layer and to the square of the misfit (given by $\frac{a_{\text{InP}} - a_{\text{InGaAs}}}{a_{\text{InGaAs}}}$). Above a critical thickness, this energy will be large enough to generate a dislocation, or this energy will be relaxed by a transition from a two-dimensional to a three-dimensional growth mode. A lot of work has been devoted to refine this model since the derivation of the basic misfitting layer energy expressions [58] (we refer to [56] for references on the subject). Experimentally, from tests performed at IEMN, the critical thickness for InAs on InP is below 1 nm, and about 15 nm for $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ (the channel layer in our structures), in agreement with the literature [124].

Band gaps and conduction band discontinuity

Some precision must be given about the band gaps of the binary alloys presented in Table 2.2. InAs, InP and GaAs are direct-gap semiconductors: the top of the valence band and the bottom of the conduction band are both at the Γ point in these compounds (their band structure can be found *e.g.* in Ref. [35]). On the contrary, AlAs has an indirect gap: it has its minima

in its conduction band at X, and the maximum of the valence band at Γ (see Fig. 2.16 in Ref. [47] for the energy band structure of AlAs). A transition from direct to indirect band gap is therefore observed in ternary alloys such as $\text{In}_x\text{Al}_{1-x}\text{As}$, as a function of the composition. In this ternary compound, the transition occurs for $x = 0.29$ [56]: the gap is direct for $x > 0.29$, which is always the case in our structures.

In order to derive the band gap of the (unstrained) ternary compounds $\text{In}_x\text{Al}_{1-x}\text{As}$ from data in table 2.2, a quadratic relation must be used [36]:

$$E_{g,\text{In}_x\text{Al}_{1-x}\text{As}}(x) = E_{g,\text{AlAs}} - x(E_{g,\text{AlAs}} - E_{g,\text{InAs}}) + x(1-x)C \quad (2.2)$$

where the constant C is related to the alloy disorder. For $x = 0.52$, this equation yields $E_g = 1.439\text{eV}$ (room temperature).

In the case of (unstrained) $\text{In}_x\text{Ga}_{1-x}\text{As}$, a similar relation can be found, which gives $E_g \sim 0.75\text{eV}$ for $x = 0.53$ [1]. This value is slightly different in *pseudomorphic* epilayers of InGaAs . In these layers, the total strain can be decomposed in an isotropic (hydrostatic) strain which changes the band gap, and an anisotropic (uniaxial compression) strain which lifts the valence band degeneracy between heavy and light holes [62].

Moreover, the band gap is temperature-dependent. O'Donnell and Chen [126] propose the following expression for the temperature dependence of E_g :

$$E_g(T) = E_g(0) - S\langle\hbar\omega\rangle(\coth(\langle\hbar\omega\rangle/2kT) - 1) \quad (2.3)$$

where $E_g(0)$ is the zero temperature bandgap (given in Table 2.2 for the binary compounds), S is a dimensionless coupling constant and $\langle\hbar\omega\rangle$ is an average phonon energy. Comparing $E_g(0)$ and $E_g(300\text{K})$ in table 2.2, one observes a slight decrease of the band gap as the temperature increases in this range.

In heterostructures, an important parameter is the conduction band offset ΔE_c at the junction between the spacer and the channel layers. Indeed, it determines the height of the potential barrier faced by conduction electrons between the delta doped layer and the channel. In our case, the spacer is $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ and the channel is $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$, see section 2.2.2. An empirical expression for ΔE_c in the heterojunction $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_x\text{Ga}_{1-x}\text{As}$ was found by Huang and coworkers [82] for $x > 0.58$ (pseudomorphic case): $\Delta E_c(x) \sim 0.344 + 0.487x$ (in eV). This expression gives $\Delta E_c = 0.68\text{eV}$ for $x = 0.70$ (*i.e.* in our heterostructures).

Effective mass

The electron effective mass is a particularly critical transport parameter due to its direct relation with the electron mobility. One can note that InAs has the lowest effective mass among the binary compounds of Table 2.2. This is the main origin of the interest for heterostructures with a high In content in the channel layer. As in the case of the lattice parameter, one can obtain the effective mass of ternary compounds by a linear interpolation between the values of the corresponding binary elements, presented in Table 2.2 [1, 2]:

$$m^*/m_0(x) = 0.067 - 0.044x \quad (2.4)$$

in the case of unstrained $\text{In}_x\text{Ga}_{1-x}\text{As}$. Therefore, $m^*/m_0 \sim 0.036$ in unstrained $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$. As the strain affects the band structure, it also influences the effective mass. Simulations [124] showed that the effective mass in the plane of the heterostructure growth is increased in the case of pseudomorphic $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_x\text{Ga}_{1-x}\text{As}$ structures with $x > 0.53$. The calculated value in strained $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ is $m^*/m_0 \sim 0.04$.

2.2.2 Heterostructure growth

The best-quality semiconductor heterostructures are presently grown using molecular beam epitaxy (MBE). MBE systems indeed make possible the production of single-crystal multi-layer samples with a very accurate control of the thicknesses as well as the composition of the different layers, and with extremely abrupt changes in the composition. These features are the basic ingredients needed to obtain high mobility samples. Note that, ultimately, the mobility is limited in ternary systems at low temperature by an intrinsic mechanism, alloy scattering, arising from the random distribution of the alloy atoms in the available lattice points.

Fig. 2.3 provides a schematic illustration of a typical MBE system. It is essentially a very "clean" ultra-high vacuum evaporation chamber. Typical pressures of $\sim 10^{-14}$ atm inside the chamber are required during the growth process to avoid significant deposition of residual gas species on the substrate. Such a low pressure is obtained using various pumping systems such as ion-pumps and cryopumps. A heated ($\sim 520^\circ\text{C}$) semi-insulating (SI) InP substrate is placed on a rotating sample holder in front of effusion cells containing the high-purity source materials (here : In, Al, Ga, As and Si). Prior to heterostructure growth, the surface oxide is removed. Then, the cells are independently heated until the desired material flux is achieved. Shutters are positioned between each effusion cells and the substrate, to

be able to stop the flux reaching the sample within a fraction of a second. Controlling the shutters and the molecular flux ratios (through the effusion cells temperatures) allow to change the composition of the growing layer. Reflection high-energy electron diffraction (RHEED) is used to monitor *in situ* the surface morphology and crystallography. Typical growth rates of 1 monolayer of InGaAs per second ($\sim 1\mu\text{m/h}$) are used to obtain high quality heterostructures.

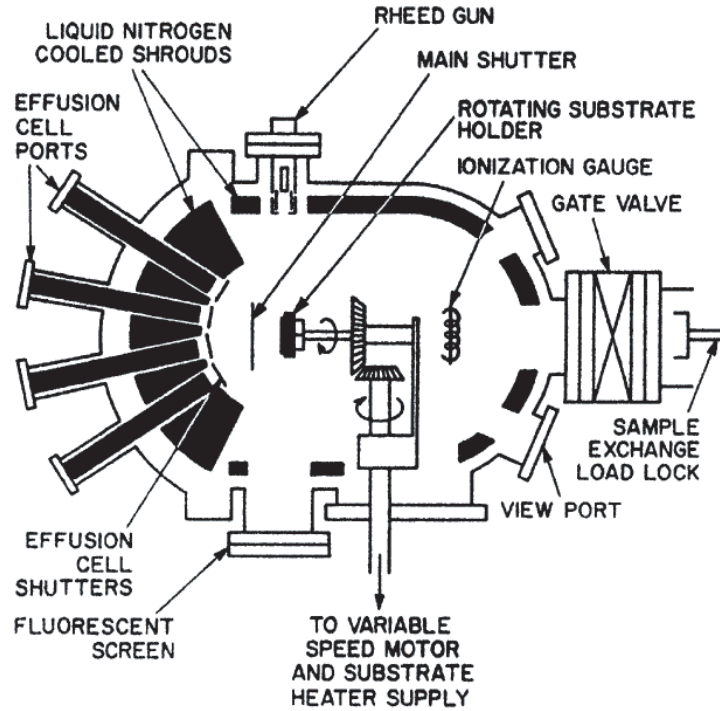


Figure 2.3: Scheme of a typical MBE system (after Ref.[37]).

As shown in Fig. 2.1, the three heterostructures (A,B and C) used in this thesis are similarly structured. Each layer has a well-defined function, that we detail hereafter, from the bottom to the top of the heterostructure. The growth of the heterostructure starts with the lattice-matched InAlAs buffer layer. This layer must have a high resistivity, to avoid current leakages, and must also prevent the migration of impurities from the InP substrate into the active layers. This goal is achieved by a control of the growth temperature: at first, a 100 nm-thick InAlAs layer is grown at 520°C , then 200 nm are grown at 420°C , and the remaining 100 nm are grown at 520°C . The part

of the buffer layer grown at lower temperature has a larger resistivity and avoids impurity segregation.

The role of the channel layer is to host the 2DEG, located at the interface with the spacer layer (situated above), due to the shape of the electron confining potential. As explained above (section 2.2.1), this layer is lattice-mismatched, so that its maximum thickness is limited. The spacer layer thickness L_s and the density of the δ -doping layer N_δ are critical factors as they strongly influence the electron density and mobility in the 2DEG. A large spacer thickness will increase the mobility but decrease the density of the 2DEG.¹ A too large N_δ must be avoided as a number of impurities are left non-ionized above some threshold, which may give rise to significant parallel conduction through this δ -doped layer (this may happen for $N_\delta \gtrsim 6 \times 10^{15} \text{m}^{-2}$ in our case). Note that N_δ and L_s are different in layers A and layers B, C.

Concerning the Schottky layer, particular care is taken to avoid the segregation of Si from the δ -doped layer. This is done by lowering the substrate temperature to 450°C during the growth of the first 2 nm of this layer. A metal layer can be deposited over this layer to serve as a gate, or it can be left in ambient air. Finally, the cap layer is a highly-doped InGaAs layer. Its role is essentially to help the formation of low-resistance ohmic contacts. It also serves as a protection against the surface oxydation.

The band structure profile along the direction perpendicular to the surface is shown on Fig. 2.4. This profile is a solution of the Poisson-Schrödinger equations. Note that strain was not taken into account in this calculation. The cap layer was not etched, contrary to the samples that are discussed in the next chapters. Removing the cap layer changes the surface potential, so that the shape of the whole band structure is altered. A metal layer on the top of the heterostructure also shifts the surface potential. This induces changes in the electron density and mobility in the 2DEG.

2.2.3 Electron beam lithography

Several steps are involved in Electron Beam Lithography (EBL). At first, a resist is deposited on the substrate by spinning. We employ the ‘standard’

¹The Si impurities in the δ -doped layer give their excess electrons to the channel layer so that a constant Fermi level is maintained throughout the structure. This results in a bending of the conduction band in the vicinity of the InGaAs/InAlAs interface (Fig. 2.4). This also leaves a layer of positively-charged impurities, which contribute to the scattering of the 2DEG electrons. Such a scattering obviously decreases with the distance L_s between the impurities and the 2DEG. An increased L_s also intuitively lower the probability for electrons to reach the channel layer, and therefore lower its density.

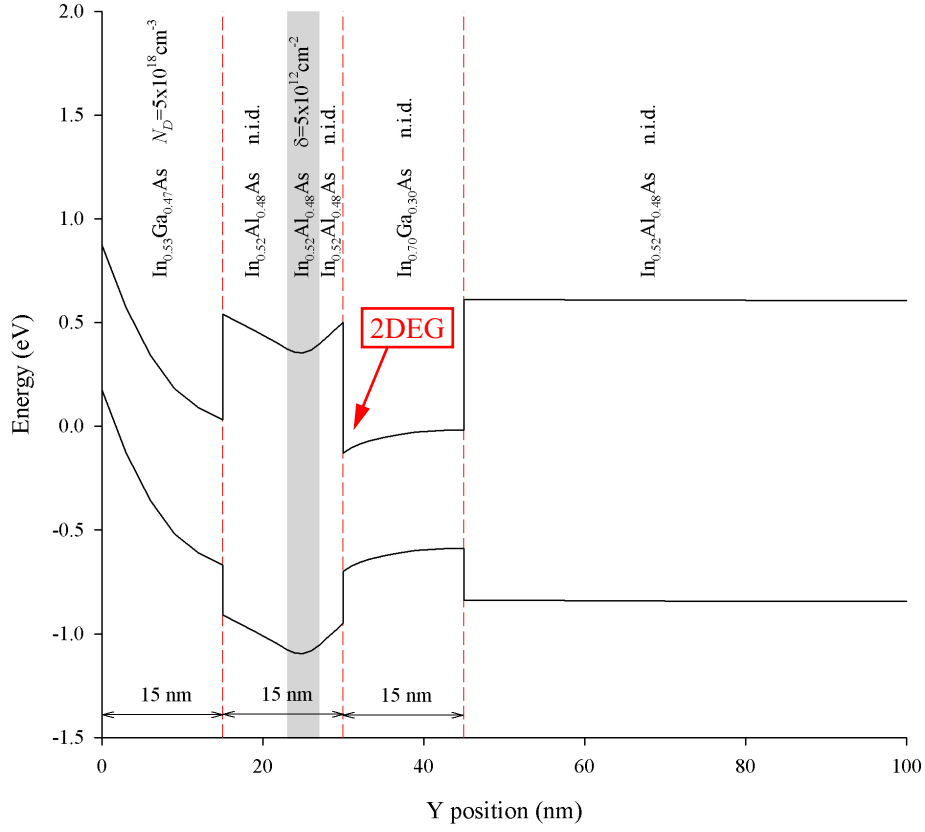


Figure 2.4: Illustration of the 2DEG confining potential profile in a $\text{In}_{0.70}\text{Ga}_{0.30}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ heterostructure along the direction perpendicular to the wafer surface. Upper and lower curves correspond to the bottom of the conduction band and the top of the valence band, respectively. The gray region is the δ -doped layer. Note that the cap layer is not removed. The calculation does not take into account the strain in the channel layer. [Courtesy of J. Mateos]

resist for EBL : poly-methyl-methacrylate (PMMA), diluted at 3 or 6 % in chlorobenzene. The thickness of the resist layer depends on its dilution, the length of the PMMA molecules (950 K), as well as on the spinning parameters; in our case, we always used a speed of 5000 rpm, an acceleration of 5000 rpm/s, a time of 60 s. With these parameters, we measured a thickness of ~ 150 and ~ 350 nm with the resist diluted at 3 and 6 %, respectively, after baking on a hot plate in order to evaporate the solvent. The choice of the dilution of the resist depends on the precision required for the lithography (precision is worse with the 6% PMMA, due to the thicker layer inducing a larger ‘proximity effect’, see below), but also on the process step following the EBL. If metal evaporation follows the EBL, the thickness of the resist layer must be significantly larger than the metal thickness; otherwise, the lift off is difficult. This imposes the choice of the 6%-diluted resist in the case of the ohmic contacts EBL and 3% for the wet etching EBL.

The principle of the exposure step of the EBL is very simple. PMMA is irradiated using the computer-controlled electron beam of a modified scanning electron microscope (SEM; a Philips XL30 SFEG in our case), which results in the scission of PMMA molecules. The fragmented polymeric chains are then more susceptible to dissolution in a methyl-isobutyl-ketone (MIBK) developer (step no. 9 in Table 2.2).

The modification of the SEM for its use as an EBL system consists in including a beam blanker, a control over the beam scanning system and (in our case) a laser interferometer system to control the X and Y position of the sample (a very complete discussion about EBL systems is given in Ref. [51])² The beam blanker is a pair of plates mounted in the column, on which a large potential difference can be quickly applied, in order to deflect the electron beam and to prevent it from reaching the sample. The computer control over the beam scanning system is provided through digital-to-analog converters (DACs), and allows to transfer a pattern drawn on a computer into the resist. This pattern is organized in a series of layers. Each layer is assigned to a specific step the process, and multiple layers are displayed as overlapping patterns (usually in different colors, see the example on Fig. 2.5). The layers are split apart into separate pattern files, each of them corresponding to specific exposure parameters.

The PMMA exposure itself is the most crucial step, and depends on several parameters. The most important one is the dose D_e , *i.e.* the charge deposited by the beam per unit area. The dose necessary to fully expose

²Freely available online at <http://www.cnf.cornell.edu/spiebook/TOC.HTM>.

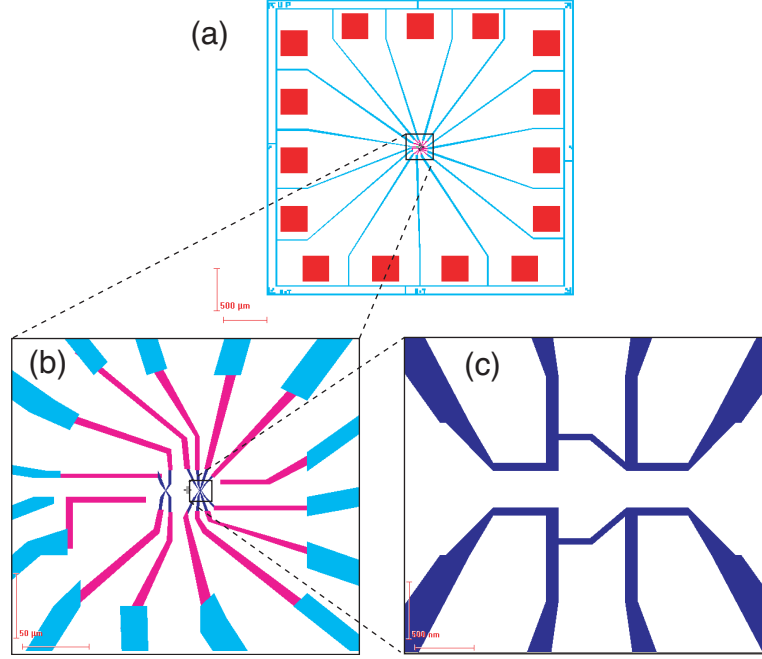


Figure 2.5: (a) General view of a whole ELPHY pattern for EBL. The size of the structure is 3.5×3.5 mm. Red boxes correspond to ohmic contacts, and all the other colors correspond to etched regions (including the alignment marks in the corners). The exposure parameters are specific for each colored layer. (b) Magnified view of the central part of the layout. (c) Detailed view of a quantum dot pattern.

our PMMA layers is typically $\sim 140 - 200$ and $200 - 240 \mu\text{Cb}/\text{cm}^2$ for the 3% and 6% PMMA, respectively. In practice, D_e depends on the electron beam current I , the area A of the elementary surface addressed by the control system, and the time t spent by the beam over each elementary surface, so that $D_e = It/A$. I , t and A are determined according to the specific features of the SEM (beam size, apertures, magnification, etc...), and of the control system (maximum frequency, DACs characteristics, ...). Moreover, as an effect of electron scattering in the PMMA, the dose delivered by the electron beam is not confined to the shapes that the beam writes, resulting in pattern-specific linewidth variations known as the ‘proximity effect’. A narrow line between two large exposed areas may receive so many scattered electrons that it can actually develop away while a small isolated feature may lose

so much of its dose due to scattering that it develops incompletely. This is why the doses given above are only indicative, and the common practice is to try on a dummy sample several doses for each pattern in order to find the best one. We give in table 2.3 typical exposure parameters that we used to expose fine patterns in a 3% PMMA resist, and to expose larger patterns (*e.g.* ohmic contacts) in 6% PMMA resist.

Table 2.3: EBL parameters for the exposure of a 3 % and 6 % PMMA resists spin-coated on an InGaAs substrate. The ‘Step’ is the distance between each elementary surface exposed by the SEM.

Dilution	Field size	Dose	Current	t	Step
3 %	43.7 μm	196 $\mu\text{Cb}/\text{cm}^2$	18 pA	1.72 μs	3.8 nm
6 %	216 μm	230 $\mu\text{Cb}/\text{cm}^2$	250 pA	2.15 μs	16.4 nm

Several successive EBL steps are involved in our process. To prevent misalignment between the different layers, each layer is aligned on the previous one using a procedure involving the recognition of marks written at a previous stage (these marks are visible in the corners of Fig. 2.5(a)). The success of this procedure relies on a precise positioning system, controlled by laser interferometers in our SEM. Such a system is also very useful in the case of very large patterns: these patterns are cut into smaller patterns, and the sample stage moves between the exposure of each pattern (‘stitch fields’ procedure).

2.2.4 Wet etching

Two different etching procedures are used in our process (steps no. 10 and 22 in Table 2.2). Both procedures are ‘wet’, *i.e.* the sample is soaked in an acid solution for a given time in controlled conditions, and then rinsed in water. We choose this technique rather than ‘dry’ etching techniques for two reasons. At first, wet etching is easy to implement and is fast. Secondly, as we began this work, we wanted to avoid any risk of deterioration of the 2DEG properties (in particular the mobility) at this stage. At that time, this was not guaranteed in the case of dry etching techniques.

The first etching procedure, referred to as ‘mesa etching’ is a deep etch: the material is removed down to the buffer layer. On the electrical point of view, the basic requirement of this etching procedure is to prevent any

leakage between the contacts, which would short-circuit the device. This is particularly critical in the case of devices with in-plane gates (see chapter 5), where voltages are applied accross narrow mesa ‘trenches’. In view of such configurations, we etch down to the buffer layer in order to maximize the electrical isolation (the buffer layer is the less conducting layer in our heterostructures). Moreover, this step is also crucial for the lateral definition of the geometry of the nano-devices used in this work.

The second etching procedure, referred to as ‘cap recess’ is a selective etch: the etching speed is much higher for InGaAs than for InAlAs. It is used to remove the top layer of the heterostructure after the thermal annealing of the ohmic contacts. This layer (the cap layer) is heavily doped, in order to decrease the electrical resistance of the ohmic contacts. It could therefore constitute a parasitic parallel conduction path for electrons if it were not removed.

The following subsections detail the etching parameters and their calibration, as well as some precautions that have to be taken before each etching process.

Mesa etching

All the etching processes are essentially characterized by their selectivity, their speed, and their anisotropy. Ideally, the mesa etching should be non-selective (*i.e.* the etching speed should be identical whatever the material in the heterostructure) and anisotropic (*i.e.*, in our case, the etching speed in the plane of the sample surface should be negligible compared to the etching speed perpendicular to the surface). Under these ‘ideal’ conditions, the etched profiles are very steep, and the pattern is very well transfered from the resist to the sample.

In the case of the mesa etching, we always used a solution based on orthophosphoric acid : $\text{H}_3\text{PO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ in volume ratios 5/1/40. We first calibrated the etching speed of this solution. We performed the calibration on four test samples. The solution was not shaken during the etching, and the etching depth d was measured by atomic force microscopy after resist removal. Fig. 2.6(a) shows d as a function of the time t in the solution. The etching depth increases linearly with the time in the solution in the investigated time range ($20 \text{ s} < t < 60 \text{ s}$) (*i.e.* the etching speed is constant). The best linear fit to our d vs t data is $d = 3t - 13$ ³ (with d in [nm] and t

³The presence of a constant term in the linear fit indicates that some time is needed to initiate the etching reaction (about 4 s; see the extrapolation of the linear fit on Fig. 2.6(a) down to $d = 0 \text{ nm}$), or to reach a constant etching speed.

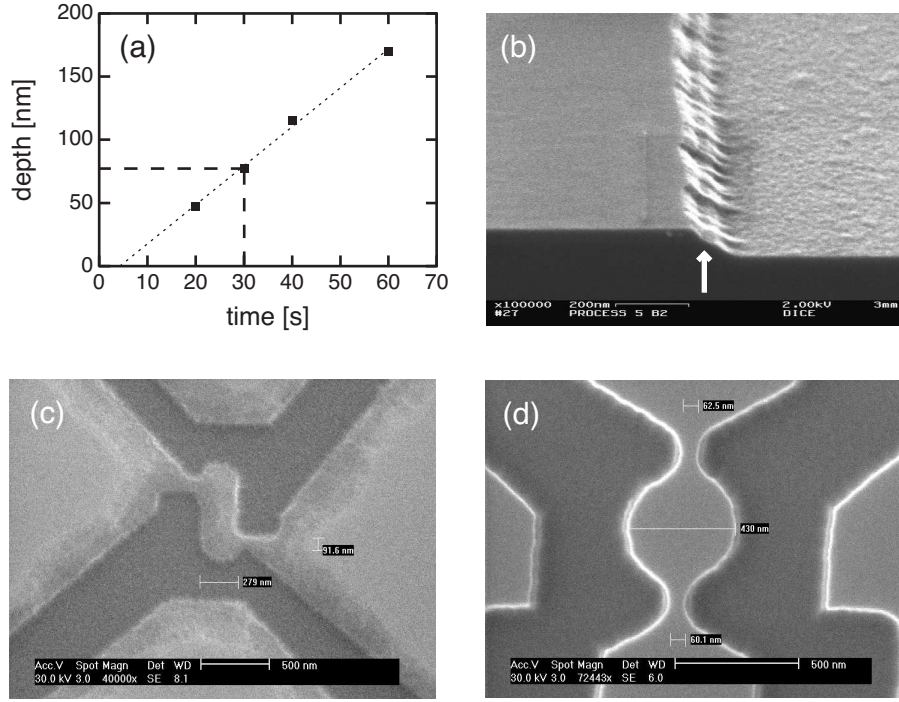


Figure 2.6: (a) Etching depth vs time. The dotted line is a linear fit to the data. Dashed lines indicate the parameters used in our process ($t=30$ s, $d \sim 75$ nm). (b) Micrography of an etching profile (the region at the right of the figure is etched). The sample has been etched for 30 s. (c) Micrography of an underetched sample. (d) Micrography (top view) of a properly etched sample.

in [s]).

Fig. 2.6(b) shows the etching profile obtained after soaking a sample for 30 s in the etching solution, and then removing the cap layer (see below), so that this profile is comparable to the profile of the measured samples. In this case, the direction of the crystallographic axis in the plane of the sample surface is unknown, but we did not observe any noticeable difference between profiles along different directions.

Two conclusions can be drawn from this figure. At first, the transition between the etched and non-etched regions is not steep at all. The surface corresponding to this transition makes an angle of $\sim 45^\circ$ with the sample surface plane. This means that the etching is almost isotropic. This must be

taken into account for the design of any device layout, and for the estimation of the final device size from top-views micrographs. Secondly, there is a discontinuity in the etching profile at a depth corresponding to the channel layer (pointed by the arrow on Fig. 2.6(b)). This effect is due to the selectivity of the solution used for the cap recess.

Finally, we want to emphasize that water molecules adsorbed on the sample surface have a dramatic influence on the final result of the mesa etching. Indeed, they cause a bad adhesion of the PMMA resist, so that the etching solution can penetrate below the resist. In such a case, etching occurs below the resist (underetching), and the pattern in the resist is poorly transferred on the sample. This is visible on Fig. 2.6(c), showing an electron micrograph of an underetched sample: the irregular dark ‘halo’ around the pattern edges is the underetched region, which extends hundreds of nanometers away from the original pattern edges in the resist. Fig. 2.6(c) can be compared with Fig. 2.6(d), showing the micrograph of a properly-etched sample: in this case, the edges are much sharper, so that the contrast of the micrograph is better. Underetching is avoided by drying the sample for (at least) 24h in an oven at 140°C and spin coating the sample directly (within ~ 20 s) after getting the sample out of the oven.

Cap recess

The goal of the second etching step of the process (step no. 22 in Table 2.2) is to remove the top layer of the heterostructure, made from heavily doped InGaAs, without altering the second layer (Schottky layer), made from InAlAs. The etching solution must therefore be highly selective. We used a solution of succinic acid (SA, $\text{HO}_2 - \text{CH}_2 - \text{CH}_2 - \text{CO}_2\text{H}$)/hydrogen peroxide (H_2O_2) in volume ratio 30/4. The succinic acid solution is obtained by dilution of granules in DI water. A complete dilution is only obtained by adding NH_4OH to the solution, which is also used to adjust the pH of the solution at 5. Using such a solution, one obtains an etching speed of 60 nm/min for InGaAs and less than 1 nm/min for InAlAs [56]. We used an etching time of one minute for all the samples, in order to ensure that the cap layer is etched, and that the InAlAs layer is not significantly affected.

Note that once the cap layer is removed, the InAlAs layer is exposed to ambient air, and oxidizes with time. This has an effect on the transport properties of the devices, due to changes of the surface potential. We observed a significative increase of the devices’ resistances over time scales of ~ 1 year.

It is also important to notice that the cap recess is done after the mesa

etching. This has an influence on the etching profile at the level of the channel as shown on Fig. 2.6(b). Indeed, as the channel is made from InGaAs, it is etched by the succinic acid solution. However, the etching speed of this layer is not equal to the etching speed of the cap layer: both the In content and the etching conditions are very different in both layers. This lateral etching can be used to avoid electrical contact between the channel and a metallic gate deposited over the structure [15], as in the case of sample B₁. In samples where the cap recess was done before the mesa etching, we always measured a leakage current between the gate and the 2DEG at room temperature, and significant leakages at low temperature, preventing any reliable measurements.

2.2.5 Ohmic contacts

In principle, an ohmic contact is a metal-semiconductor junction with a linear $I - V$ characteristic for both current directions. The contact is usually acceptable if it can supply the required current density with a voltage drop that is very small (negligible) compared to the drop across the active region of the device. Other requirements include good adhesion to the semiconductor, ability to bond gold wires to connect the device to external circuitry and finally contact reliability.

The practical ohmic contact system consists of an adhesion layer, followed by a dopant layer, which will diffuse into the semiconductor during a rapid thermal annealing, and finally a thick layer of Au for bonding purposes. The theory of the formation of these contacts is out of the scope of the present work: as we use a four contacts technique to measure the electrical properties of our devices, the contact resistances play no role as long as they are small compared to the devices' resistances. No further optimization of these resistances is required once this objective is achieved. We will therefore only concentrate on some practical aspects of ohmic contacts on our InGaAs samples. For further informations, we refer to Ref. [156].

We used the following sequence of metal layers for our ohmic contacts: Ni (2.5 nm)/ Ge (40 nm)/ Au (80 nm)/ Ni (5 nm)/ Au (30-60 nm). Very schematically, the bottom layer, Ni, favors the adhesion of the contact, Ge is the dopant, and Au is added for bonding purposes, as well as to prevent oxydation, which would alter the contact reliability. The Ni layer inserted between the two gold layers serves as a diffusion barrier : it ensures that the topmost layer is made of pure Au, without any diffusion of Ge. Practically, we use an electron beam evaporator to grow this layer sequence in a high vacuum ($\sim 10^{-6}$ mbar), with a precise control over the layer thickness.

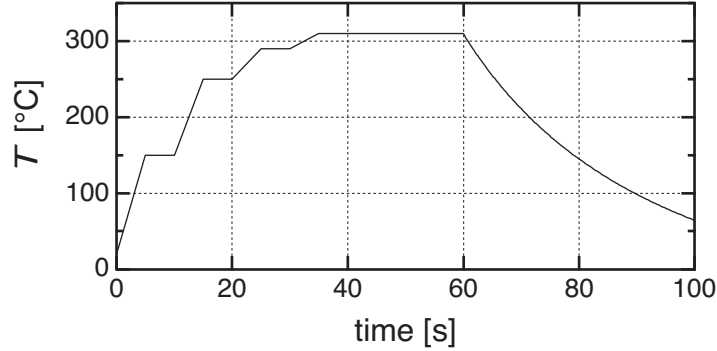


Figure 2.7: Temperature cycle for the rapid thermal annealing of InGaAs samples.

After the metal deposition, the next step is the lift-off (step no. 20 in Table 2.2). In this procedure, a solvent (acetone) is used to dissolve the PMMA resist, leaving only the metal that is in contact with the wafer. Unlike the etching, the lift-off procedure is highly sensitive to the edge profile of the patterned resist, and to its thickness. An undercut resist profile and a resist thickness of about two times the metal thickness ease the lift-off process as, in these conditions, one obtains a clean break between the metal on the resist and the metal that goes through the openings. As the ohmic contacts are $\sim 150\text{-}200$ nm thick and the 6% PMMA resist is ~ 350 nm thick in our process, the lift-off is not difficult, and ultrasound is often not necessary.

Once the resist is removed, and metal only remains at the desired places, the sample undergoes a thermal treatment (Rapid Thermal Annealing, or RTA; step no. 21 in Table 2.2) in order to diffuse the dopant to form the ohmic contacts. RTA, as the name implies involves a fast heating and cooling, which is performed in a small chamber heated by flash lamps, in a $\text{N}_2(95\%)/\text{H}_2(5\%)$ atmosphere. The temperature is monitored by a thermocouple positioned close to the sample. The complete temperature cycle for our RTA is shown on Fig. 2.7. Such a process results in a roughening of the Ohmic contact surface, visible with an optical microscope.

We have checked that ohmic contacts produced in the conditions described above have a linear $I - V$ characteristic in the voltage range used for the conductance measurements on quantum dots (chapter 3). We can only speculate about the behavior of our ohmic contacts up to the voltages

used in chapter 5. However the influence of any nonlinearity of the ohmic contacts on the measurements presented in chapter 5 should be very limited for two reasons: (1) all our measurements are performed in the 4-contacts configuration, so that the contribution of the contact resistances is removed in the measurements; (2) the resistances of the contacts (typically 0.15 - 0.25 Ω .mm) is negligible compared to the resistance of the devices.

2.2.6 Metal Gates

The process to deposit a metal gate is almost identical to the ohmic contacts process: an e-beam lithography on a thick resist, followed by metal evaporation (5 nm Ni and 100 nm Au) and finally a lift-off. Metal gates were only seldom used in this work: we noticed that current leaks between the top gate and the 2DEG already appeared for small bias voltages (below $V \sim -0.7$ V, *i.e.* too low to deplete the 2DEG underneath, or above ~ 0.5 V). Therefore, we never used voltages beyond that range. The reason for these leaks is not completely understood, but we suspect that lateral contacts between the metal gate and the 2DEG may explain our observations.

2.2.7 Bonding

The bonding of InGaAs devices is not as critical as for Bi nanodevices (see section 2.3.3). The sample is glued with vacuum grease on an epoxy sample holder. Then gold wires are connected both to the ohmic contact paths on the sample and to the metallic pins of the sample holder using silver paint or silver epoxy. In the case of silver epoxy, the sample is put in an oven at 140°C for one hour in order to evaporate the solvent.

2.3 Bi samples

2.3.1 Bulk Bi properties (overview)

The main properties of Bi have been reviewed by several authors. Here, we only present some of them, which will be useful for our data analysis (more information can be found in Ref. [88]). Bi belongs to column V of the Mendeleev periodic table. It shares some physical properties with metals (*e.g.* its electrical conductivity decreases when the temperature decreases), and some others with semiconductors (*e.g.* the carrier density increases with the temperature). As it could not be classified with metals or semiconductors, it was named ‘semimetal’ along with some other materials with

complex properties, such as Sb and As. A big part of the complexity of bismuth properties, including their strong anisotropy, stems from its rhombohedral crystal lattice, which can also be viewed as a cubic lattice slightly strained along its diagonal [118, 88]. The Brillouin zone of Bi, shown on Fig. 2.8 is therefore close to that of a FCC lattice. However, contrary to the FCC Brillouin zone which has eight equivalent hexagonal sides, the Bi Brillouin zone has only two truly hexagonal sides (corresponding to the trigonal axis), the other ones being only ‘pseudo-hexagonal’.

Fig. 2.8 shows the location of the electron and hole pockets in the Brillouin zone. Isoenergetic surfaces are highly anisotropic ellipsoids, which do not have all their principal axis along the symmetry axis of the Brillouin zone in the case of electron pockets (contrary to hole pockets). These energy surfaces in k space can be described by the following relation :

$$E(\mathbf{k}) = (\hbar^2/2m_0)\mathbf{k}m^{-1}\mathbf{k}, \quad (2.5)$$

where E is the energy, $\mathbf{k}$ is a wavevector, and m^{-1} the (dimensionless) reciprocal effective mass tensor of Bi, for electrons or for holes. If the principal axes of the carrier ellipsoids are chosen as the reference frame for m^{-1} , one has :

$$m^{-1} = \begin{pmatrix} m_1 & 0 & 0 \\ 0 & m_2 & 0 \\ 0 & 0 & m_3 \end{pmatrix}^{-1}, \quad (2.6)$$

where $m_1 = 0.00119$, $m_2 = 0.266$ and $m_3 = 0.00228$ in the case of electrons and $m_1 = m_2 = 0.064$ and $m_3 = 0.69$ in the case of holes (data from ref. [88]; note that there are some significant variations among the values given in the literature). Expressing (2.6) in another reference frame requires to rotate it, knowing that the tilt angle of the electron ellipsoid axes with respect to the crystallographic reference frame is $\sim 6^\circ$, and that the ellipsoids are related by inversion through the Brillouin zone center and by rotation of $\pm 120^\circ$ about the trigonal direction.

The lattice distortion is responsible for a very small energy overlap between the L -point conduction band and the T -point valence band, shown on Fig. 2.8. In bulk Bi, the Fermi level goes through these two bands, in such a way that they are populated by an equal number of electrons and holes (charge neutrality condition; in bulk Bi, $E_F = 27.6$ meV). The direct band gap at the L -point is very small ($E_g = 13.6$ meV). The strong coupling between the L -point bands gives rise to a non-parabolicity of these bands

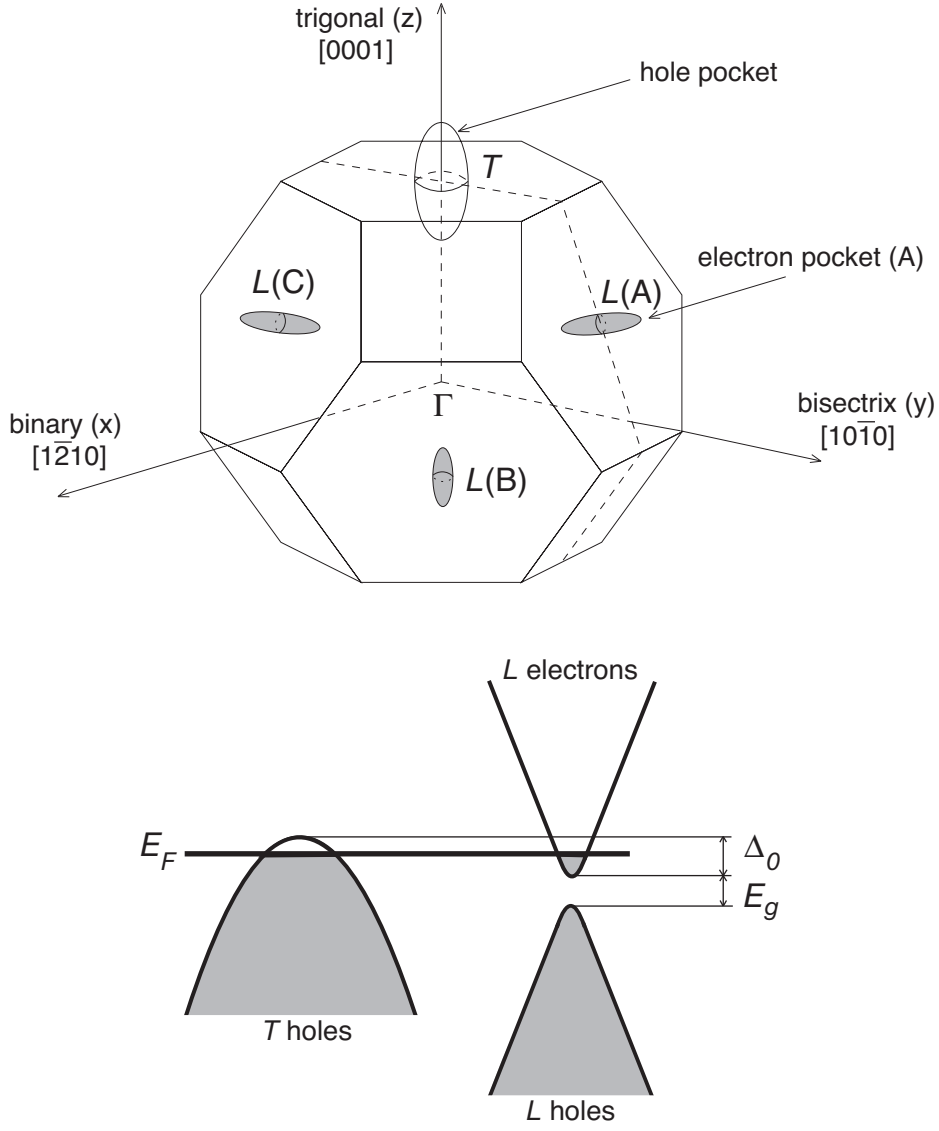


Figure 2.8: Top: The Brillouin zone of Bi, with the Fermi surfaces of electron pockets at L -points (shaded areas; only 3 among 6 are shown) and the hole pocket at T -point (adapted from Ref. [43]). Bottom: schematic representation of the energy band structure of Bi at the L -point and at the T -point. The direct energy gap between L -point electrons and L -point holes is $E_g = 13.6$ meV at $T = 0$ K and the band overlap of the L -point conduction band and the T -point valence band is $\Delta_0 = -38$ meV.

(they are only parabolic very close to the band edge, see Fig. 2.8). Therefore, the effective masses change with the energy of the carriers, according to the following relation ('Lax model') :

$$m_i^*(E) = m_i(1 + 2E/E_g), \quad (2.7)$$

where m_i ($i = 1..3$) are the electron effective masses at the bottom of the band (given above), and m_i^* are the corrected effective masses. The dispersion relation at L -point must also be corrected, and becomes:

$$E(\mathbf{k}) = \pm \frac{1}{2}[E_g^2 + 2E_g(\hbar^2/m_0)\mathbf{k}\mathbf{m}^{-1}\mathbf{k}]^{1/2} - \frac{1}{2}E_g, \quad (2.8)$$

where $\mathbf{m}^{-1}$ is the reciprocal effective mass tensor *at the bottom of the band*. Note that Equ. (2.8) still represents ellipsoids in k space.

All the values of band parameters given above are for $T = 0$ K. As T increases, thermal expansion slightly changes the lattice constant, which significantly affects the band parameters. The effective masses of the electrons and holes at finite temperature are given by [153]:

$$m_i(T) = \frac{m_i}{1 - (2.94 \times 10^{-3})T + (5.56 \times 10^{-7})T^2}, \quad (2.9)$$

and the direct bandgap follows the relation [153]:

$$E_g = 13.6 + (2.1 \times 10^{-3})T + (2.5 \times 10^{-4})T^2 \text{ [meV]} \quad (2.10)$$

These temperature dependences are relatively weak below liquid nitrogen temperature, and much stronger at higher temperatures.

2.3.2 Bi films growth

The first step in the fabrication of Bi nanodevices is the growth of good quality Bi films. The substrate consists of a Si 2" wafer (330 μ m-thick), covered with a 100 nm-thick SiO₂ layer, to prevent electrical leakages. After standard cleaning of the Si wafer (acetone-methanol-water), deposition of the high purity Bi film is carried out in an e-beam evaporation system (the purity of the Bi source is 99.9999%, and is even better in the film due to the evaporation process). The deposition rate is ~ 0.1 nm/s and the residual pressure in the chamber during the growth is $\sim 2\text{-}3 \times 10^{-6}$ mbar. The film thickness was measured during the growth using a quartz-based measurement system, and was then recalibrated using SEM images of cross-sections of the films. Films grown using this technique are polycrystalline,

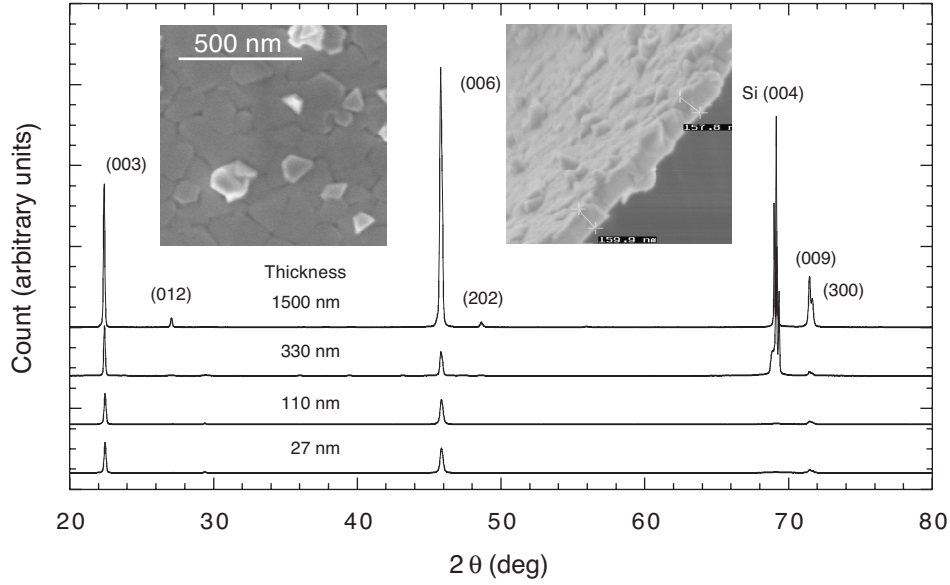


Figure 2.9: X-ray diffraction spectra of Bi films. The film thickness is indicated above each trace. The insets show a SEM micrograph of a 160 nm-thick Bi film (the left inset is a top view and the right inset is a cross-sectional view).

with typical lateral crystallites dimension of ~ 100 nm (as shown in the inset of Fig. 2.9). Fig. 2.9 also shows X-ray diffraction spectra of films of various thicknesses, obtained with a Siemens D500 diffractometer⁴ ($K_{\alpha} = 1.5418\text{\AA}$). The (003), (006) and (009) peaks of Bi are clearly visible in all the spectra, together with the (004) peak of silicon at $\theta = 69.11^{\circ}$. This indicates that all Bi crystallites in the films have a very strong preferred orientation: their trigonal axis is perpendicular to the substrate.

Our final objective was to obtain single crystalline nanodevices. We therefore tried to increase the crystallites lateral sizes in the films using two different methods, based on thermal treatments taking place either during the film growth (evaporation on heated substrate) or after the film growth (annealing). This required the fabrication of an annealing furnace and the modification of the e-beam evaporator.⁵

⁴These spectra, as well as the polar figures (Fig. 2.10) were measured by Prof. B. Lenoir at the 'Ecole des Mines de Nancy'.

⁵This was done at UCL by Dr. J. P. Minet as well as the work on the annealing

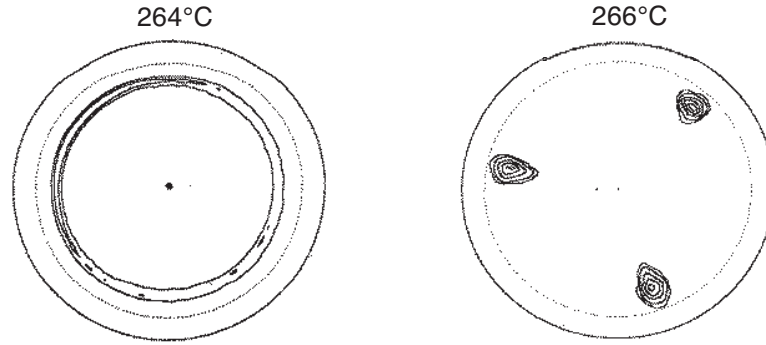


Figure 2.10: X-ray pole figure of one of the threefold-symmetry peaks of Bi films annealed at 264°C and 266°C. The radial direction is the tilt angle θ between the normal direction of the film and the diffraction plane, and the angular direction is the rotating angle.

At first, we briefly present the results of the annealing technique. This treatment was inspired by the work of Yang and coworkers on the annealing of 1-10 μm -thick electrodeposited Bi films [157]. The annealing system consists of a cylindrical copper block, ensuring isothermal conditions in the chamber hosting the samples. The copper piece is inserted in a heating element, which is itself contained in a vacuum chamber (pressure $< 10^{-1}$ mbar). Thermal treatment consisted in a temperature ramp up to 230°C at 20°C/min, followed by a ramp to 264°C at 1.2°C/min, and a final slow ramp of 0.3°C/min up to 266°C. Note that this temperature is very close to the Bi melting temperature (272°C).

Films of various thicknesses were annealed using such a method. Small angle X-ray diffraction was used to fully characterize the film texture. X-Ray diffraction polar figures are shown on Fig. 2.10 for two different films, annealed during 24 hours at 264°C and 266°C. Below 264°C, the polar figure is essentially isotropic with respect to the angular direction, indicating that there is no preferred crystal orientation in the plane of the film. Interestingly, it was found that there is a critical temperature, between 264°C and 266°C, at which all the grains get organized and adopt the same orientation in the plane of the film. This is demonstrated by the threefold symmetry of the polar figure (Fig. 2.10) at 266°C. This observation is in agreement with the report by Yang and coworkers [157]. This improvement of the crystallinity

treatment.

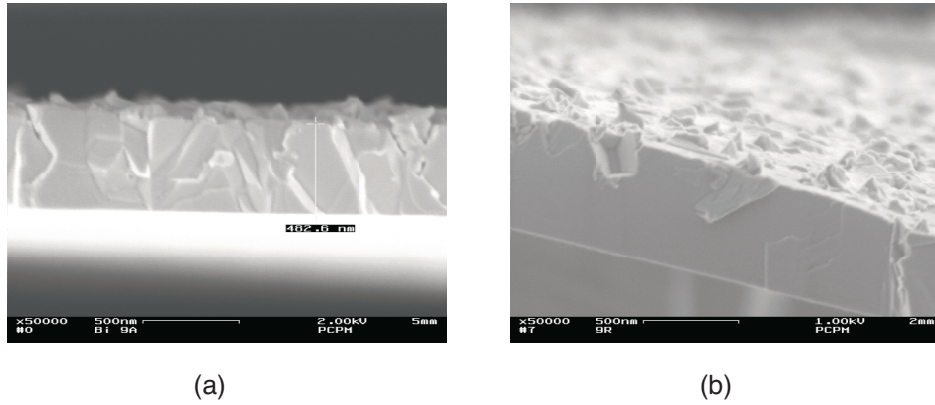


Figure 2.11: SEM micrographs of cross-sections of 500-nm thick Bi films before (a) and after (b) annealing at 266°C.

is also clearly visible on Fig. 2.11, showing cross-sectional SEM micrographs of a 500 nm-thick film before and after annealing at 266°C. Despite this improvement, it is clear from Fig. 2.11 that annealing does not decrease the roughness of the top surface of the film. Moreover, we observed that very thin films (thickness below 200 to 300 nm),⁶ of major importance in view of the measurements of quantum or size effects, tend to coalesce at this annealing temperature.

The drawbacks of the annealing method lead us to consider an alternative method to improve the crystal quality of our films. In this case, the Si/SiO₂ substrates were heated during the film growth. A heating system was fitted in a small vacuum chamber mounted on the main evaporator chamber through a gate valve. Figure 2.12 shows a global view of the system. The heater consists of a 2' diameter copper block, in which two heating cartridges are fitted. A first thermocouple for regulating the temperature is positioned between the two heating elements, while a second thermocouple, measuring the sample temperature, is anchored 1 mm below the heater surface. In steady state conditions, the temperature difference observed between the two thermocouples is less than 0.5°C. Standard 2' silicon wafers, used as sample holders for spin coating and e-beam lithography, can be clamped on the heater surface by means of an external ring. Figure 2.12 shows the sample holder with the silicon wafer fixing ring.

The benefit of heating the substrate during the film growth is illustrated

⁶ *i.e.* films behaving in a 2D manner; see Fig. 1.10(b).

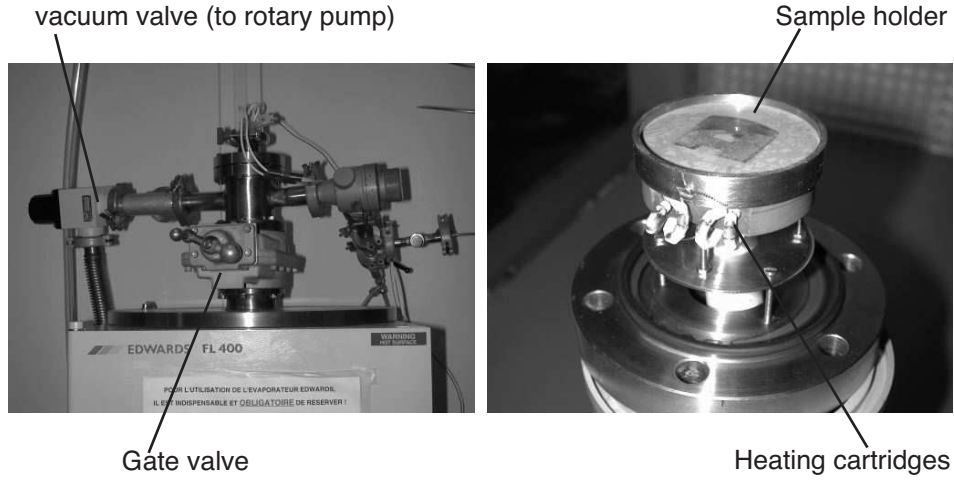


Figure 2.12: Left: heating system mounted on the top of the main evaporator chamber. Right: sample holder, fitting inside the vacuum chamber shown on the left figure.

in Figure 2.13. The film deposited at 100°C [Fig. 2.13(b)] shows a larger grain size compared to films deposited at room temperature [Fig. 2.13(a)]. When the substrate is heated above 100°C , if the evaporation conditions are unchanged, bismuth condensates in the form of spheres, which are not electrically connected, as shown on Fig. 2.14. However, films can be grown at higher substrate temperature using a two-steps method. First, the substrate temperature is set to 70°C and a 30 nm-thick Bi layer is deposited. Then, the substrate temperature is raised to 150°C and a 50 nm-thick bismuth layer is deposited. The film has a crystallite mean lateral size of ~ 500 nm, as shown on Fig. 2.13(c), with a much smoother surface than films grown at room temperature. We adopted this two-steps technique for the growth of the films used to fabricate the Bi cavities, presented hereafter. No annealing was performed after the film growth (due to the above-mentioned coalescence problem).

2.3.3 Bi nanocavity fabrication

A relatively small number of process steps are required to produce a Bi nanocavity (Table 2.4). For example, no ohmic contact lithography and evaporation was required: the Bi film was directly contacted to the gold

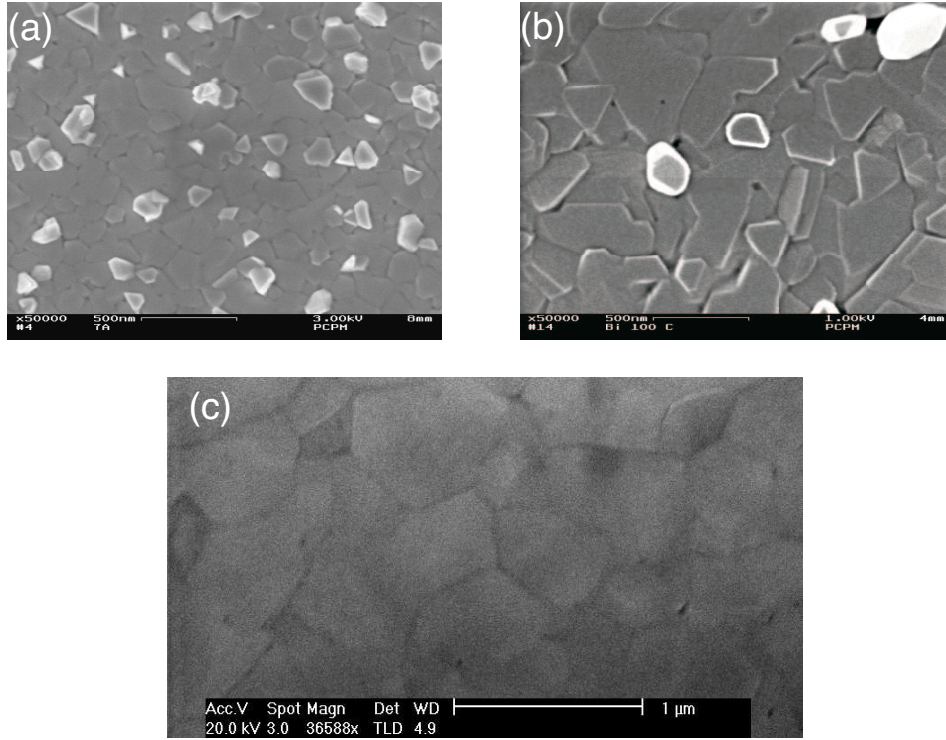


Figure 2.13: SEM micrograph of a Bi film grown on (a) a non-heated Si/SiO₂ substrate, (b) a substrate at a temperature of 100°C (the thicknesses of both films are similar). (c) SEM micrograph of a Bi film grown using the two-steps method (see text). Note that all micrographs have the same scale.

wires. However, almost each step in Table 2.4 brings its own difficulties. The Bi film growth process has already been described above. It was only slightly modified in view of the fabrication of the nanodevice : instead of evaporating over the whole surface of a Si piece, the evaporation was done through a shadow mask, which consisted of a small metal piece with three ~ 1 mm diameter holes. This allowed us to restrict the total area that had to be exposed by the electron beam. The specific aspects of the ‘Bi nanocavity process’ are discussed in the following sections.

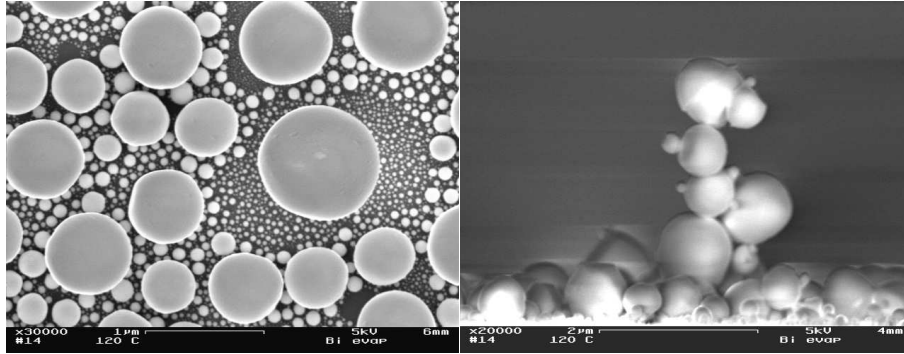


Figure 2.14: Left: top view of Bi spheres obtained on a Si/SiO₂ substrate heated at 120°. Right: side view of connected Bi spheres formed in the same conditions (both are SEM micrographs).

Table 2.4: Standard process sheet for Bi nanodevices fabrication.

Step	Description	Parameters
1	Si wafer oxydation	oxyde thickness : 100 nm
2	Si wafer cutting	size: $\sim 8 \times 4mm$
3	Standard cleaning	
4	Bi film growth	see section 2.3.2
5	glueing on 2" Si wafer	glue : carbon paint
6	baking on hot plate	100°C - 5 min
7	SEM observation	see below
7	resist spin coating	PMMA 6% in chlorobenzene 5000 rpm; 5000 rpm/s; 60 s
8	resist baking (hot plate)	150°C - 5 min
9	SEM lithography (mesa)	see below
10	resist development	MIBK:Isopropanol (3:1) 90 s - Isopropanol 20 s - DI water 10 min
10	plasma etching	see below

Continued on next page

Step	Description	Parameters
11	resist removal	cold acetone 10 min
12	bonding	see below

Electron beam lithography

The electron beam lithography process on Bi films is very similar to the procedure for InGaAs samples, described in section 2.2.3, except for several details. At first, on each Si piece, three Bi disks are evaporated through a shadow mask. On each of these disks, a device with four contacts will be defined by etching.⁷ This requires to locate approximately the center of each Bi disk before the beginning of the lithography. Moreover, we want to make sure that our cavity is etched in a single Bi grain. In order to achieve this, we find a large enough Bi crystallite on each Bi disk. This is done before spin-coating the resist. The position of the crystallite is determined with respect to three or four points of reference on the sample. After the resist spin-coating, the points of references are located again, and the SEM stage is blindly moved so that the center of the exposure field matches the position of the large crystallite. After the alignment, the smallest field is exposed (magnification: $\times 2000$, *i.e.* a $43.4 \times 43.4 \mu\text{m}$ square). Then, the SEM magnification is changed to $\times 400$ without moving the stage and the intermediate field is exposed. Finally, the last step consists in defining large contact pads at the edges of the Bi disks. This is done at a SEM magnification of $\times 100$.

Care must be taken to prevent the small Bi devices to be burned out by unwanted electrical currents, arising from static discharges. This point is critical here: Bi has a low melting point temperature (271°C), so that even small discharges can damage our devices. To prevent this from happening, we have included *on-wafer* shorts between the contact pads, consisting of thin Bi conducting strips running along the perimeter of the pattern, as shown on the EBL pattern on Fig. 2.15(a).

Plasma etching

In a first step, the plasma etching parameters have been explored on 80 nm-thick Bi films deposited at room temperature. We used an Electrotech

⁷Note that the contact electrodes are in Bi. Contrary to semiconductor samples, there is indeed no need to deposit another metal layer on the Bi film to decrease the contact resistance.

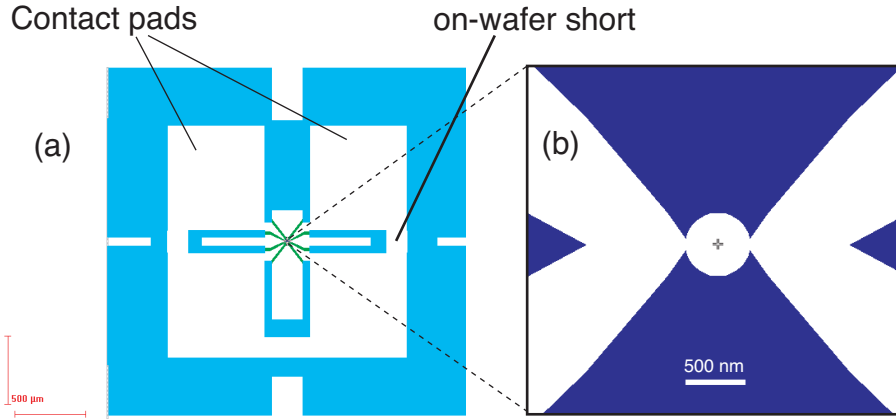


Figure 2.15: EBL pattern for a Bi nanocavity. (a) large-scale view. (b) small-scale view. This pattern has been used to fabricate the samples shown on Fig. 2.16(a-b).

RD600 plasma etcher, applying 40 W power (for a 3" chamber diameter), and a mixture of Cl_2/He in a ratio 8:3 at 65 mTorr. A similar recipe (BCl_3/Ar ; 20 mTorr; 200 W; etching rate: 100 nm/min) was used by Il'in and coworkers [87] to etch thin Bi films. Figures 2.16(a) and (b) show SEM micrographs of films etched during 1'30" and 2'30". While the etch is incomplete after 1'30", the etching profile is very sharp after 2'30". One also observes in Figure 2.16(a) that plasma etching is anisotropic and depends on grain boundaries and film morphology. In the above-mentioned conditions, we noted that some unexposed PMMA was always remaining, even after 4' of plasma treatment (overetching conditions). This ensures that the part of the film covered by the PMMA is not modified by the plasma treatment.

Bi sample bonding

As explained in section 2.3.3, unwanted electrical currents can damage our samples, as shown on Fig. 2.16(c). We have therefore adopted a particular bonding technique to prevent this from happening. At first, a long gold wire is soldered on the sample holder, so that all its electrical contacts are shorted. The sample is glued on the sample holder using vacuum grease (so that it can be easily removed from its holder after the measurement). Then we can connect thin gold wires between the sample bonding pads and on the

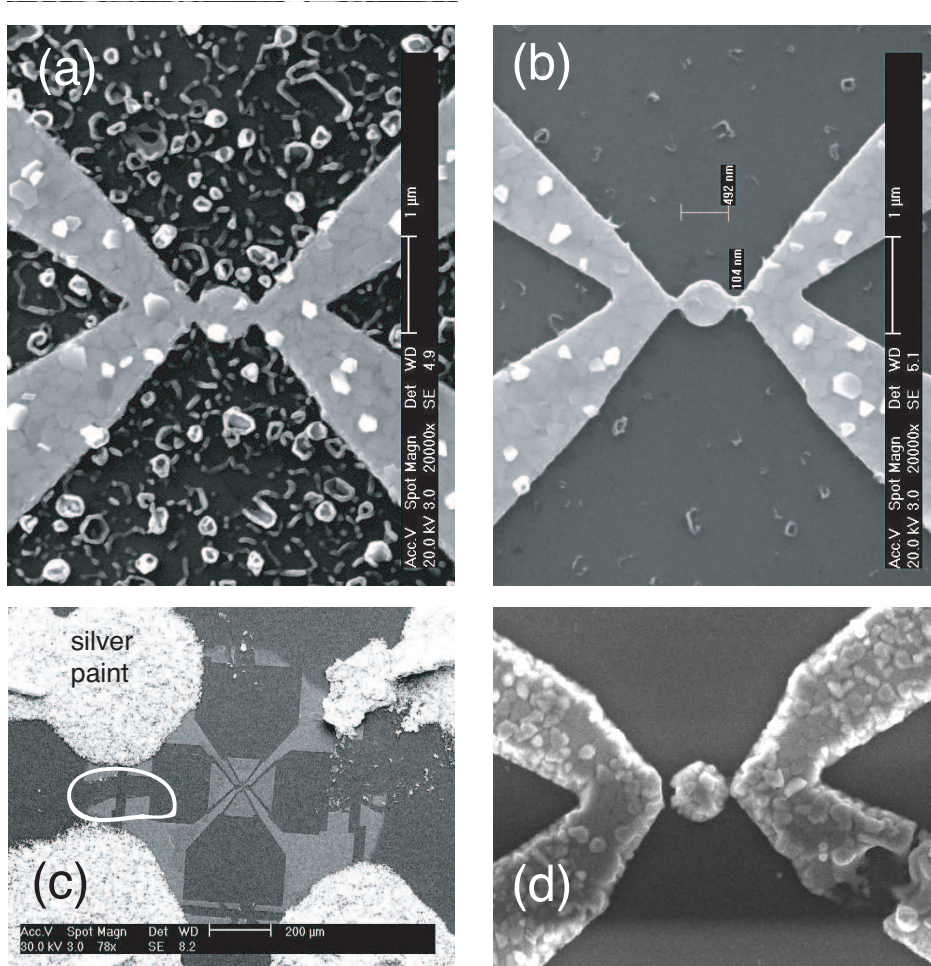


Figure 2.16: SEM micrograph of Bi films plasma etched during (a) 1'30" and (b) 2'30". (c) SEM micrograph of a Bi sample, with bonding wires attached with silver paint. One of the marks of the scribing tool is encircled. The device is at the center. (d) SEM micrograph of a sample damaged by static discharges during the bonding.

sample holder contacts by depositing silver paint.⁸ The contact resistance was always found negligible with respect to the resistance of the samples. Once this is done, the contacts are shorted twice. It is therefore safe to remove the on-wafer shorts, using a diamond scribe. A SEM picture of a scribed sample is shown Fig. 2.16(c). The sample holder is then mounted on the measurement system (after grounding all the connections to the sample), and the wire shorting the contacts on the sample holder is cut before the measurements. After the measurements and before removing the sample from the measurement system, a new wire is soldered in order to short all the contacts on the sample holder.

When a Bi sample is finished and bonded, it must be measured as quickly as possible, because oxydation takes place, and may change the actual size of the device. This is of course particularly critical in samples with very small cross-section, such as nanowires (a 7 nm-thick oxyde was observed on Bi wires in ref. [43]). We noticed that our Bi cavity samples became insulating due to oxydation 8-12 months after their fabrication.

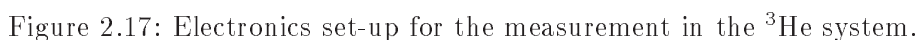
2.4 Measurement techniques

A schematic view of the whole magnetoconductance measurement system is shown in Fig. 2.17. Part of the system is dedicated to the production of cryogenic temperatures, necessary to reach the ballistic and phase coherent regime in our samples. It is composed of a commercial ³He cryostat with some control electronics. Its working principle is briefly described in section 2.4.1, as well as the practical methods to maintain constant temperatures in various operating regimes. The other part of the system allows to perform the electrical measurements on the samples. The measurement parameters are discussed in section 2.4.2.

2.4.1 Low-temperature ³He system

Producing low temperatures using ³He relies on the variation of the vapour pressure of ³He with temperature. The principle is simply to lower the vapour pressure above a liquid ³He bath, so that the bath temperature will ultimately reach ~ 0.25 - 0.3 K. In practice, this is done in a two-steps cycle: ³He is first condensed and then pumped. Condensing ³He is realized along a surface cooled at ~ 1.5 - 2 K. This temperature is obtained by lowering the

⁸The tweezers used to manipulate the gold wires are grounded and connected to the sample holder's contact pads.



vapour pressure inside a small chamber containing liquid ^4He (the ‘1K pot’) using a rotary pump. The 1K pot also limits thermal transfer between the sample and the upper (hotter) part of the cryostat. Once a sufficient amount of ^3He is condensed at the bottom of the system, the second step can begin. Lowering the vapour pressure over the ^3He bath is achieved using a sorption (or ‘sorb’) pump, which adsorbs ^3He at its surface when it is cooled down to 4.2 K, and maintains a ^3He vapour pressure of $\sim 10^{-3}\text{mbar}$. When all the liquid ^3He is evaporated and adsorbed at the surface of the sorb pump, the temperature rises in the sample chamber. The sorb pump is then heated up to $T = 30\text{K}$ so that it releases its adsorbed ^3He , which can be condensed again. The temperatures of the sorb pump and the 1K pot are measured using carbon glass resistors, and continuously monitored. The duration of the pumping cycle (*i.e.* the time during which the sample can be maintained at the base temperature) is $\sim 12 - 24$ hours, depending on the amount of condensed ^3He , of the type of measurements (fast B -sweeps, regulation at intermediate temperatures).

2.4.2 Transport measurements

The transport measurements presented here are performed using a four-wires lock-in technique (the wires for the resistance measurements are shown in pink and blue on Fig. 2.17). We apply a low frequency (in the range $\sim 3\text{--}20$ Hz) ac current through the sample using two ohmic contacts, and detect the ac voltage across the device using two different ohmic contacts, at the same frequency as the input current frequency. We use a bandpass filtering of the measured voltage around this frequency, provided by the lock-in. Additional filtering is also provided by pi filters (from RS components, 5000 pF) at the top of the cryostat.

It is important to keep the bias V across the device as small as possible in order to avoid unwanted heating effects (otherwise, higher energy states become accessible to electrons). One of the conditions to fulfill is therefore $eV \ll k_B T$;⁹ as an example at $T = 300$ mK, this corresponds to $V \ll 25\mu\text{V}$. In practice, at the beginning of a measurement campaign, we measure G vs B for several values of the input current, and choose the value of the current such that: (i) the measured voltage depends linearly on the current (ohmic regime); (ii) the amplitude of UCFs does not depend on the current around the chosen value; (iii) the noise level is acceptable¹⁰ (the intrinsic noise level of our measurement system is $\sim 20\text{--}40$ nV in the best conditions).

The magnetic field (up to 9 T) is obtained by applying a current in a superconducting solenoid cooled down to 4.2 K.¹¹ In our case, sweeping the magnetic field is usually done at a very low speed ($\sim 0.001\text{--}0.1$ T/min), due to the rich pattern of UCFs that must be accurately determined. Several sweeps at different speeds are performed to adjust this rate. Note that after the adjustment of the current and of the B -sweeping speed, we often observed that the sample needed to be ‘stabilized’, as slight changes occur in the magnetoconductance curves during the first days of measurements, probably due to a relaxation of some impurities in the substrate.

The sample temperature T is adjusted between 0.3 K and 1.8 K by regulating the temperature of the sorb pump, and hence the ^3He vapour pressure in the chamber. We use a heating resistor to reach and regulate at temperatures above 1.8 K. T is measured by two different calibrated sensors - RuO_2 and carbon glass resistors, depending on the temperature range.

⁹This does not *necessarily* guarantees that heating effects are avoided.

¹⁰In our measurement configuration, the noise can be easily detected since magnetoresistance or magnetoconductance curves are symmetric with respect to $B = 0$ T.

¹¹The magnetic field is deduced from the current in the solenoid. The error over B increases around $B = 0$ T, due to the hysteresis of the solenoid. In critical cases, the magnetic field is measured from a Hall sensor patterned next to the sample.

Small differences between the sample and the thermometer temperature can be observed, as they are positioned at different heights in the ^3He bath, and liquid ^3He is not a good thermal conductor in this range of temperature. In our measurements, the maximum error over T due to this effect is $\sim 40\text{mK}$.¹² Drift of the electron temperature during the measurement is another cause of error. Finally, the sensitivity of the carbon glass resistor decreases at high temperature. Taking all these effects into account, we estimate that the combined error over the temperature of the electron system never exceeds $\sim 10\%$ over the whole temperature range.

¹²Note that this problem only occurred during the measurements on the first samples: corrections were made to the system to solve the problem.