Gated Ring Oscillator-Based Time-to-Digital Converter for Event-Triggered Sensing Applications

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***Abstract*—The requirements for high-performance and low-power sensing applications have recently pushed for utilizing time-based approaches. Indeed, time-based circuits, such as time-to-digital converters (TDCs), benefit from technology scaling and improved time resolution with their highly digital nature. For instance, ring-oscillator (RO) based TDCs have received significant interest in embedded sensing applications due to their simplicity of operation and low time resolution. However, current RO-based topologies are not always suited for event-triggered operations because they consume high power in free-running mode, or suffer from several implementation challenges in gated mode due to charge sharing, leakage or sampling errors. To tackle these challenges, this work proposes an event-based GRO TDC, to target low-power sensing and radar applications. The proposed GRO TDC's differential topology and gating mechanisms maintain the performance and significantly reduce power consumption, enabling efficient event-based operations with negligible charge and sampling errors. The TDC is implemented in 65-nm technology, occupying 100 µm ×147 µm. The oscillator's differential and integral non-linearity errors are kept below 0.17 LSB. An SNDR of 53.9 dB at 50 kHz is achieved with a 115 ps raw time resolution. The power dissipation is proportional to the operation frequency, with for instance 45.82 µW at 1 MHz.**

***Index Terms*—Event-Triggered Applications, Time-to-Digital Converter, gated ring oscillators, LiDAR, Time-based Sensors**

I. Introduction

With the rapid growth of embedded sensing applications, sensor interfaces are required to be highly efficient, compact, and scalable. Thus, topologies allowing ease of integration with all/mostly digital processing circuits and AI accelerators are needed [1], [2]. This is the case for time-based circuits, for which the information is encoded in the timing properties of a pulse. In contrast, analog-intensive interfaces can have performance limitations in modern technologies because of the reduced voltage headroom and intrinsic gain [3]. In that regard, time-to-digital converters TDCs are used to perform analog and mixed-signal processing functions in applications such as time-based analog-to-digital converters TB-ADC [4], [5], all-digital phase-locked loops AD-PLLs [6], time-of-flight ToF or biomedical sensors [7], [8], and jitter measurement [9].

Typically, a TDC comprises a delay generator or a time reference that determines the time resolution, and a readout circuitry that provides a digital output code D_{out} proportional to the input time ΔT_{in} as shown in Fig.1. Free-running ring oscillators (ROs) are often employed as a time reference, owing to their simple structure and ability to generate multiple phases. The RO's phases form a quantization grid with a resolution as low as the delay of a single inverting stage τ_d. The delay

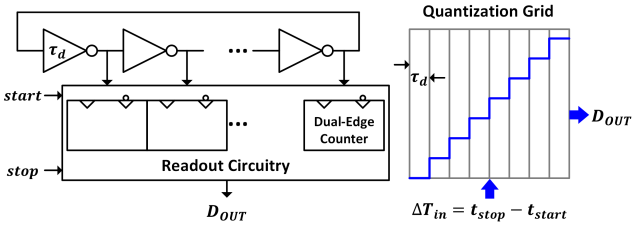

Fig. 1: Ring Oscillator-Based TDC

elements in the loop are reused to enhance the dynamic range and area efficiency. The readout circuitry accumulates phase, e.g. through dual-edge counters, while the digital code D_{out} is obtained by summing the counters' outputs.

Despite their advantages, free-running ROs are not optimal for event-based embedded applications because they dissipate high dynamic power (P_d) when high time resolution is required. To have a lower P_d, the oscillator's activity factor (ON time) can be lowered by employing a gated RO (GRO) [10]. Yet, GROs suffer from several design challenges as they are prone to errors arising from charge sharing, leakage or sampling. For example, with longer times between measurements, leakage can pull the oscillator phases into illegal states, corrupting the quantization grid and introducing errors. Finally, special care must be given to the errors introduced due to the asynchronous sampling of the counters [11], [12].

To tackle these challenges, this paper proposes a TDC architecture for low-power sensing applications, such as light detection and ranging LiDAR sensors [13], time-based temperature sensors [14], optical biosensors [15], and frequency-modulated FM inertial sensors [16]. To minimize power and allow event-based operation, the architecture uses a differential GRO topology, enabling the RO only during the measurement windows. The proposed gated topology maintains a linear operation, while the controller and readout circuits offer a scaling-friendly and easy-to-reconfigure solution with immunity against sampling errors.

With this architecture, the performance is competitive with existing implementations, achieving 0.17 LSB INL, an ENOB of 8.66 bits and an effective time resolution $t_{n,rms}$ of 15.66 ps in the signal bandwidth. In addition, the mostly-dynamic power consumption and event-based operation lead to an idle power consumption of only 1.71 µW and 374.9 nW (resp. at 1 MHz and 10 MHz sampling frequencies), scaling up to 45.82 µW

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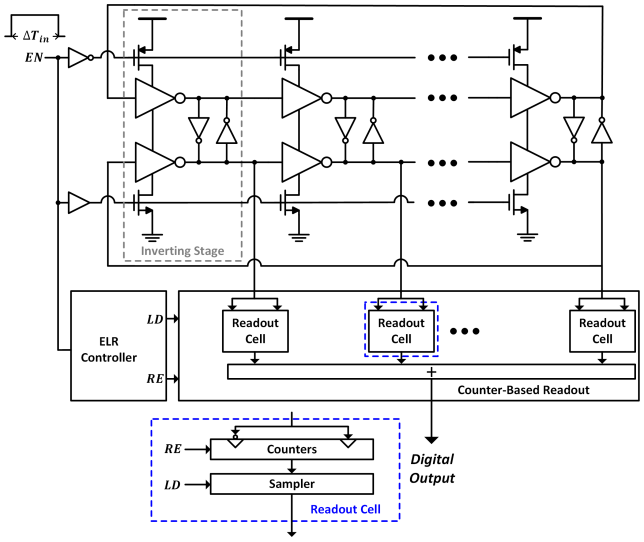
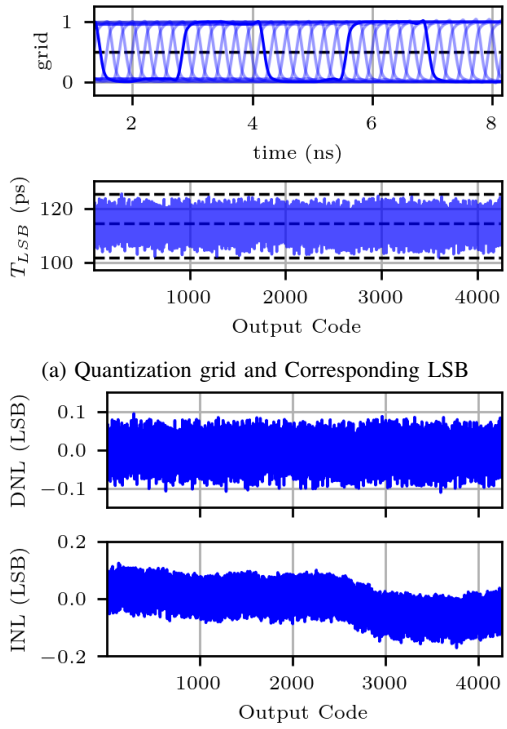


Fig. 2: Proposed TDC Architecture



(a) Quantization grid and Corresponding LSB

(b) Differential and Integral Non-linearity (DNL, INL)

Fig. 3: RO Quantization Grid

and 448 µW at half full-scale range.

The rest of this paper is organized as follows. Section II details the proposed architecture focusing on the event-based operation, linearity and minimization of various errors. The simulation results of the proposed TDC and the conclusion are given in Section III, and Section IV, respectively.

II. Proposed Gate Ring Oscillator-Based TDC

Fig. 2 shows the proposed TDC architecture, composing a 13-stage differential gated ring oscillator, a 9-bit counter-based readout, and an asynchronous controller. In this section, we detail the techniques employed to ensure the TDC robustness against non-linearity, charge leakage, and sampling errors.

A. Gated Ring Oscillator Design

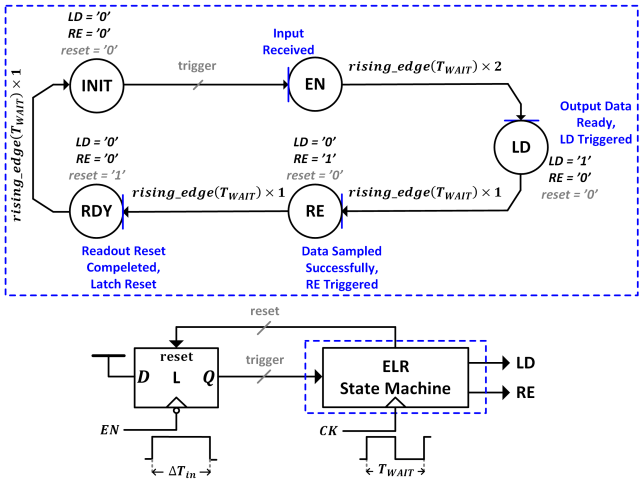
Fig. 3a shows the 115-picosecond quantization grid ($T_{LSB} = 115$ ps) generated by the proposed oscillator. Here, the grid resolution is determined by the average time difference between two consecutive edges. To limit the **static non-linearity errors when the oscillator is enabled**, the transistor sizes of the RO are chosen large enough to dismiss the differential non-linearity DNL due to local process variation (device mismatches) [17]. Additionally, in the layout, the order of the inverting stages in the RO is shuffled to equalize the horizontal wires between the stages, thereby reducing systematic DNL errors arising from the layout asymmetry.
Fig. 3b shows the DNL and the integral non-linearity INL covering 500 nanoseconds time measurement simulated with the layout systematic mismatches (post-layout simulation) and device transient noise enabled. The errors are kept below 0.17 LSB ($|DNL|_{max} = 0.11$ LSB and $|INL|_{max} = 0.17$ LSB).

To enable proper event-based operation, the RO must retain its state when paused. Yet, **leakage and charge errors** can significantly affect the TDC performance, since leakage can pull the oscillator phases to illegal states. This leads to counting errors in the following measurements when the RO is started again. To reduce this effect, we employ latch loads (see Fig. 2) to pull the oscillator phases to the nearest legal state.

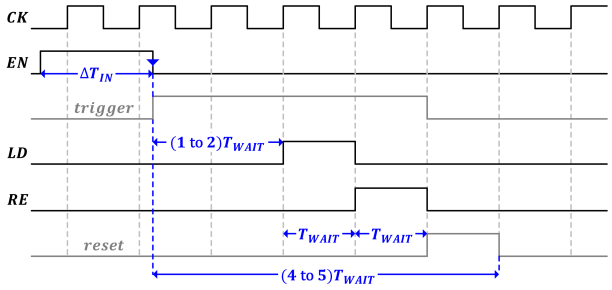
B. Counter-Based Readout and ELR Controller

The counter-based readout shown in Fig. 2 comprises 13 identical cells (1 cell for each oscillator tap) and an adder, where each cell has a dual-edge counter and output sampler. With an all-digital implementation, it is highly scalable and easy to reconfigure, e.g., for different numbers of oscillator stages and/or for different dynamic ranges (different numbers of bits). In addition, the design allows for a fully asynchronous and event-triggered operation, using the proposed Enable-Load-Reset ELR state machine shown in Fig. 4a. The ELR's timing operation is described in Fig.4b. Triggered by the EN signal representing the sensed time information ΔT_{in}, the ELR waits for a specific time defined by CK (one or more times of T_{WAIT}) to allow enough processing time for the readout e.g., until the counters output is ready. Then, the load LD signal is fired to trigger the samplers in the readout cells to capture the counter outputs (see Fig. 4a). Finally, a reset RE signal resets the counters and gets them ready for the next measurement. The rising edge of the RE signal (or the falling edge of LD) can be used to indicate that a TDC sample is ready. Here, both the pulse widths of the LD and RE are defined by T_{WAIT}.

Performing an **asynchronous sampling of the counters may result in large errors** caused by partial sampling [11],



(a) ELR State Machine and Circuit Implementation



(b) ELR Controller Timing Diagram

Fig. 4: ELR Controller Implementation and Timing Diagram

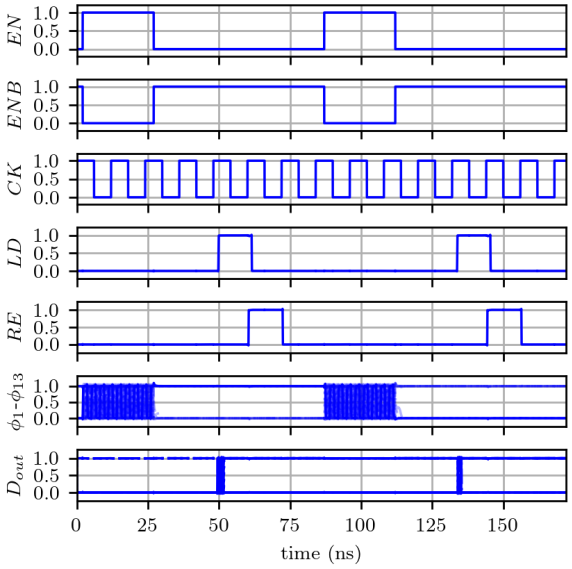


Fig. 5: TDC Transient Simulation

[12], which occurs when the counter value changes around the sampling instants. This typically requires the use of error-correction algorithms introducing additional overheads in the architecture. In contrast, the proposed architecture does not require error correction, as the RO's state is held unchanged before sampling (see Fig. 4b). This allows enough time T_{WAIT} for the counter to settle avoiding the sub-sampling errors without applying expensive correction algorithms.

III. Circuit Implementation and Simulation Results

The proposed TDC is implemented in 1V 65-nm CMOS technology. It occupies 100 µm ×147 µm, and supports 44 nanoseconds input dynamic range.

The TDC's operation and performance are verified by post-layout transient simulations with device transient noise enabled. The control signals (LD and RE), the oscillator phases (ϕ_1-ϕ_{13}), and the digital outputs (D_{out}) are monitored in consecutive measurements, as shown in Fig. 5.

The power dissipation depends on the duration of the input pulse ΔT_{in} and the sampling frequency f_{clk}. This dependency is shown in Fig. 6. An average power (at half full-scale range) of 448 µW at 10 MHz sampling frequency is dissipated (down to 51.4 µW when ΔT_{in} = 1 ns). The average dissipation is reduced to 45.82 µW at 1 MHz sampling frequency (down to 5.14 µW).

Since this work targets event-triggered applications, the power dissipation is also characterized when no input is applied (idle mode of operation). In this mode, the power dissipation is reduced to 1.17 µW and 374.9 nW at the sampling frequencies.

To examine the linearity of the TDC, a more advanced test scenario is implemented using the testbench shown in Fig. 7. The testbench is built using a voltage-to-time converter VTC which operates at 10 MHz clock/sampling frequency (f_{clk} = 10MHz), and it has 7.324 kHz sinusoidal input (f_{in} = 7.324 KHz) to generate 10 MHz pulses with sinusoidal varying pulse widths (durations) ΔT_{in}.

The VTC output is applied to an ideal TDC model and the proposed TDC. As shown in Fig. 8a, the proposed TDC output $\Delta T_{out}[n]$ successfully tracks the 7.324 kHz sinusoidal input ΔT_{in} ($\simeq$ 10 ns peak-to-peak) following the ideal model.

The frequency-domain (FFT) output in Fig. 8b shows that the TDC achieves a signal-to-noise and distortion ratio SNDR of 53.91 dB at 50 kHz bandwidth, and an effective number of bits ENOB of 8.66 bits. This is equivalent to an effective time resolution $t_{n,rms}$ of 15.66 ps in the signal bandwidth. The effective resolution is calculated from the total integrated noise in the bandwidth = $\sqrt{0.5\Delta T_{in,pp}^2/\text{SNDR}}$.

In this test, the signal frequency and bandwidth are inspired by the speciations of FM gyroscopes but scaled up to shorten the simulation time. Increasing the over-sampling ratio OSR can further shorten $t_{n,rms}$ (increase the effective resolution). At 25 kHz bandwidth (2× OSR), 10.22 ps $t_{n,rms}$ is achieved.

A comparison with the state-of-the-art relevant TDCs that target sensing applications is conducted in Table I. As shown, the proposed TDC achieves competitive metrics with a scaling-friendly and reconfigurable architecture that suits low-power and event-triggered sensing applications.

TABLE I: Comparison of State-of-the-Art Time-to-Digital Converters

	TCASII'16 [18]	TVLSI'20 [14]	TCASII'22 [19]	TCASII'23 [13]	This work
Technology (nm)	65	180	65	350	65
TDC Architecture	Successive Approximation	Pulse-Shrinking	Oscillator-Based	Oscillator-Based	Oscillator-Based
Applications	Generic	Temperature Sensing	ToF 3D Imaging	LiDAR	Event-Triggered Sensing
Number of Bits	10	10	12	11	9
Resolution (ps)	61	45	24.5	40	115 (**15.66** [a])
Range (ns)	31.5	40	100	82 [b]	44
INL_{max} (LSB)	2.38	0.85	6.12	1 [b]	0.17
Rate (Hz)	29.4M	10k	125M [c]	100M	10M
Area (μm^2)	Not Reported	$19x10^3$	1920	1350	14700
Power Dissipation (µW)	2769	550	1030	2190	448 [d], (**1.17 in Idle Mode**)
FoM [e] (pJ/conv)	0.311	99.37	0.014	0.021	0.102 [f]

[a] Effective Resolution considering oversampling, calculated from the total integrated noise in the signal bandwidth: $t_{n,rms} = \sqrt{\frac{0.5\Delta T_{in,pp}^2}{\text{SNDR(OSR)}}}$

[b] Estimated

[c] Limited by the serializer

[d] Input Dependent down to 51.4 µW

[e] FoM = Power Diss./(Rate$\times 2^{\text{Linear Bits}}$), Linear Bits = Number of Bits - $\log_2$(INL + 1)

[f] Input Dependent down to 0.012 pj/conv

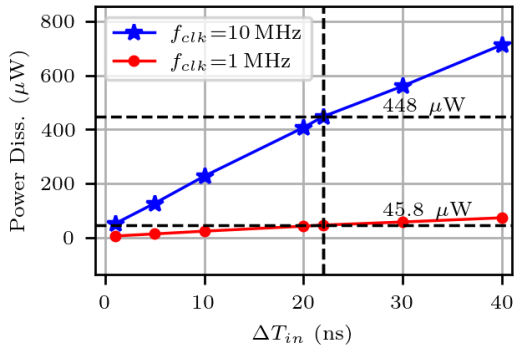


Fig. 6: Power Dissipation Versus ΔT_{in}

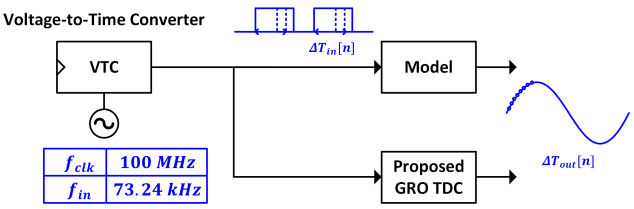
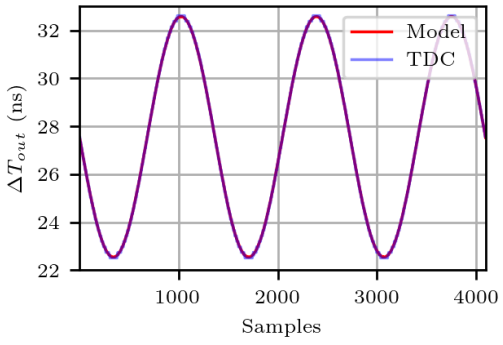
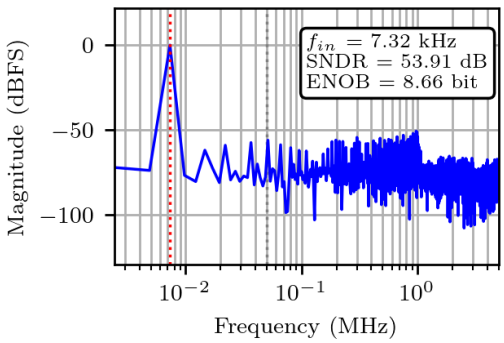


Fig. 7: VTC-Based Testbench



(a) Time-Domain Outputs



(b) Frequency-Domain (FFT) Outputs

Fig. 8: Post-Layout Simulation Results

IV. Conclusion

This paper presents a low-power GRO TDC to target event-triggered applications. The proposed TDC is implemented in 1V 65-nm CMOS technology, occupying 100 µm ×147 µm. The RO's static non-linearity errors are kept below 0.17 LSB, and the charge and leakage errors are minimized.

The proposed ELR controller and readout offer a scaling-friendly and easy-to-reconfigure solution with immunity against sampling errors.

The TDC dissipates 448 µW at 10 MHz sampling frequency. The power dissipation is reduced to 45.82 µW at 1 MHz. The idle power dissipation is as low as a few hundred nanowatts. An SNDR of 53.91 dB is achieved at 50 kHz bandwidth and 10 MHz sampling (ENOB of 8.66 bits, and effective time resolution of 15.66 ps) verifying the TDC linearity. Higher effective resolution can be achieved by increasing the OSR. With these metrics, the proposed TDC suits low-power and event-triggered sensing applications.

REFERENCES

[1] A. Amaravati, S. B. Nasir, J. Ting, I. Yoon, and A. Raychowdhury, "A 55-nm, 1.0-0.4v, 1.25-pj/mac time-domain mixed-signal neuromorphic accelerator with stochastic synapses for reinforcement learning in autonomous mobile robots," *IEEE Journal of Solid-State Circuits*, vol. 54, no. 1, pp. 75–87, 2019.

[2] A. M. Mohey, J. Leslin, G. Singh, M. Kosunen, J. Ryynänen, and M. Andraud, "A. m. mohey, j. leslin, g. singh, m. kosunen, j. ryynänen, m. andraud," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 32, no. 12, pp. 2220–2231, 2024.

[3] A.-J. Annema, B. Nauta, R. V. Langevelde, and H. Tuinhout, "Analog circuits in ultra-deep-submicron cmos," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, p. 10.1109/jssc.2004.837247, 2005.

[4] V. Unnikrishnan and M. Vesterbacka, "Time-mode analog-to-digital conversion using standard cells," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 12, pp. 3348–3357, 2014.

[5] V. Unnikrishnan, O. Jarvinen, W. Siddiqui, K. Stadius, M. Kosunen, and J. Ryynänen, "Data conversion with subgate-delay time resolution using cyclic-coupled ring oscillators," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 29, no. 1, pp. 203–214, 2021.

[6] L. Xu, S. Lindfors, K. Stadius, and J. Ryynänen, "A 2.4-ghz low-power all-digital phase-locked loop," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 8, pp. 1513–1521, 2010.

[7] S. Kurtti, J.-P. Jansson, and J. Kostamovaara, "A cmos receiver-tdc chip set for accurate pulsed tof laser ranging," *IEEE Transactions on Instrumentation and Measurement*, vol. 69, no. 5, pp. 2208–2217, 2020.

[8] O. Olabode, M. Kosunen, V. Unnikrishnan, T. Palomäki, T. Laurila, K. Halonen, and J. Ryynäsnen, "Time-based sensor interface for dopamine detection," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 10, pp. 3284–3296, 2020.

[9] J. Yu and F. F. Dai, "On-chip jitter measurement using vernier ring time-to-digital converter," in *19th IEEE Asian Test Symposium*, 2010, pp. 167–170.

[10] M. Z. Straayer and M. H. Perrott, "A multi-path gated ring oscillator tdc with first-order noise shaping," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, 2009.

[11] V. Unnikrishnan and M. Vesterbacka, "Mitigation of sampling errors in vco-based adcs," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 7, pp. 1730–1739, 2017.

[12] K.-C. Choi, S.-W. Lee, B.-C. Lee, and W.-Y. Choi, "A time-to-digital converter based on a multiphase reference clock and a binary counter with a novel sampling error corrector," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, no. 3, pp. 143–147, 2012.

[13] J. Hu, D. Li, X. Wang, R. Ma, Y. Liu, and Z. Zhu, "A 40-ps resolution robust continuous running vcro-based tdc for lidar applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 2, pp. 426–430, 2023.

[14] C.-C. Chen, C.-L. Chen, W. Fang, and Y.-C. Chu, "All-digital cmos time-to-digital converter with temperature-measuring capability," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 9, pp. 2079–2083, 2020.

[15] Z. Ebrahimi and B. Gosselin, "Photodetector innovations for advancing wearable optical biosensors: A review," *IEEE Sensors Journal*, vol. 25, no. 3, pp. 4070–4095, 2025.

[16] M. Leoncini, M. Bestetti, A. Bonfanti, S. Facchinetti, P. Minotti, and G. Langfelder, "Fully integrated, 406 μa, 5 °/hr, full digital output lissajous frequency-modulated gyroscope," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 9, pp. 7386–7396, 2019.

[17] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of mos transistors," *IEEE Journal of Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, 1989.

[18] K. O. Ragab, H. Mostafa, and A. Eladawy, "A novel 10-bit 2.8-mw tdc design using sar with continuous disassembly algorithm," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 10, pp. 909–913, 2016.

[19] F. Arvani and T. C. Carusone, "A reconfigurable 5-channel ring-oscillator-based tdc for direct time-of-flight 3d imaging," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 69, no. 5, pp. 2408–2412, 2022.