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Traps characterization in RF SOI substrates including a buried SiGe layer☆

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ABSTRACT

This work analyzes the interface traps density (D_{it}) at the SiO_2/SiGe interface of a buried SiGe stressor SOI substrate, and demonstrates the impact of those traps on the effective resistivity (ρ_{eff}) of the substrate. The *C-V* behavior of MOS capacitors and the RF insertion loss along coplanar waveguide transmission lines on various substrates are measured. TCAD simulations are employed to interpret the traps characteristics and to forecast the RF performance of a buried SiGe stressor SOI wafer having a high resistivity handle Si substrate. The results demonstrate that thanks to the interface traps introduced by the SiGe layer the substrate effective resistivity (ρ_{eff}) is enhanced.

1. Introduction

When it comes to radio-frequency (RF) applications, an Silicon-on-Insulator (SOI) substrate requires low propagation losses and harmonic distortion at microwave frequencies, and this necessitates a high effective resistivity. However, fixed charges present at the BOX/semiconductor bottom interface attract free carriers toward the interface, lowering the effective resistivity of the substrate. This is referred to as the parasitic surface conduction (PSC) that undermines the efficiency of employing a High-Resistivity (HR) substrate. One efficient way to reduce free carriers near the Si surface and conserve the high resistivity property of the substrate is to take advantage of a large density of interface traps (D_{it}) at the SiO_2/Si interface. High interface trapping states lead to deep Fermi level pinning in the band gap, so that the concentration of free carriers remains low, ensuring a state of high resistivity. This translates into lower losses and higher linearity of the substrate[1,2]. In our work, an epitaxial SiGe layer is inserted between the buried oxide (BOX) and the handle Si substrate. A SiO_2/SiGe interface tends to have higher D_{it} values than SiO_2/Si, attributed to the formation of Ge-O bonds at the interfacial layer [3]. Consequently, it would be valuable to investigate D_{it} and the effective resistivity (ρ_{eff}) in different buried SiGe stressor substrates.

2. Experimental Details

Fig. 1 shows a SiGe MOS capacitor (a) and a coplanar waveguide (CPW) transmission line structure schematic cross-section (b). Here, R_s is the series resistance of the Si substrate. C_{ox} is the capacitance of the dielectric stack. G_p and C_p are the parallel equivalent conductance and capacitance, respectively, corresponding to the SiO_2/SiGe interface. SiGe/Si is assumed to be a trap-free interface. Table 1 lists the composition of five buried SiGe stressor fully-depleted (FD) SOI substrates and the related thickness of the SiGe layer. The preparation of MOS capacitor and CPW lines on buried SiGe stressor FD SOI substrate is described hereafter. 300 nm SOI wafers (<100>, *p*-type, standard resistivity) with buried SiGe under the BOX (20 nm) were fabricated by Acorn Technologies.

The *C-V* measurements were conducted under dark conditions using a PM8PS prober and B1500 semiconductor analyzer. The frequency ranges from 1 kHz to 400 kHz at room temperature. The small-signal measurements of the CPW lines have been performed using an Agilent 2-port performance network analyzer (PNA) and a pair of 100-μm pitch ground signal ground (GSG) |Z| probes. The S-parameters have been measured to extract the effective resistivity. Short-open-thru-load (SOTL) method was used to calibrate the system at the probe tips. After measuring the open, thru, and line, the de-embedding method proposed by Gillon [4] was used to remove the pad parasitics.

With reference to Fig. 1 (b), the physical parameters of the structure are: the metal thickness of CPW line $t_{metal} = 1$ um, the oxide thickness $t_{ox} = 200$ nm, the signal line width $W_c = 26$ μm, the ground line width $W_G = 208$ μm, and gap spacing to ground lines of $S = 12$ μm.

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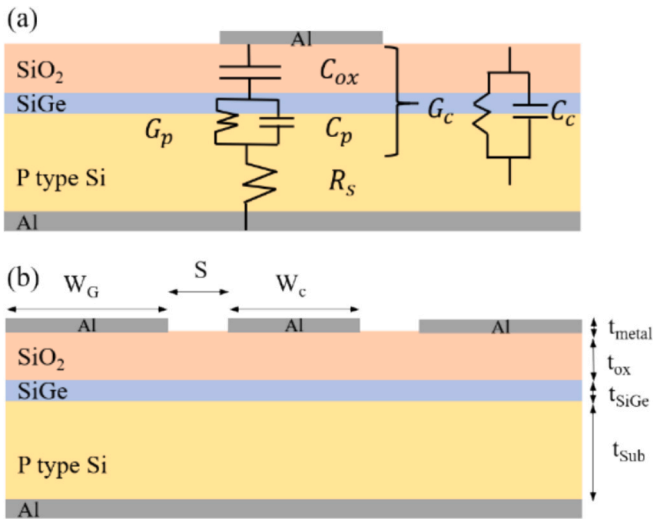

Fig. 1. (a) The cross-section of SiGe buried stressor FD SOI capacitor. (b) The cross-section of a CPW line on top of SiGe buried stressor FD SOI substrate.

Table 1
Summary of Substrate Parameters.

Sample number	SiGe thickness (Å)	% Ge	D_{it} ($eV^{-1}cm^{-2}$)	ρ_{eff} (Ω•cm) @ 2 GHz @ 0 V
1	90	20	1.6×10^{12}	45.7
2	130	20	2.2×10^{12}	46.0
3	700	20	2.5×10^{12}	46.1
4	60	40	4.0×10^{11}	39.3
5	110	30	8.0×10^{11}	43.6
Standard Si	–	–	2.5×10^{11}	21.5
SiGe/HR Si (TCAD)	1100	20	2.2×10^{12}	5213

3. Results and Discussion

3.1. A. Interface trap Behaviour

Fig. 2 shows the traps occupancy and free carrier variation in response to a shift of Fermi level (E_f) at 0 V applied bias, where Q_{ox} is fixed to 1×10^{11} cm^{-2}, D_{it_don} and D_{it_acc} are the acceptor and donor interface traps density, respectively, N_{tD}^{+} and N_{tA}^{-} are the densities of ionized donor and acceptor traps, respectively, and p and n are the free carrier densities for holes and electrons, respectively. The PSC effect arises from the presence of the fixed charge, Q_{ox} (typically positive at the SiO_2/SiGe interface), which triggers significant band bending of the Fermi level towards the conduction band edge.

Consequently, this phenomenon results in an increased population of free electrons that counterbalance the positive fixed charges found at the interface and form a conductive PSC sheet layer. To maintain the high resistivity of the substrate (high ρ_{eff}), the compensating charges at the interface must be ionized interface traps instead of free carriers that contribute to the PSC. The ionized interface traps N_{tD}^{+} and N_{tA}^{-} at the interface SiO_2/SiGe distributed in the band gap will mainly compensate for the applied charge ($Q_{applied} = Q_{ionized} + Q_{free}$) [5]. In Fig. 2 (a), when the density of ionized interface traps exceeds 1×10^{12} $eV^{-1}cm^{-2}$, it primarily contributes to compensation instead of free carriers (at least for usual values of Q_{ox} (i.e. in the range of 10^{11}) and/or of usual applied bias voltages (i.e. in the range of a few Volts). This leads to the Fermi level being strongly pinned within the band gap. Conversely, in Fig. 2 (b), when the density of ionized interface traps is lower than 1×10^{12} $eV^{-1}cm^{-2}$, the free carriers n and p dominate the compensation, causing the Fermi level to shift closer to the conduction band, and a to the formation of a PSC layer to compensate for the Q_{ox}.

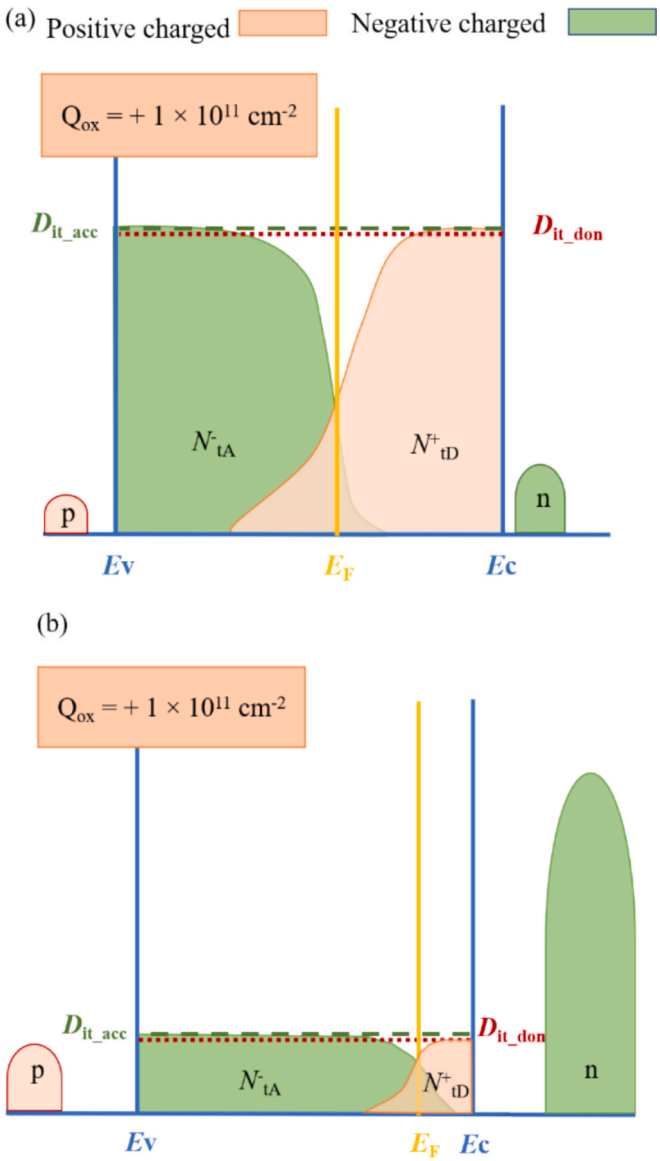

Fig. 2. Graphic representations of traps occupancy and free carrier density variation in response to a shift of Fermi level E_F at 0 V applied bias: (a) PSC induced by Q_{ox} is compensated mainly by ionized acceptor and donor interface traps (D_{it_acc} & $D_{it\_don} > 1 \times 10^{12}$ $eV^{-1}cm^{-2}$) at SiO_2/SiGe interface. (b) PSC induced by Q_{ox} is compensated mainly by free carriers p and n (D_{it_acc} & $D_{it\_don} < 1 \times 10^{12}$ $eV^{-1}cm^{-2}$).

3.2. B. C-V Characterizations and trap Parameter Extractions

Fig. 3 (a) and 3 (b) shows the measured and simulated (with TCAD Silvaco Atlas) corrected C_c-V curves for frequencies ranging from 1 kHz to 400 kHz. The measured and simulated (d) parallel equivalent conductance (G_p/ω) as a function of angular frequency (ω) at different gate voltages in the depletion regime for sample 2 are shown in Fig. 3 (c) and 3 (d), respectively. The simulated C_c-V and $G_p/\omega - f$ curves, along with the extracted D_{it} from the C-V measurements, exhibit similar trends. Using the series resistance correction model (SRC) proposed by Nicollian [6] presented in Fig. 1 (a), C_c and G_c, can be calculated to withdraw the effect of the series resistance in Fig. 3 (a) and (b). One can see the flatband voltages shift towards negative values with increased frequencies, preventing a conventional flatband extraction. This horizontal frequency-dependent shift can be explained with the effective

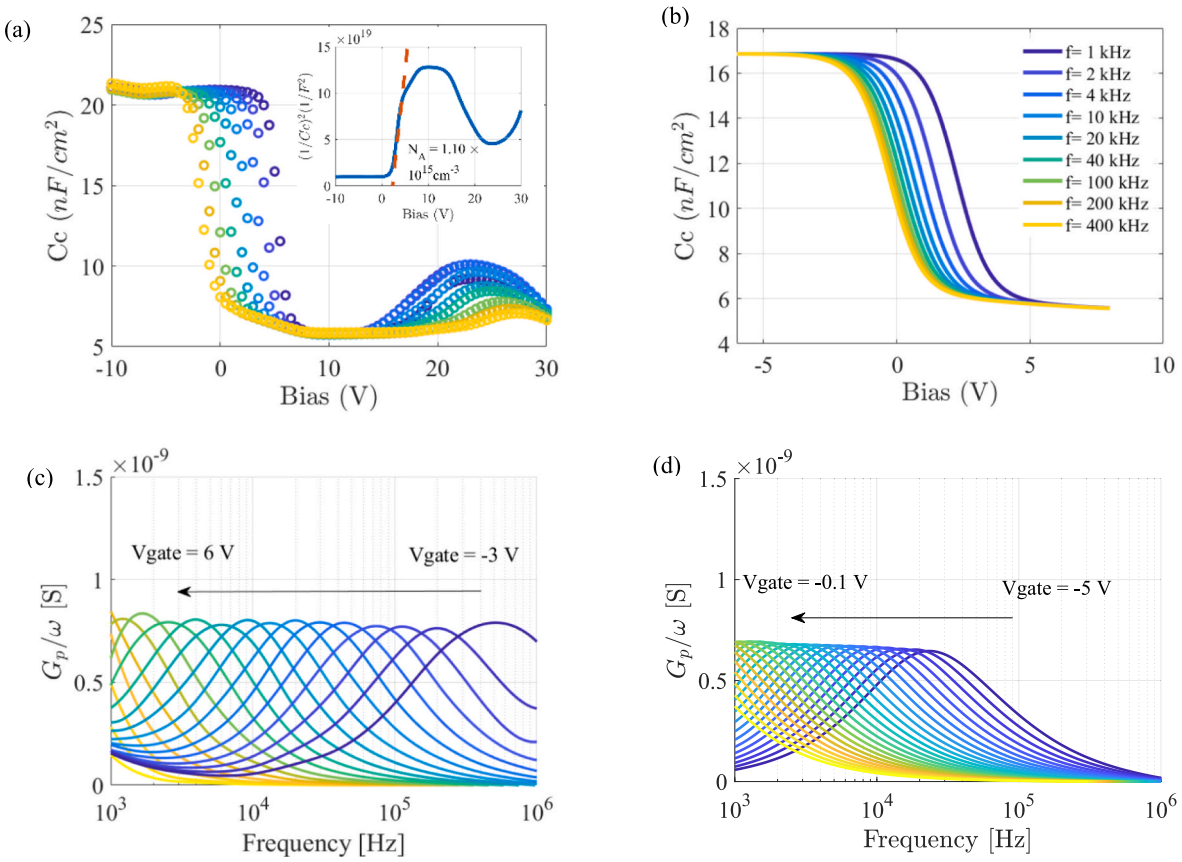

Fig. 3. (a) Measured and (b) simulated corrected capacitance versus applied bias ($C_c - V$) from 1 kHz to 400 kHz for sample 2. (c) Measured and (d) simulated parallel equivalent conductance (G_p/ω) as a function of angular frequency (ω) at different gate voltages in depletion regime. In simulations, $Q_{ox} = 1 \times 10^{11}$ cm^{-2} and $D_{it} = 2.2 \times 10^{12}$ eV^{-1}cm^{-2} are used. The inset shown in (a) corresponds to N_A doping extraction. The curve $C_c - V$ at 10 kHz is taken for calculating the slope of the linear part of the $(1/C_c)^2$ curve with respect to applied bias.

pinned Fermi level by high D_{it} at the interface SiO_2/SiGe [7]. The "bump" arises within the inversion region, where the increase in capacitance under positive bias with decreasing frequency is largely mitigated. This could also be attributed to a high interface traps density effectively stabilizing the Fermi level [8]. The extraction of average substrate p-type doping concentration, N_A (= 1.10×10^{15} cm^{-3}) is here based on the slope of the linear part of the $(1/C_c)^2$ curve versus the applied voltage in the inset [9], corresponding to 14 Ω•cm for all SiGe samples. Fig. 3 (c) and (d) show $G_p/\omega - f$ curves for both measurements and simulations. The peak positions of the G_p/ω (f) curves shift to high voltage values with decreased frequency due to the presence of interface traps states. Therefore, we obtain the interface traps response for a gate voltage range from −3 to 6 V.

3.3. C. RF Characterizations of CPW lines and Extrapolation of Burried SiGe in a HR SOI substrate

Fig. 4 (a) shows the D_{it} ($\Delta E = E_T - E_v$) profiles of samples 3, 4, standard Si, and TCAD SiGe/HR Si at room temperature, the trap energy states distributed in the band from 0.3 to 0.5 eV above the valence band. For comparison, samples 3, and 4 with the highest and lowest D_{it}, respectively, are selected among all buried SiGe substrates. The D_{it} of TCAD SiGe/HR Si is based on the extracted value from sample 2. Standard Si with a SiO_2/Si interface typically exhibits the normal D_{it} around $\sim 10^{10}$ eV^{-1}cm^{-2}. In Fig. 4 (b), sample 3, which has the highest D_{it} (2.5×10^{12} eV^{-1}cm^{-2}) among five SiGe samples, shows a relatively flat and elevated ρ_{eff} compared to sample 4 over the range of −15 to 15 V at 2 GHz. In contrast, sample 4, with the lowest D_{it} (4.0×10^{11} eV^{-1}cm^{-2}), exhibits a more bias-dependent ρ_{eff} due to reduced interface trap compensation. Unlike samples 3 and 4, standard Si (15–20 Ω·cm) demonstrates an even lower ρ_{eff}, which also varies with gate bias, corresponding to a D_{it} an order of magnitude lower than that of sample 4. The boost of ρ_{eff} is attributed to the larger D_{it} at SiO_2/SiGe compared with SiO_2/Si. The simulations for samples 3 and 4 align with its experimental characterization, which can then be used to model high resistivity buried SiGe stressor FD-SOI substrate. To give insight into the potential of SiGe solution in enabling high-quality RF performance, buried SiGe high resistivity Si substrate (2 kΩ•cm) is employed in the TCAD simulation, as seen in Table 1. It presents a high ρ_{eff} above 2 kΩ•cm being bias independent due to the sufficient compensation provided by the interface traps.

4. Conclusion

Summarizing, the efficiency of the buried SiGe stressor substrate has been characterized. Both small signal measurements and simulations demonstrate that high D_{it} extracted from the conductance method at an SiO_2/SiGe interface can neutralize the free carriers coming from bulk, thus overcoming the PSC effect and ensuring a state of high resistivity. High resistivity buried SiGe stressor substrate emerges as a promising candidate for RF SOI integration. At the same time, a buried SiGe layer can be a useful layer being able to induce tensile strain in the channel of an SOI MOSFET if both the SOI and BOX layers are extremely thin (FD-SOI), thereby boosting transistor mobility [10].

CRediT authorship contribution statement

Y. Yan: Writing – original draft, Investigation, Formal analysis. **M.**

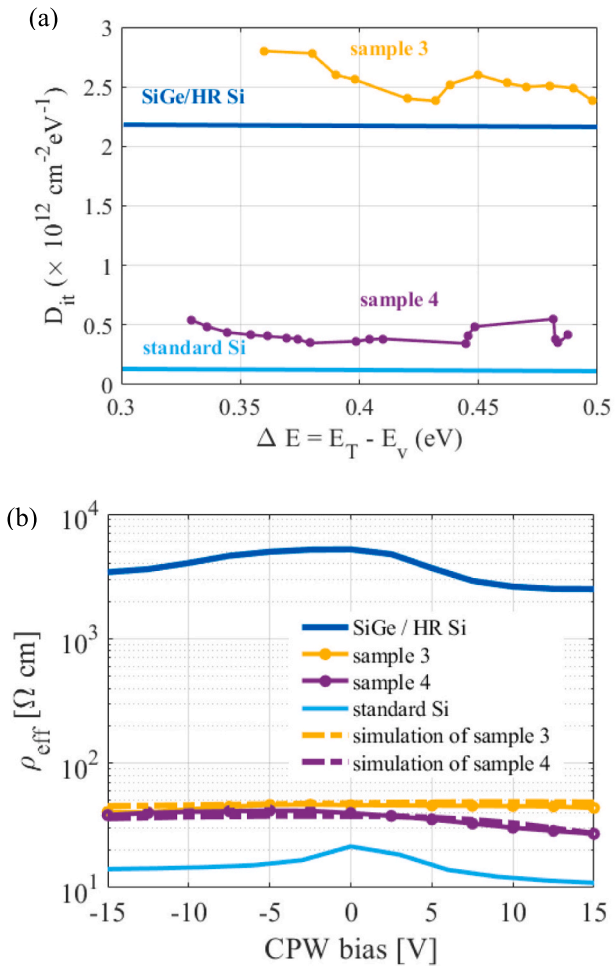

Fig. 4. (a) D_{it} ($\Delta E = E_T - E_v$) profile showing D_{it} of samples 3, 4, standard Si, and SiGe/HR Si energy distribution in the band gap respectively. (b) CPW line effective resistivity of samples 3 (includes the simulation), 4 (with the simulation), standard Si, and simulated SiGe/HR Si extracted at 2 GHz as a function of applied bias from −15 to 15 V.

Rack: Writing – review & editing, Validation, Methodology. **M. Vanbrabant:** Writing – review & editing, Investigation, Formal analysis. **M. Nabet:** Writing – review & editing, Validation. **A. Goebel:** Writing – review & editing, Supervision, Resources, Project administration. **P. Clifton:** Writing – review & editing, Supervision, Resources, Project administration. **J.-P. Raskin:** Writing – review & editing, Supervision, Resources, Project administration, Funding acquisition.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

The authors do not have permission to share data.

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