Solid-State Electronics 229 (2025) 109174

Contents lists available at ScienceDirect

Solid State Electronics

journal homepage: www.elsevier.com/locate/sse

Low-loss silicon substrates with PN passivation in 28 nm FD-SOI☆

M. Rack [a,*], M. Nabet [a], Y. Bendou [a], M. Vanbrabant [a], M. Moulin [a], Q. Courte [a], S. Cremer [b], A. Cathelin [b], D. Lederer [a], J.-P. Raskin [a]

[a] Université catholique de Louvain, Louvain-la-Neuve, Belgium
[b] STMicroelectronics, Crolles, France

ARTICLE INFO

The review of this paper was arranged by Francisco F. Gamiz

Keywords:
Substrate losses
Substrate linearity
Effective resistivity
Parasitic surface conduction
Interface passivation

ABSTRACT

In this work, the 28 nm FD-SOI technology from ST Microelectronics was run for the first time on high-resistivity wafer samples. The gain in RF performance through the use of high-resistivity bulk is characterized in terms of losses, effective resistivity (ρ_{eff}) and generated harmonics through on-wafer measurements of coplanar waveguides (CPW). Beyond the use of a high-resistivity bulk, special care was taken to ensure a state of high-resistivity at the silicon/oxide interface. This was achieved through the PN junction interface passivation solution, implemented locally on the wafer at the foundry level, below passive RF devices. A study was performed on the dose and energy parameters of these implants to achieve optimal RF performance and giving insight into the PN design.

1. Introduction

Nowadays, advanced CMOS nodes offer competitive figures of merit for radio-frequency (RF) and mm-wave applications. In particular, FD-SOI devices boast f_t and f_{max} metrics in the range of 300 to 400 GHz [1,2], and support rich back-end-of-line options with 8 to 10 metal layers, including several thick layers supporting high-Q RF/mm-wave passives and interconnects.

In RFICs, signals propagate in metals atop insulator-semiconductor stacks, such as in a coplanar waveguide (CPW), the cross-section of which is depicted in Fig. 1a. The silicon substrate is part of the electromagnetic environment of such devices, and can be responsible for significant amounts of losses, coupling and non-linear signal distortion if the silicon resistivity is low [3].

Using high-resistivity (HR) silicon substrates (with nominal resistivity $\rho_{nom} > 1$ kΩcm) rather than standard doped silicon ($\rho_{nom} = 10$ to 20 Ωcm) brings an improvement to these effects, though the benefits are hindered by the *parasitic surface conduction* (PSC) effect [4]. A PSC layer is induced by fixed positive charges at the Si/SiO_2 interface that attract significant amounts of free electrons, forming a thin channel-like layer that is highly conductive [3,4], (oftentimes down to a few mΩcm). PSC then degrades (lowers) the *effective resistivity* (ρ_{eff}) sensed by coplanar circuitry overlying the Si-substrate stack. For these reasons the ρ_{eff} of HR substrates is typically in the range of 30 to 150 Ωcm.

Interface passivation solutions have then been developed to counter the PSC layer, the most widespread of which is the *trap-rich* solution, that introduces a thin layer of polysilicon in between the SiO_2 and Si, that is rich in defects that trap free carriers and render the interface resistive [5,6]. Trap-rich SOI has seen strong industrial success in PD-SOI nodes. However, FD-SOI support below-BOX features (back-gate contacts, isolations wells, diodes, etc.) that are difficult to integrate within defect-rich poly-Si. Such compatibility issues motivate the development of alternative interface passivation schemes.

The *PN interface passivation* technique is then particularly of interest for FD-SOI. By utilizing alternating regions of P- and N-type doping, the conductive interface is interrupted locally by induced depletion junctions, whose chain-series combination results in a strong increase in overall substrate impedance (ρ_{eff}) [7].

This passivation scheme was first described in [7], and in this work is applied to an industrial FD-SOI process.

The implementation of this passivation technique is depicted in Fig. 1b, where PN junction are placed *parallel* to the line, such that the induced PN junctions are defined *perpendicular* the E-field in the CPW line (E-field between the signal and ground lines of the CPW), increasing the substrate impedance, reducing the lineic conductance "G" of the line, and hence the RF losses.

☆ This article is part of a special issue entitled: 'EuroSOI-ULIS 2024' published in Solid State Electronics.

* Corresponding author.
E-mail address: martin.rack@uclouvain.be (M. Rack).

https://doi.org/10.1016/j.sse.2025.109174

Available online 8 June 2025

In this paper, the PN interface passivation solution is applied to STMicroelecronics' 28 nm FD-SOI line run on both the standard 10 Ωcm Si as well as on split runs using HR wafers. Several splits were considered pertaining to the PN implant energies and doses targeting the optimal interface passivation process, giving strong insight into the critical parameters involved in this solution.

Overall, the on-wafer RF measurements of CPW test structures demonstrate strong increase in substrate ρ_{eff}, lower substrate loss and reduced non-linearities.

2. Test structures and process splits

The principle behind the PN passivation is to interrupt the interface conduction layer with highly resistive depletion regions that are induced at alternating PN boundaries [7]. To illustrate the principle of increased in interface sheet resistivity, TCAD simulations were run using the Athena and Altas softwares from Silvaco to emulate the PN-implant process and extract the electrical properties of the substrates considered. Fig. 2 plots the resistivity profile along the Si interface, highlighting the high-resistivity peaks at the PN junctions that dominate the value of the effective interface sheet resistivity. That sheet resistivity is higher-valued the larger the PN junction density per unit of distance along the interface. A depletion density can be defined as the ratio of W_{dep} over the pitch P (see Fig. 2). To maximize the depletion density, large values of W_{dep} and low values of P are sought [7,8]. W_{dep} is set by implant conditions, and lower-ranged doses are then preferred to maximize it [7]. Low values of P are achieved using the tightest lithography available in the process for substrate implants. However, using the most aggressive pitch can lead to undesired electrical coupling and connections between different wells. This problem is highlighted in Fig. 1c: if the depths of the N and P implants are not well balanced, using a tight-pitch results in connection between the deeper polarity wells via the region below the shallower wells. Fig. 1d shows that even if that same depth-imbalance exists while using larger pitch values, the problem is avoided.

Aiming for the best possible results using the tightest pitch values, 10 different wafers were processed with variations in the implant conditions attempting to achieve an optimal depth-implant balance suitable for the most aggressive pitch parameter. The implants are performed as an additional step in the foundry's FEOL process. Those 10 conditions were determined based on predictive TCAD simulations prior to the wafer processing.

3. Substrate performance – CPW data

3.1. Small-signal results

Fig. 3 plots the effective resistivity and line losses extracted [9] from the measured CPW lines.

Two types of CPWs were fabricated and measured, with the dimensions given in Fig. 3b. The first set of CPWs was fabricated by stacking the thick high-level metals IB and LB, leading to CPW that is around 3.5 μm from the Si interface. A second set of CPW lines was designed in a stacked combination of M1 to LB. These lines are much closer to the Si material (around 0.4 μm) and therefore have inherently higher sensitivity to the various substrate options considered, and will serve to extract accurate effective substrate properties close to the Si/SiO_2 interface. The dimensions for both sets of lines were chosen to achieve 50 Ω of characteristic impedance.

The results demonstrate for the M1LB lines that the 30 GHz losses can be reduced from 2.75 to 1.06 dB/mm using a high resistivity (around 1 kΩcm) substrate over the standard 10 Ωcm one, and that the loss can be further reduced down to 0.36 dB/mm when using the PN passivation (W09). Overall, by including both a highly resistive bulk along with a highly resistive interface, the effective resistivity sensed by the M1LB CPWs can be improved from 10 Ωcm to over 500 Ωcm.

Similar observations can be made for the IBLB lines in Fig. 3c, that demonstrates that the 30 GHz losses can be reduced from 1.18 to 0.60 dB/mm using the HR substrate over the standard one, reducing further down to 0.34 dB/mm when adding the PN passivation (W09). By including both a highly resistive bulk along with a highly resistive interface, the effective resistivity sensed by the IBLB coplanar lines can be improved from around 30 Ωcm to around 1000 Ωcm.

3.2. Impact of PN implant parameters

Tables 1 and 2 recap the extracted effective resistivity and line loss values on all 10 wafer splits for the M1LB lines. Samples from Table 1 employ normalized P and N implant doses of 100 %, while samples in Table 2 employ halved doses. The splits are made in N and P implant energies, to try and achieve ideal depth balance between neighbouring wells. The implant parameters pertaining to wafers W01, W02, W08, W04, W05 and W10 are imbalanced, with the N wells being deeper than the P wells, and parasitic N-well to N-well coupling happening in those wafers, bypassing the resistive depletion region at the interface, as depicted in Fig. 1c. Thanks to the split wafer processes, wafers W03, W07, W06 and W09 achieve good balance and high performance RF results by implanting the N wells shallower with reduced energy or by implanting the P wells deeper with higher energy. In those cases, effective resistivities up to 540 Ωcm can be achieved, with losses reduced to 0.36 dB/mm at 30 GHz.

Experiments on the same 10 wafers utilising relaxed-pitch PN implant patterns below the same lines were run. When the PN pitch is relaxed to 2x the minimum value, all wafers achieve ρ_{eff} values in the range of 250 to 350 Ωcm. Since the depletion density is reduced (see Fig. 2), values of 400 to 540 Ωcm are no longer attainable. However, the passivation becomes more robust to the implant conditions, since with that relaxed pitch, all 10 different implant parameters yield decent (~300 Ωcm) results (whereas for the fine-pitch only 4 of the 10 wafers exhibited a ρ_{eff} value above 300 Ωcm), and no wafers suffer from

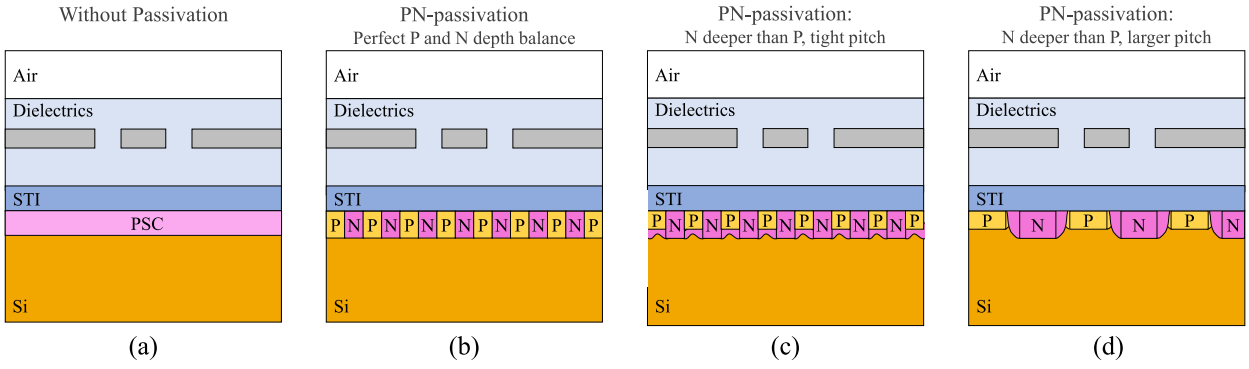

Fig. 1. CPW above (a) an unpassivated substrate with PSC (a), and above three types of PN-passivated substrates (b), (c) and (d).

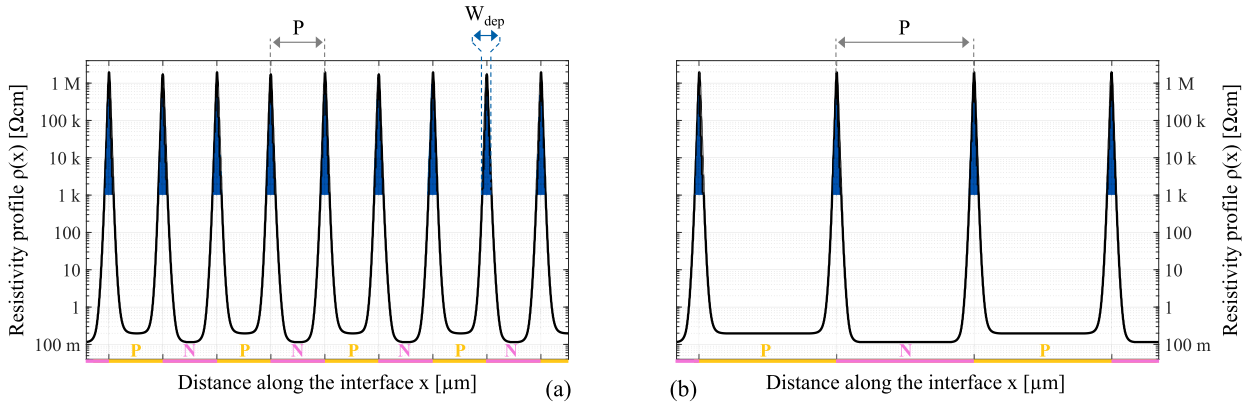

Fig. 2. Local resistivity profile ρ(x) along the Si/STI interface passivated with alternating PN junctions (obtained from TCAD). (a) using a tight pitch achieving a depletion ratio of $W_{dep}/P = 20$ %, and (b) using a relaxed pitch achieving 7 %.

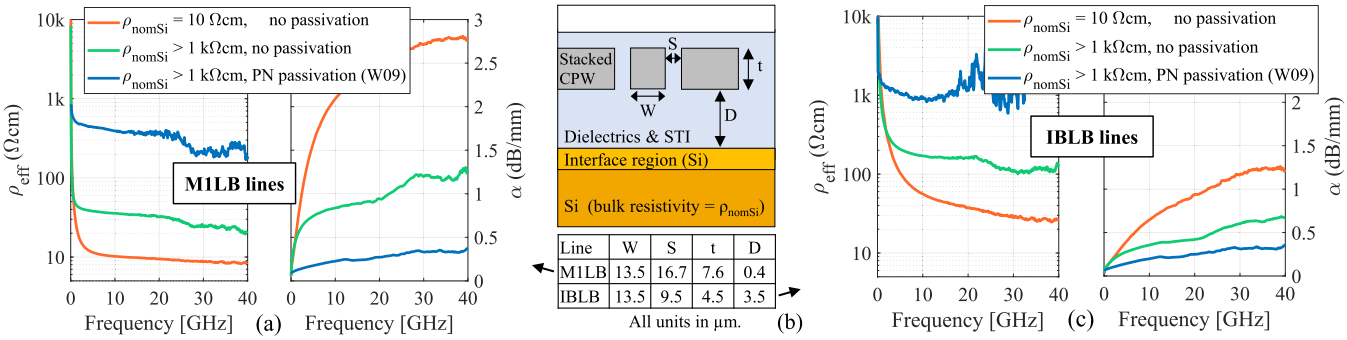

Fig. 3. Effective resistivity and line loss extracted from M1LB lines: (a), and from IBLB lines: (c), for selected wafers. Geometry of the CPWs: (b).

Table 1
RF Performance from M1LB CPW Lines of Wafer Splits in PN Implant Energy for Doses of 100 % (tight pitch).

Wafer ID	Energy P [%]	Energy N [%]	ρ_{eff} [Ωcm]	Line loss at 30 GHz [dB/mm]	Comment
W01	100	100	76	0.67	N too deep relative to P
W02	90	100	45	0.94	N too deep relative to P
W03	**110**	100	400	0.41	Good balance with **deeper P**
W07	100	**90**	400	0.42	Good balance with **shallower N**
W08	100	110	25	1.26	N too deep relative to P

Table 2
RF Performance from M1LB CPW Lines of Wafer Splits in PN Implant Energy for Doses of 50 % (tight pitch).

Wafer ID	Energy P [%]	Energy N [%]	ρ_{eff} [Ωcm]	Line loss at 30 GHz [dB/mm]	Comment
W04	100	100	200	0.44	N too deep relative to P
W05	90	100	150	0.50	N too deep relative to P
W06	**110**	100	500	0.37	Good balance with **deeper P**
W09	100	**90**	540	0.36	Good balance with **shallower N**
W10	100	110	61	0.72	N too deep relative to P

neighbouring identical-polarity wells being in electrical connection with one another below the interposing opposite-polarity well, as depicted in Fig. 1d. By relaxing the pitch, fine control on the implant parameters is alleviated, at the cost of a little RF performance.

3.3. *Large-signal results*

Large-signal measurements of the CPWs were performed on-wafer using a dedicated setup by which a single tone with fundamental frequency of 900 MHz is injected into one port of the CPWs on each substrate [10,11]. The power of this input tone H'1, is swept from −30 dBm to +25 dBm, and the output signal's components H1 (fundamental), H2 and H3 (second and third harmonics) are retrieved and are plotted in Fig. 4 for several considered substrate variants.

Fig. 4 demonstrates that the harmonic components H2 and H3 decrease by around 20 dB when replacing the standard-resistivity substrate by a high-resistivity variant (with PSC).

On top of that, a further 30 dB can be gained in substrate linearity when adding the PN interface passivation solution.

4. Conclusion

In this paper, the PN passivation solution of HR interfaces has been integrated into an advanced industrial design flow, the 28 nm FD-SOI node from STMicroelectronics.

The impact of the PN implant energy and doses was presented, and all trends from the 10 presented wafers can be well explained based on the P/N depth balance set by the ratio of implant energies. These split-wafer studies give strong insight into the optimization paths for this passivation solution, and highlight the implant energies as critical process parameters, particularly when working with aggressive pitches.

The efficient countering of the PSC effect was well demonstrated

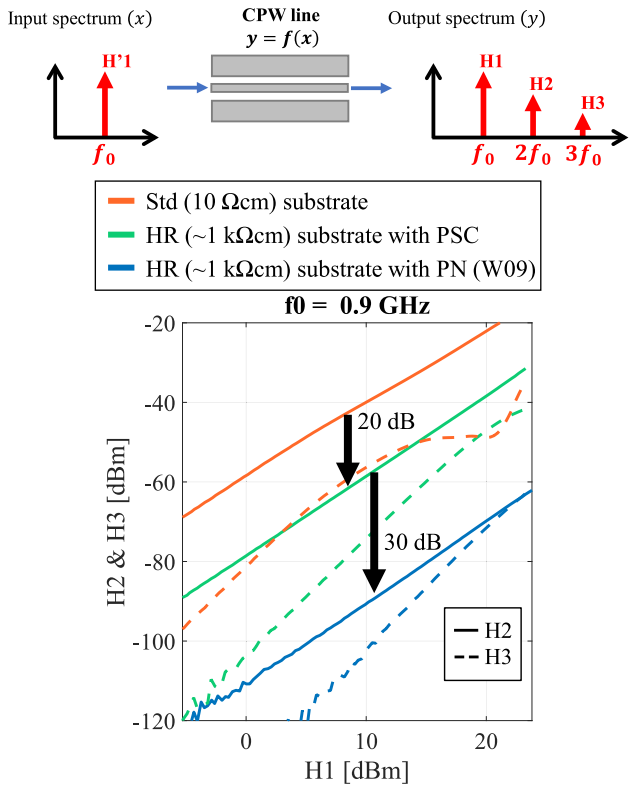

Fig. 4. Harmonic distortion levels at the output of M1LB lines.

through the small- and large-signal on-wafer measurements of two sets of CPW lines.

Strong improvements in substrate-induced losses and harmonic distortion levels were demonstrated.

Measured ρ_{eff} metrics above 500 (1000) Ωcm were achieved in CPW lines implemented in the M1LB (IBLB) layer stack, corresponding to a lineic loss reduction of 2.39 dB/mm (0.85 dB/mm) at 30 GHz compared to the reference standard-resistivity option.

Finally, correspondingly strong reductions in substrate non-linearities were also demonstrated, with a 20 dB reduction achieved by implementing a high-resistivity bulk wafer as compared to the standard resistivity potion, and a further 30 dB reduction achieved on top of that when passivating the interface with an efficient PN solution.

The PN-passivation solution is implementable at the foundry level and can be defined locally in the key areas of the chip (such below RF passives) that require reduced substrate losses and coupling.

CRediT authorship contribution statement

M. Rack: Writing – review & editing, Writing – original draft, Visualization, Validation, Software, Methodology, Investigation, Formal analysis, Data curation, Conceptualization. **M. Nabet:** Writing – review & editing, Investigation, Data curation. **Y. Bendou:** Writing – review & editing, Methodology, Investigation, Data curation. **M. Vanbrabant:** Writing – review & editing, Investigation, Formal analysis, Data curation. **M. Moulin:** Writing – review & editing, Investigation. **Q. Courte:** Writing – review & editing, Investigation. **S. Cremer:** Writing – review & editing, Supervision, Project administration, Methodology, Investigation, Conceptualization. **A. Cathelin:** Writing – review & editing, Supervision, Resources, Project administration, Investigation, Formal analysis, Conceptualization. **D. Lederer:** Writing – review & editing, Supervision, Resources, Methodology, Investigation. **J.-P. Raskin:** Writing – review & editing, Supervision, Resources, Project administration, Methodology, Investigation, Formal analysis, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgment

This work is supported by Ecsel JU project “Beyond5” (grant agreement No 876124) via EU H2020 and Innoviris (Brussels/Belgium) funding.

Data availability

The data that has been used is confidential.

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