Ultra-Thinned Individual SOI Die ACF FC Bonded on Rigid and Flex PCB

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Abstract—We have developed a straightforward die-level thinning process suitable for SOI dies. The process has been demonstrated on SOI CMOS die assembled on rigid and flexible PCBs using previously-developed anisotropic conductive adhesive flip-chip method. Unlike standard wafer-level thinning processes, in the demonstrated process the full thickness SOI die is directly mounted on PCB and after that thinned. The demonstrated process is simple and robust; it comprises fewer process steps compared to conventional die thinning process. The ultra-thinning process has no effects on the assembly integrity and device performance.

Keywords—Ultra-thinned SOI die, low-cost ultra-thinng, anisotropic conductive films, flip-chip bonding.

I. Introduction

Ultra-thin Si die is a key enabler for compact and miniaturized packages used for high-density 3D integration [1] that are required for various applications [2] such as memories, telecommunications, processors, multi-chip packages etc. The most common way [3] to obtain a thin die is through wafer thinning. The wafer is thinned down to a required thickness followed by wafer singulation [4]. Conceptually, wafer thinning process is simple, but its implementation is complex and costly, requires several process steps [5] such as wafer back-grinding (coarse and fine), followed by stress release. The process might comprise a combination [6] of chemical mechanical polishing and wet or dry etch, or both. Ultra-thin wafer handling [7], sequential singulation [8] are also complex processes. There are several ways to address that, the most common [9] is, prior to the wafer-level thinning to bond temporarily the full-thickness wafer to a corresponding wafer carrier. Then, the wafer is singulated together with the carrier. After the individual die mounting the carrier is removed [10]. The ultra-thin wafer characterization is also not straightforward and requires dedicated technique and metrology [10, 11]. On the contrary, there is no mature commercially available technique to perform thinning of an individual Si die, so-called thinning at die-level. Such die-level thinning would be required for low-scale manufacturing and niche applications where the dies come as already singulated e.g. from multi-project wafers.

In response to that, we have demonstrated a process flow that allows for mounting an individual CMOS silicon-on-Insulator (SOI) die on both rigid and flexible printed circuit boards (PCBs) by means of anisotropic conductive film (ACF) flip chip (FC) bonding and sequential thinning by dry etching. The process has no complex issues that are typically present during processing on the wafer-level, such as the thin wafer handling and singulation, does not require a complex dedicated metrology for the characterization. The demonstrated process is simple and robust; it comprises fewer process steps and limited processing equipment and characterization units compared to conventional die thinning process.

II. Test Material and Assembly

To demonstrate the concept, we used a 300 µm-thick test die processed at UCLouvain using CMOS SOI platform, featuring 12 pads of 250 x 250 µm^2 that are connected in pairs through conductive tracks for continuity qualification. The test die has an area of 2x2 mm^2. As test carriers, we used a 0.8 mm thick rigid FR4 PCB and a 25 µm polyimide (PI) PCB. For mounting the test die, we applied previously-developed [12] ACF FC process. As an interconnect material we used 40 µm-thick ACF 7376-10 manufactured by 3M^{TM}, loaded with gold plated polymer conductive particles of 10 µm diameter. The ACF FC bonding was performed by a submicron die bonder FINEPLACER Lambda from Finetech, using the following optimized bonding parameters: bonding force of 1.6 kgf (3.93 MPa) at 160°C process temperature, during 30 s. We measured the resistance of 6 individual daisy chains on each ACF FC assembly. After that, the assembled samples both on rigid FR4 and on flex PI PCBs were subjected to die thinning processing.

Examples of the test die ACF FC bonded to a flexible PCB are presented in the fig. 1.

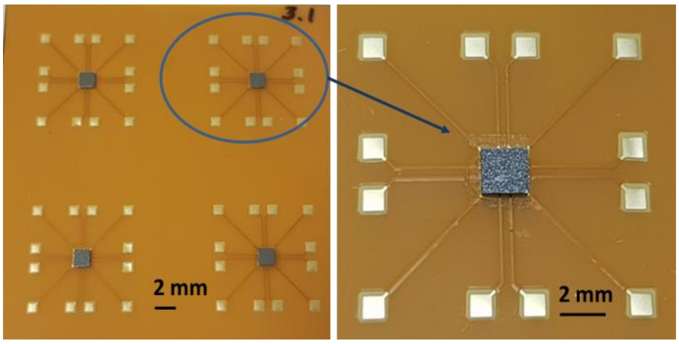

Fig. 1. Top view: 4 individual dies ACF FC bonded to flexible PCB panel of 10x10 mm^2 (left) and enlarged image of an individual die ACF FC bonded to flexible PCB.

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III. Die Thinning

The concept for an individual SOI die thinning is simple and illustrated schematically in the fig. 2.

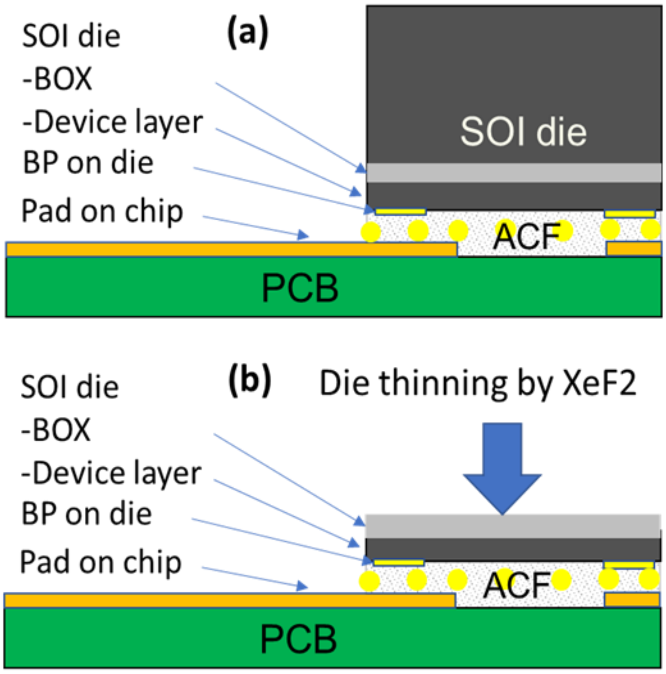

Fig. 2. Individual SOI die thinning concept.

Unlike standard wafer-level thinning processes where the full-thickness Si wafer is temporarily bonded to a wafer-size carrier, thinned down to a required thickness, singulated in individual dies, followed by an individual die mounting and finally the carrier removal; in the demonstrated process the full thickness SOI die is mounted by ACF FC on the rigid or flexible carrier and after that thinned.

Xenon fluoride (XeF_2) is a crystal at atmospheric pressure which sublimates at ~4 Torr [13]. As fluorinating agent, it can be used to etch silicon, extending the already large portfolio which contains dry or wet techniques, as respectively the Bosch process with deep reactive ion etching (DRIE) and the tetramethylammonium bath (TMAH) for example. XeF_2 presents the advantages of simple, dry (no stiction), plasma-free (less/no interface state defects), isotropic and highly selective ($Si:SiO_2$ >1,000:1) silicon etching method, following this chemical formula:

$$2XeF2 + Si \rightarrow 2Xe\ (g) + SiF4\ (g) \qquad [13]$$

The classical purpose is to use silicon as a sacrificial layer to produce released MEMS: cantilevers, bridges, diaphragms, etc. but in UCLouvain, we also used it to remove the back Si substrate of SOI wafers and chips till the buried oxide, precisely, without degrading the top SOI devices [14].

For flexible ultrathin chips (UTC), doing a thinning or a release after the packaging is not the conventional way. The three major methods are: (i) flip chip assembly of already thinned dies on flexible substrate, (ii) laminating UTCs between two flexible layers, (iii) UTCs on foil with printed connections [15]. Standard wedge/ball wire-bonding is not recommended due to risk of cracks into/through the fragile ultra-thinned dies.

Indeed, while XeF_2 Si etch selectivity against polymers, organic materials and packages is very high and mentioned in the SPTS Xactix equipment description [16], no scientific article, to the best of our knowledge, shows such a use of a post-packaged Si etch on FR4 PCB. However, gluing the die by ACF before thinning on flex or FR4 substrates allows to thin down to extremely small thickness, which would make the dies impossible to handle either. Especially the frequent case of compressive or tensile stresses into the stacked layers constituting the die leads to surface/volume cracks, or to the chip to roll up on itself.

The presented packaging method, even if particularly adapted to deformation sensing where the highest die compliance is desirable, is not limited to strain sensors. For all sensors requiring to be exposed to outside atmosphere (as pressure and gas sensors), it is feasible to position the die central sensitive part in front of a PCB via/hole, itself aligned with the same opening in the ACF. The die would be maintained by its ACF-glued periphery where all the pads are classically distributed. Optical sensors can either be exposed from this opening or have a backside illumination, the BOX being transparent to light [14].

To implement that, the whole assembly (ACF FC bonded individual die) was placed with the Si substrate facing the top, inside the Xactix vacuum etching tool, and isotropically etched in xenon difluoride (XeF_2) atmosphere at room temperature [17]. The full thickness die handling for flip chip (Fig 2.a), requiring pressure, heat and alignment, is not challenging for industrial tools. It is only after the XeF_2 etching itself (Fig 2.b) that the flexibility of the stack is greatly improved. The remaining 1.4 µm-thick test die comprises a 1 µm-thick Al device layer, separated by 0.4 µm of SiO2 buried oxide (BOX) after the complete etching of the Si supporting substrate, by ~50 120 s-long pulses of XeF2, at 4 Torr. Also, as mentioned, such gas does not etch the FR4 or PI layers.

After Si thinning, we re-measured the resistance of 6 individual daisy chains on each ACF FC assembly. The resistance value did not change and all assemblies survived the die thinning process.

IV. Test and Characterization

An initial step to control the ACF FC assembly after the die thinning process and the daisy chains measurements, was an observation in reflective visible light using Leica Z6APO optical microscope, with a magnification to 225x. The 0.4 µm thick BOX is transparent to visible light. Transparency of Si to the visible light depends on different factors such e.g. Si absorption and thickness, surface roughness and doping [18]. According to our observation, the ultra-thinned die is here highly transparent to the visible light, so that we can see easily through the die and inspect corresponding parts of the assembly, as illustrated in the fig. 3, confirming full Si substrate removal.

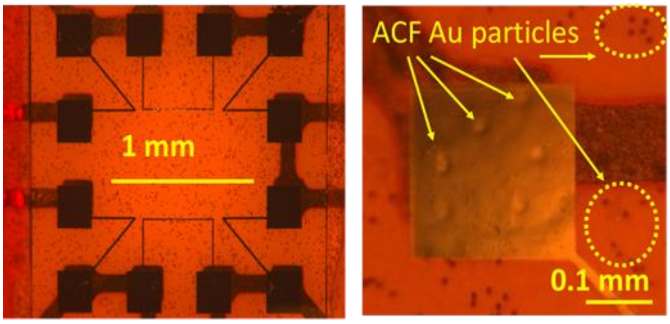

Fig. 3. Top view: Zoom in on the ultra-thinned test die ACF FC after XeF2 process, bonded on PI PCB (left), zoom in on the die bond pad bonded to the landing pad on PI (right).

The top view microscopic observation allows to assess the die alignment to the receiving PCB, reveals distribution of gold plated ACF particles and their contribution in establishing an electrical interconnection, and can also detect some potential assembly irregularities. The die top surface after thinning is highly transparent and using microscope we did not detect any irregularities, such die thickness variation, or Si non-etched debris on top of the BOX. For that and other characterizations, we need to use an additional technique.

For an accurate die thickness measurements, die thickness variation (DTV) and die surface roughness, we used contact profilometry. For that, we employed a stylus type profilometer Bruker, Dektak XT. The stylus tip diameter is 12.5 µm and the stylus force was as low as 3 mg to reduced impact of the stylus on results of profilometry scan. The profilometry scan on the ultra-thinned die ACF FC bonded on PI PCB is presented in the fig. 4.

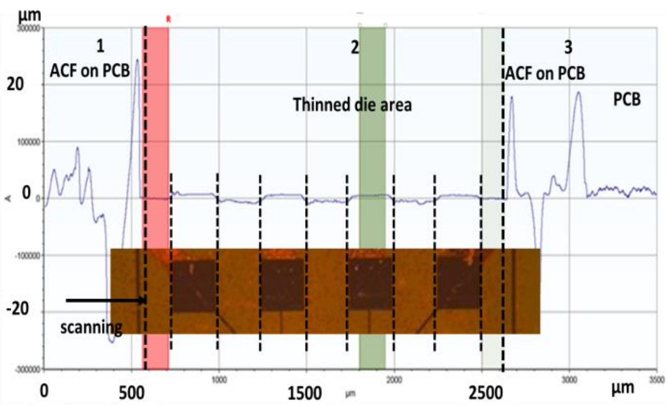

Fig. 4. Profilometry scan on the ultra-thinned die ACF FC bonded on PI PCB. Insertion: fragment of the test die and scanning direction.

In fig. 4, we distinguish:

- Section 1: Scanning over a transition zone from PCB surface to the die surface, on ACF, thickness variation up to 40 µm that corresponds to ACF thickness.
- Section 2: Scanning on the surface of the thinned die.
- Section 3: Identical to Section 1, it comprises part of PCB with ACF laminated and PCB part without ACF.

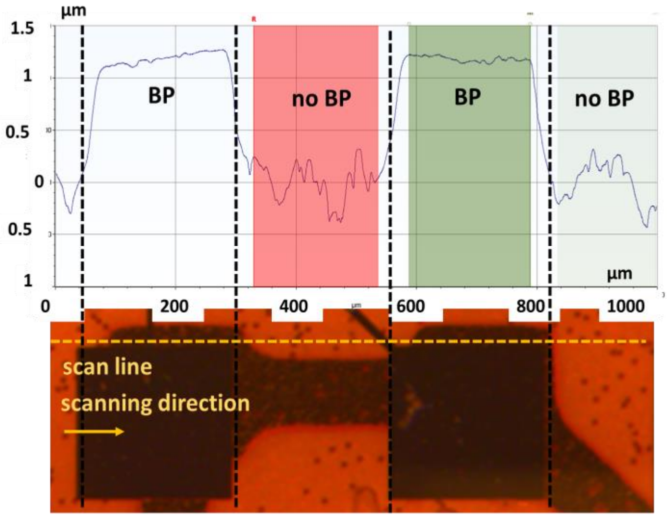

Fig. 5. Profilometry scan on surface of the ultra-thinned die ACF FC bonded on PI PCB, over two bond pads bonded on PCB landing pads. . Insertion: fragment of the test die and scanning direction.

In fig. 5, we observe 2 bumps on the die surface of 1.20 µm thickness corresponding to 2 Al bond pads of 1.00 µm thick on the die bonded to corresponding landing pads on PCB. The section 2 was used to measure the thinned die surface roughness.

On the die surface we have detected a die thickness variation (DTV) of 1.20±0.20 µm. Such DTV caused a deformation in device layer of SOI die because of stressed generated by ACF FC interconnection. In the area of the die out of BP we did not detect any DTV, we observed only micro-roughness as illustrated in fig. 5.

The micro-roughness scan was performed on a surface of the ultra-thinned die. Based on the micro-roughness value we have identified two areas: on top of the bonding pads and area free of the bonding pads. A result of the profilometry roughness scan on the surface of the thinned die is presented in table 1.

TABLE I. SURFACE ROUGHNESS CHARACTERIZATION OF THE TOP OF THE THINNED DIE.

Parameter	On BP area	On BP free area
Ra, µm	0.0228	0.0389
Rq, µm	0.0260	0.0506
Rp, µm	0.0342	0.0414
Rv, µm	0.0554	0.0697
Rmax, µm	0.0896	0.1111

Abbreviation list:
Ra - arithmetic average of absolute values
Rq - root mean squared
Rmax=Rp+Rv, maximum height of the profile
Rp – maximum peak height
Rv - maximum valley depth.

Based on the roughness characterization, we concluded that the die surface after thinning is very smooth and varies in terms of Ra from 0.0228 µm on the top of the bond pads to 0.0389 µm all over the die surface. The value of the roughness we measured is in line with roughness of the BOX layer. Slightly smoother

BOX surface on top of the bond pads can be explained by planarization effect of bonding together two relatively stiff parts by means of ACF, the bond pads on the die and the corresponding landing pads on PCB.

Based on performed characterizations, namely visible light microscopy and stylus type profilometry, we can conclude that all the 300 µm thick supporting Si on top of BOX was fully etched away during XeF_2 dry thinning processing leaving no Si residues on the BOX. We also did not detect any foreign material and/ or contaminants on top of the BOX. The surface of BOX is very smooth, the roughness is as good as Ra=0.0389 µm. We also did not reveal any changes to any part of the assembly such ACF, PCB both FR4 and PI caused by XeF_2 dry thinning processing that confirms high selectivity of silicon etch process. One can conclude that the ultra-thinned die processed using the described method, does not require a dedicated metrology for the characterization.

Additionally to that, we analyzed selected samples using a cross-sectioning method. The method is destructive and typically used for failure analyses, can help in detecting a versatile latent defects and other irregularities related to die mounting and eventually die thinning. The cross-sectioning method includes embedding a test sample in a molding compound for an accurate handling of an individual sample, followed by sequential polishing using abrasive paper set of different grids (starting from #600 to #4000) and finishing it with a final polish with diamond suspension of 0.5 µm diameter on a soft polishing cloth.

We cross-sectioned the ultra-thinned die assembled on the rigid PCB using ACF FC and a full-thickness die for a comparison purpose. The results are presented in the fig. 6.

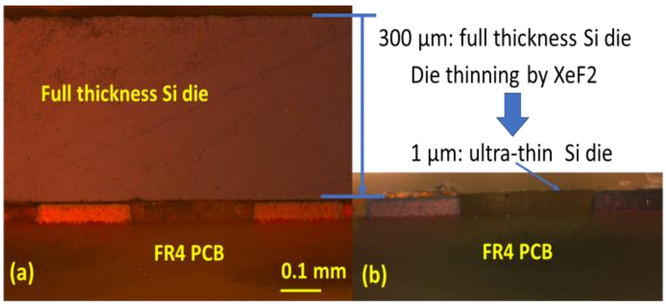

Fig. 6. Cross-sectional view on ACF FC bonded samples on FR4 PCB: full thickness Si die (a) and ultra-thinned Si die (b).

To detect more details on the ultra-thinned die bonded on PI PCB, we observed the samples at higher magnification, zoom in on the corresponding assembly parts of interest, as depicted in the fig. 7.

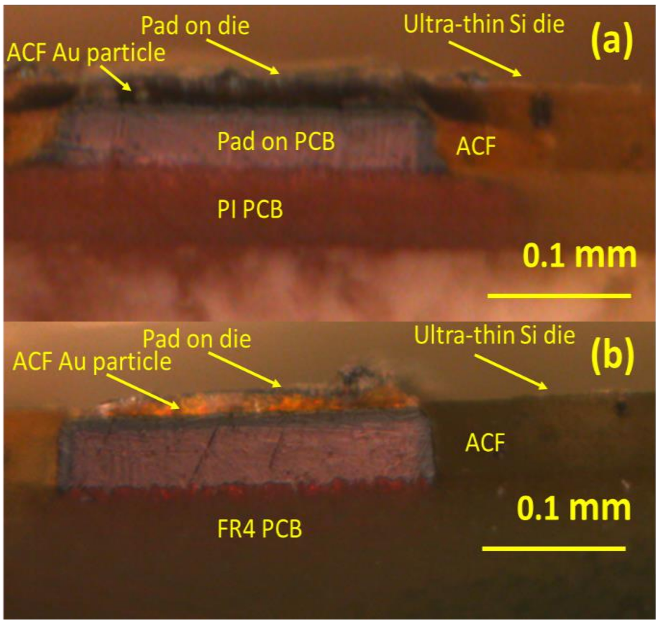

Fig. 7. Cross-sectional view on ultra-thinned Si die ACF FC bonded samples on PI (a) and FR4 (b) PCB.

We observed the interconnection area between the bonding pad on the die and the landing pads on PCB. Several gold plated ACF particles, between 4 and 6 take part in establishing an electrical contact. The ACF is evenly distributed and without air voids laminated on the surface of the PCB. In case of the flexible PCB it follows the substrate curvature. On the top of the ACF, one can see the ultra-thing SOI die, it is evenly bonded on top of the ACF. However, because of physical limits of the cross-sectioning method (diamond suspension of 0.5 µm diameter), we could not distinguish details on the ultra-thin die as Al bond pads, BOX and cannot detect other possible defects. Meanwhile, above-performed high-magnification reflective visible light microscopic top view ultra-thin die observation (fig.3, a) are sufficiently accurate to detect a possible cracks and other eventual irregularities in the ultra-thing Si die. To conclude about the cross-sectioning part, the method is effective to detect eventual failures and irregularities in ACF FC joint and not in the body of the ultra-thin die.

V. Conclusion

We developed and successfully demonstrated die-level thinning process suitable for SOI dies. The process has been demonstrated on 300 µm thick SOI CMOS die assembled on rigid (FR4) and flexible (PI) PCBs using anisotropic conductive adhesive flip-chip bonding process. In the demonstrated process the full thickness SOI die is directly mounted on PCB and after that thinned by XeF_2 etch at atmospheric pressure. The XeF_2 etch is highly selective Si etchant, etches Si and stop on BOX. It does not affect other part of the assembly. The ultra-thin die processed using the method has a die thickness variation less than 0.2 µm and the die surface is very smooth, the roughness is as good as Ra=0.0389 µm. The proved that a simple visible light optical microscope observation and contact profilometry is sufficient for the ultra-thinned die characterization. It is also sufficient to perform a failure analyses. The thinning process comprises fewer process steps compared to a conventional die thinning process on a wafer level. Based on of 6 individual daisy chains resistance measurements on each ACF FC assembly before and after thinning, we proved that the demonstrated ultra-thinning process has no effects on the assembly integrity and device performance.

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