Modelling of Advanced Silicon-Based Substrates for RF and mm-Wave Applications

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Abstract

At high frequency, the accurate modelling of parasitic elements is crucial to IC design.

Substrate behavior is a significant contributor to such parasitics, and its modelling is a challenge, not only under small-signal conditions due to strongly non-uniform resistivity profiles in semiconductor materials, but especially under large-amplitude excitations.

In this work, substrate impact on a variety of pertinent integrated devices is studied, under both small- and large-signal conditions.

To do so, the effective resistivity and linearity parameters are defined as RF substrate figures of merit, and their extraction procedures are described.

These figures of merit serve as reliable indicators of substrate loss, coupling, and induced signal distortion. It is required that such considerations be kept under careful control in front-end circuitry for advanced telecommunication applications that have stringent spectral cross-contamination specifications between adjacent communication bands.

In this thesis, both small- and large-signal modelling approaches are developed to account for such substrate effects.

The developed models are heavily based in material semiconductor physics, and, in this work, the physical charge-balance interplay is rigorously studied, shedding light on the inner workings of a wide range of silicon-based substrates under both quasistatic and strong non-equilibrium transient conditions.

In particular, the developed large-signal modelling scheme is demonstrated to be stable, i.e. to converge in both space and time, and to correlate well to a wide set of measurement data from over 20 different silicon-based substrates.

The impact of each considered parameter, be it a material parameter (traps, doping, interface charge, etc.), an excitation parameter (signal amplitude, frequency, etc.), or an environment parameter (temperature, dimensions/layout of the structure, etc.), is not only well captured by the model, but beyond that the data trends can be fully explained thanks to the deep physical understanding developed throughout this text, based on a set of key concepts such as *Fermi-level pinning*, *finite carrier inertia*, *drift and recombination time constants*, *partial equilibrium*, *available free carriers*, etc.

After applying the physical analyses to the most widespread flavors of RF

substrate solutions, i.e. high-resistivity-types and trap-rich-types of wafers (commercial 300 mm samples from Soitec and university-fabricated samples), the models are used to develop and optimize novel RF substrates.

Two novel interface passivation schemes of HR-Si are presented, the first based on P and N surface implants, and the second on substrate interface potential control through the field-effect. Furthermore, two bulk passivation schemes are presented, the first based on the introduction of deep-level traps in all silicon regions by doping with Gold (Au) atoms, and the second based on the porosification of the silicon bulk. All four of schemes are demonstrated as being viable through simulations and by measurements of fabricated prototype wafers.

Beyond being of use for developing RF substrate solutions at the material level, the simulation approach is relevant to the design of RF and mm-wave circuits and systems. As of yet, no satisfactory large-signal modelling tool is available that can capture substrate-induced signal distortion effects. The combination of the model outputs with a full-wave EM simulator is proposed as a perspective to this work in the final chapter as a potential design flow to be of practical use to the RFIC design community.

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Introduction

Context

Silicon-based technologies present a cost and volume-manufacturing advantage over other materials thanks to a high maturity of silicon processes available on 300 mm diameter wafers.

Today (2020), the most advanced CMOS nodes, and in particular the SOI flavors, are boasting impressive high-frequency figures of merit, proposing an attractive path for cost-effective mass market productions of RF and mm-wave applications, including 5G, connected objects and smart sensors (Internet of Things), radars, etc.

To enable advanced telecommunication schemes (4G, 5G, etc.), the aggregation of multiple frequency bands is employed in order to achieve high data throughput. This brings about several challenges with regards to band isolation, as the aggregation of spectra with close frequencies imposes higher performance requirements from RF components, especially in terms of isolation and linearity, both of which are sources of spectral cross-contamination between bands. As a consequence, circuit linearity specifications become more stringent with each new generation of network standard.

At the circuit level, an increased number of supported bands translates directly into an increased complexity in the architecture of RF front-end modules. Support for multiple bands in a mobile device requires a complex array of filters and switches with high throw counts to route signals to and from the antenna(s) to the main RF transceiver(s). Within these circuits, careful considerations must be given to ***RF path loss***, ***signal cross coupling*** (crosstalk), and ***non-linearity*** to ensure the fidelity of the signal being processed.

These issues depend on the device performance, but are also critically impacted by the substrate properties at high frequencies. For these reasons (among others) SOI is well suited to high-frequency applications, thanks to its low parasitic architecture that enables a decoupling of active device optimization from the engineering of the underlying substrate materials, thanks to a physical separation by the *buried oxide layer*.

Motivation for this Work

From those considerations stems the motivation for this work: the small- and large-signal modelling of silicon-based substrates for RF and mm-wave applications.

RF path loss is fundamentally due to lossy materials. At RF frequencies, the electromagnetic fields due to signals propagating in integrated passive components (such a coplanar waveguides, spiral inductors, baluns, etc.) penetrate into the silicon substrate materials. If substrate *effective resistivity* is not well tailored (i.e. too low), then RF power is dissipated within these materials by Joule effect.

Furthermore, ***signal coupling*** through the substrate is also facilitated by low *effective resistivity*.

On top of these linear considerations, RF circuits that behave in a ***non-linear*** fashion are usually undesirable in a system chain, as non-linear elements introduce signal distortion between the input waveform and the output waveform. In the frequency domain, this corresponds to a smearing of the spectral content, with distortion components being generated outside of the initially allocated band. Advanced telecommunication schemes have stringent linearity specifications, and this linearity burden is applied to all levels of the RF chip: from the behavior of the active devices as well as to the substrate material. Semiconductor materials are non-linear by nature, as their local electrical properties depend on the electric field that penetrates them. It is then required to take substrate non-linearities into account when working at high frequencies and/or with sensitive signal modulation techniques.

This work aims to present the various linear substrate modelling approaches for semiconductor substrate stacks. At high frequencies, electromagnetic (EM) field-solver tools are required to capture the distributed nature of the integrated devices, as they present features of significant size relative to the signal wavelength. Such tools consider all materials as linear elements described by ρ, ε and μ and solve for Maxwell's equations. However, silicon's resistivity is E-field-dependent $\rho(E(x,y,z))$, and the E-field space-dependent (and also time-dependent under large-signal excitations). Obtaining the $\rho(x,y,z)$ usually requires a TCAD tool that solves for semiconductor transport equations. In practice, results from both types of tool are used for the small-signal modelling of semiconductor substrates.

Objectives

When the E-field becomes time variant, substrate response is pulsed through different (non-equilibrium) states of impedance, giving rise to non-linear signal distortion. The non-linear modelling is a challenge, as coupling Maxwell's equations with transport equations results in a complex formulation.

This work aims to provide a **non-linear RF substrate simulation methodology**, heavily **based on material parameter** inputs, such as interface charge, doping levels, trap distributions, temperature, etc.

Beyond providing a model, another goal of this thesis is to provide **strong insight into the physical mechanisms** at play in semiconductor RF substrates under both static and dynamic large-amplitude excitations, and to deeply understand the impact of fundamental material parameters on signal distortion levels.

Physical insight and accurate modelling of such non-linear substrate effects are desirable to the industry **for the development of novel substrate solutions**, and for understanding the impact of various process microfabrication steps and choices on **substrate quality for RF applications**.

Finally, adapting the results of the large-signal physical model into a compact equivalent impedance type of formulation is of high **interest to the RFIC design** community to account for the **non-linear behavior and impact of the substrate** on a full post-layout circuit simulation **within the IC design framework**.

Structure of the Thesis

This thesis is organized as follows :

Part I RF-SOI: Technology and Substrates

This part aims to paint a global picture of SOI's place in the RF world. After a brief review of SOI devices, the focus is shifted to the substrate's impact on RF circuitry, and established small-signal RF modelling approaches are presented.

Chapter 1 provides an overview of SOI technology for RF and mm-wave telecommunication applications. At the transistor level, SOI's architecture, electrostatics, and RF figures of merit are summarized. Then, at the RF-IC level, a review is made to reveal the position of SOI for key RF and mm-wave circuits (switches, LNAs and PAs).

Chapter 2 describes substrate impact at RF frequencies on a wide range of integrated passive devices. The methodology for extracting the small-signal FoM of *effective resistivity* is presented. Then, the main flavors of SOI substrates are reviewed, and substrate requirements at RF are highlighted, as they impact parasitic coupling, RF losses, and non-linear signal distortion.

Part II Substrate Modelling Techniques

This part describes the core work of this thesis: understanding the physical mechanisms at play in a semiconductor substrate under large-amplitude RF excitation, with the goal of modelling substrate-induced non-linear signal distortion in overlying circuitry.

Chapter 3 provides a solid understanding of the necessary semiconductor physics. Static analysis based on TCAD tools give strong insight into the charge-balance interplay between fixed oxide charge, applied signal, a parasitic surface conduction layer formation and/or the ionization of trap-rich types of passivation layers. Rigorous RF dynamic analyses are then considered, which deliver strong physical understanding of carrier and trap inertia and their finite response times.

Chapter 4 builds on this understanding to develop a large-signal model capable of evaluating substrate-induced harmonics at the output of a CPW line that is excited by a large-amplitude RF signal at its input.

Part III Advanced Substrate Characterization

In this part, extensive on-wafer RF characterizations of a multitude of silicon-based substrates are performed. These serve to validate the large-signal model over a wide range of parameters.

Chapter 5 presents the correlation results of the developed large-signal model to measurement data of CPW lines on 20 different silicon-based substrates. Good correlation is observed for samples with a wide range of material properties (doping, interface charge, traps, etc.), and measured under a wide range of conditions (temperature, excitation frequency, CPW geometry, etc.). These results then lend high confidence to the developed model.

Part IV Perspectives and Conclusion

Chapter 6 offers a perspective methodology to extend the non-linear substrate modelling to any arbitrary layouts, beyond uniform CPW lines. With this methodology, an integration path for the large-signal substrate model into a flow of IC design tools becomes foreseeable. The proof-of-concept of the proposed approach is demonstrated by comparing its results to on-wafer HD measurements of passive two port devices (that are significantly different from CPWs).

Chapter 7 is dedicated to reviewing the global conclusions of this thesis, and to offer perspective future endeavors in line with the presented work.

Appendix Advanced RF Substrate Solutions

Chapter 8, which is situated in the **Appendix** is dedicated to exploring and presenting alternative silicon-based RF substrate solutions, other than the mainstream high-resistivity and trap-rich substrates. Indeed, extensive research exists on other silicon-based solutions, and this chapter then aims to review all relevant solutions. In particular, several novel substrate solutions developed as part of this work are presented.

I RF-SOI: Technology and Substrates

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Overview of Part I

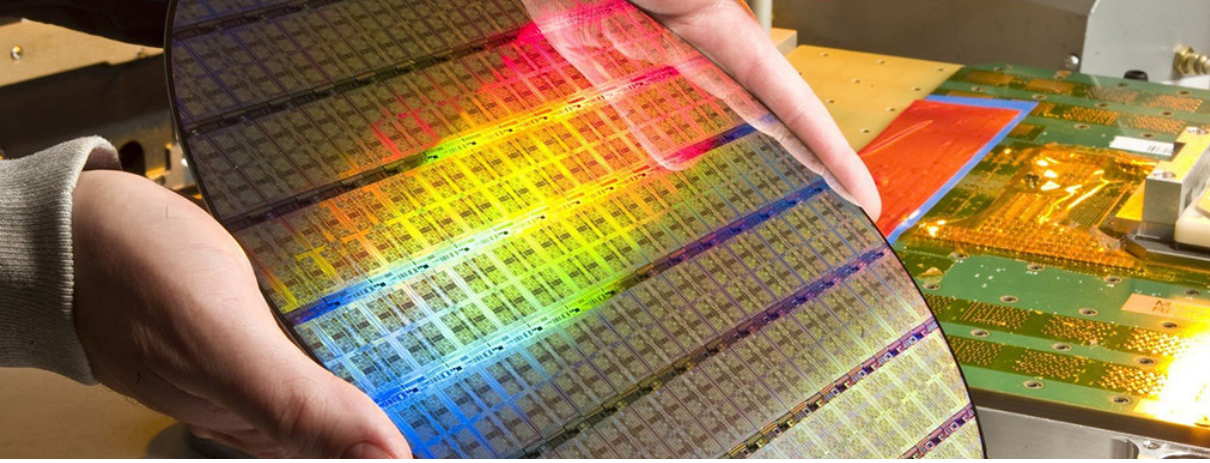
In **Part I** of this thesis, an overview of silicon-on-insulator (SOI) technology for radio-frequency (RF) and mm-wave telecommunication applications is presented.

At the transistor level, thanks to SOI's low-parasitic architecture and good electrostatics, high oscillation and cut-off frequencies in the range of 400 GHz are achieved for the latest SOI technologies.

At the RF-IC level, a review is made to reveal the position of SOI for key RF and millimeter wave circuits (switches, LNAs and PAs). Overall, SOI is shown to be a prime candidate not only for high-performance millimeter wave and 5G applications, but also for low-power RF IoT.

The substrate's impact at RF frequencies on a wide range of integrated passive devices is then investigated, and the methodology for extracting the small-signal FoM of *effective resistivity* is presented.

The main flavors of SOI substrates are reviewed, and substrate requirements at RF are highlighted, based on concerns related to parasitic coupling, RF losses, and non-linear signal distortion.



1. SOI Technologies Towards RF and Millimeter Wave Applications

This chapter reviews SOI's potential for RF and mm-wave applications at the transistor level. Both PD-SOI and FD-SOI architectures are presented, and their RF performances are highlighted. A literature-based review of state-of-the-art SOI RFICs is performed, demonstrating the growing traction SOI platforms have in the RF and mm-wave sector.

1.1 SOI Devices

1.1.1 Device Architecture and Electrostatics

SOI devices are metal-oxide field-effect transistors (MOSFETs) that differ from conventional bulk CMOS devices in that the transistor channel is located above an electrical insulator that separates the transistor silicon from the substrate silicon. Compared with planar bulk CMOS technology, SOI achieves better electrostatic control of the transistor channel by isolating it from the silicon substrate by means of a buried oxide (BOX) layer.

The insulating BOX layer also greatly enhances lateral and vertical isolation, and reduces source and drain capacitances, minimizing the total dynamic operation power and/or increasing switching speeds. Furthermore, these capacitances in SOI are more linear, due to the inexistence of PN junctions that constitute the substrate isolation scheme in bulk CMOS. Finally, the BOX isolation also leads to improved latch-up free operation and reduced leakage current **[1, 2]**.

Two main flavors of SOI devices exist: (i) partially-depleted (PD-) SOI and (ii) fully-depleted (FD-) SOI for the most advanced nodes. PD-SOI is

characterized by an active silicon film typically thicker than 50 nm while FD-SOI has an active silicon thickness roughly below 10 nm. In A PD-SOI MOSFET, the vertical space charge region induced by an applied gate voltage does not extend over the entire thickness of the active silicon layer, and a volume of unmodulated silicon (body) remains below the device's channel. In an FD-SOI however, the film is so thin that the entirety of the active silicon layer is modulated by the gate voltage. Both types of SOI devices are depicted in **Figures 1.1 and 1.2**.

PD-SOI devices scale down to roughly 30 to 40 nm gate length, with the 180 and 130 nm nodes being today's mature technologies heavily adopted by the industry, and which have already been successful in RF applications. Such devices are named partially-depleted due to the active silicon thickness not being modulated by the applied gate voltage deep in the SOI film, that is named the transistor's body region. If the body region of a PD-SOI device is left floating, an undesirable *kink effect* appears in the output current-voltage characteristics of the device. Due to a high electric field present near the (biased) drain region the electrons of the channel (in an NFET) acquire high kinetic energy and create electron-hole pairs by impact ionization. The generated electrons are collected by the drain but the holes accumulate in the floating body. The accumulation of these holes in the body leads to an increase in the body potential, which in turn provokes a drop in the device's threshold voltage, leading to a sharp increase (kink) in the drain current, and therefore to a strong non-linearity in the output conductance g_d **[3]**. To remedy the kink effect, a solution is to provide a body contact to enable an evacuation path for the generated holes. The PD-SOI transistor is then a four-terminal device (gate, source, drain and body).

While an applied DC or low frequency potential can be well established at the body node, the nonzero value of the body contact resistance leads to a loss of body potential control at RF frequencies. For these reasons, a frequency dependency is observed in the output conductance g_d, which is strongly degraded above a few hundred megahertz **[3–5]**.

The kink effect is not present in FD-SOI devices, as the active silicon layer is so thin that no body region exists beneath the inversion channel.

A sub-category of FD-SOI devices is ultra-thin body and BOX (UTBB) that is further characterized by a thin BOX layer, typically in the range of 20 to 25 nm. A typical cross-sectional view of a UTBB-FD-SOI transistor is shown in **Figure 1.2 (b)**. UTBB devices allow the option to include a back-gate electrode defined beneath the BOX layer. This is typically achieved by doping a region

below the BOX to define a conductive well that is then vertically contacted through the BOX. Since the BOX layer is very thin, a bias potential applied to the back-gate contact has the effect of modulating the transistor channel, which is a very interesting feature enabling threshold voltage tuning of the device.

Figure 1.2 (b) also shows that the source and drain regions are raised in FD-SOI devices. They are fabricated by epitaxial growth to facilitate the silicidation process, by which a metal-silicon alloy is created in the source and drain regions to lower the series contact resistances associated to these terminals.

Compared with bulk devices, we can cite the following advantages of FD-SOI **[6]**: improved electrostatics and control of short channel effects that result in much lower subthreshold slope and DIBL, and reduced off-state leakage current by two orders of magnitude. Better channel control and reduced short-channel effect (including parasitic source-to-drain coupling through the substrate) in FD-SOI results in reduced output conductance by a factor of approximately two compared with bulk. Thanks to this reduction in output conductance, FD-SOI outperforms bulk in terms of voltage and power gain.

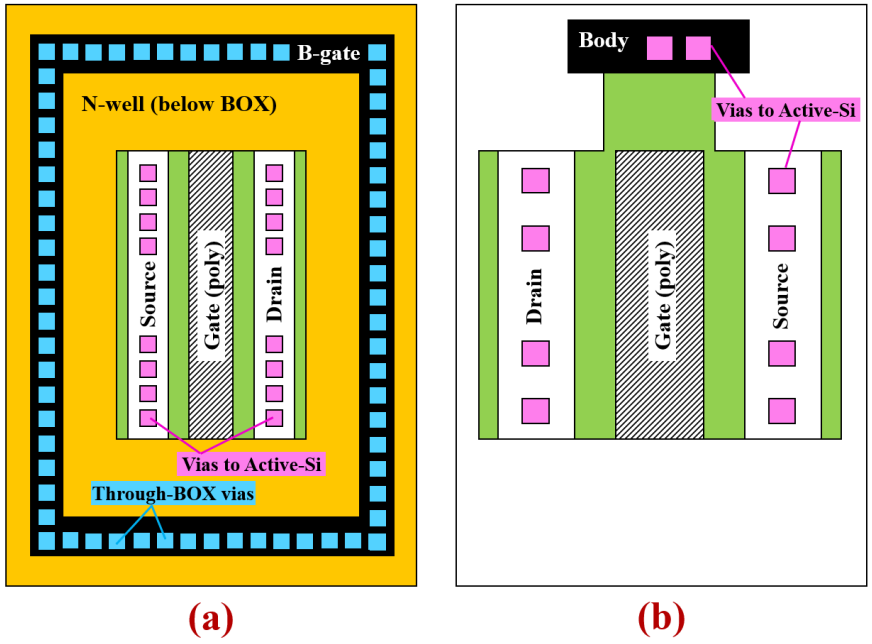


Figure 1.1: Top views of state-of-the art **(a)** FD-SOI and **(b)** PD-SOI NMOSFETs. The green regions depict the active SOI film above the BOX.

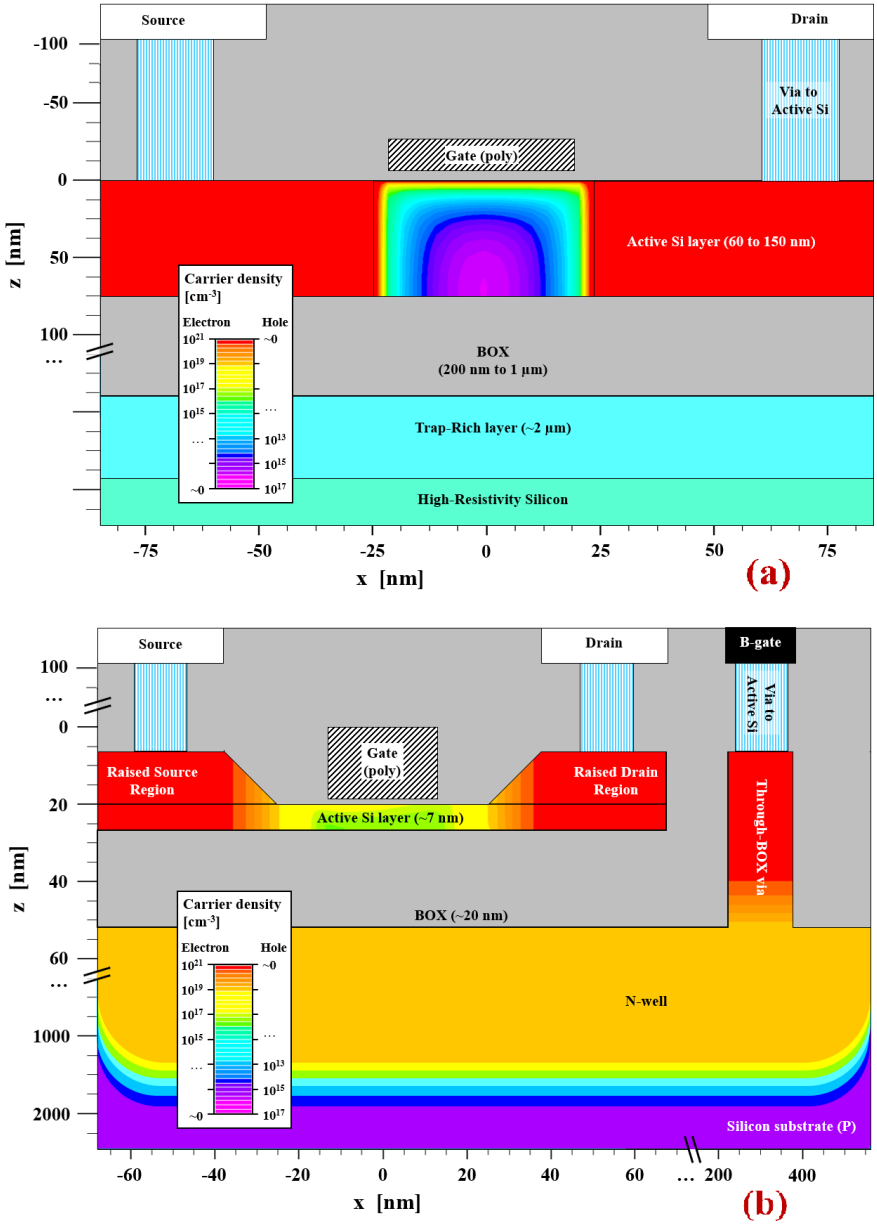


Figure 1.2: Cross-sectional view of a state-of-the art SOI NMOSFETs. **(a)** PD-SOI on trap-rich substrate. **(b)** 22 nm (SLVT) UTBB-FD-SOI, including raised source and drain regions and back-gate contact well definition.

1.1.2 A Brief History of SOI Devices

SOI's low-power performance made the technology highly attractive for digital applications, with IBM bringing the industry's first PD-SOI-based processors to the stage in 2000. Shortly after, from 2001, AMD adopted SOI for all of its x86 microprocessors. Since then, IBM continued to use SOI for many of its in-house processors and its ASICs, including CPUs at the 90 nm node for the *PlayStation 3*, *Xbox 360*, and *Nintendo Wii* game consoles. AMD rode SOI technology from 130 nm all the way down to 32 nm, and, after spinning off from AMD, GlobalFoundries continued to manufacture AMD's SOI designs [7].

On the RF side, starting from 2008, SOI steadily displaced Gallium-Arsenide (GaAs) and Silicon-on-Sapphire (SOS) technologies to become the mainstream technology for implementing RF switch banks in mobile applications. By 2014 PD-SOI accounted for more than 85% market share for mobile antenna switches [8].

In 2014 STMicroelectronics deployed its new 28 nm FD-SOI process, and licensed the technology to Samsung as a second source. GlobalFoundries also licensed ST's FD-SOI technology. But instead of bringing it directly to production, GlobalFoundries melded the technology with its own SOI developments and advanced fabrication techniques to create a 22 nm FD-SOI technology [7]. GlobalFoundries' process, called 22FDX^{TM}, implements a compressively strained channel using SiGe for the PFETs to enable its PMOS device to reach speeds and gains close to its NFETs. In 2015, GlobalFoundries acquired IBM's fabs, lending it even more SOI capabilities.

At the time of writing (2020), the most advanced FD-SOI nodes are offered by GlobalFoundries at the 22 nm node and by STMicroelectronics and Samsung at the 28 nm node. Furthermore, GlobalFoundries' highly-advanced partially-depleted (PD) 45 nm RF-SOI is greatly optimized for high-frequency performance (including at the substrate level).

1.1.3 High-Performance RF and Millimeter Wave PD- and FD-SOI

Aggressive gate-length downscaling of MOSFETs has been the main stimulus for the growth of the integrated circuit industry. This downscaling, which has proved beneficial to digital circuits, is primarily the result of the need for improved circuit performance and cost reduction and has resulted in tremendous reduction of the carrier transit time across the channel, thereby resulting in very high cut-off frequencies [9, 10].

It is only in recent decades that CMOS devices have been considered as a radio frequency (RF) technology of choice. Indeed, with the continuous gate length downscaling, the most advanced SOI nodes are now boasting speed performances that rival the established ultra-fast high-electron mobility transistors (HEMTs).

Such HEMT devices, which have been widely adopted in RF telecommunications applications since the 1980s, owe their success to their inherent high speed, enabled by their unique architecture that takes full advantage of the intrinsic high carrier mobility of the III-V materials that they are based on, typically GaAs, GaN or InP.

Nowadays, the most advanced PD- (45 nm) and FD-SOI (28 nm and 22 nm) nodes are boasting speed metrics that are entirely sufficient for RF and even mm-wave applications, opening SOI to an RF market beyond switches.

Figure 1.3 presents the state of the art current gain cut-off frequency f_t and maximum oscillation frequency f_{max} for N-type SOI MOSFETs as a function of gate length **[10, 11]**, with the dashed lines being the prediction from the International Technology Roadmap for Semiconductors (ITRS) **[12]**.

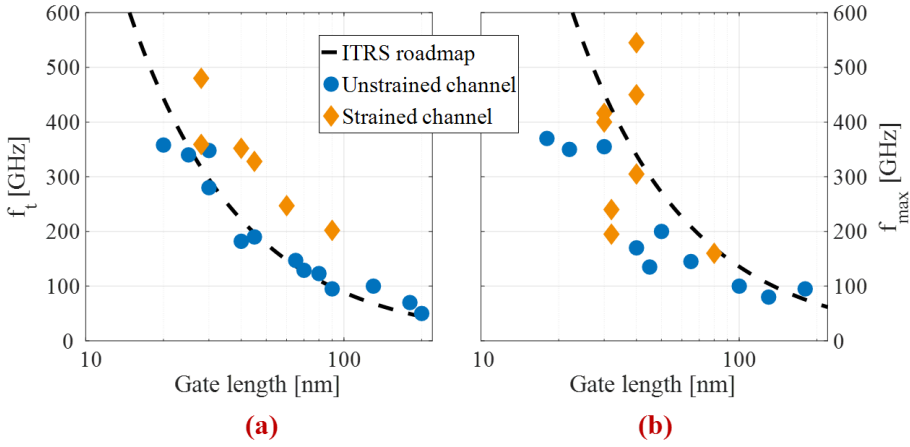


Figure 1.3: (a) Current gain cut-off frequency f_t and **(b)** maximum oscillation frequency f_{max} as a function of gate length for state of the art unstrained and strained SOI NMOSFETs.

Silicon-based devices are inherently slower than III-V transistors due to naturally lower carrier mobility. However, the mobility in silicon MOSFETs can be enhanced for electrons in N-FETs (holes in P-FETs) by applying tensile

(compressive) strain to the device's channel using silicon-carbide (silicon-germanium). SOI devices with strained channels therefore presented boosted f_t and f_{max} metrics, as shown in **Figure 1.3**. Despite the lower carrier mobility in silicon compared with III-V materials, short-gate silicon MOSFETs can be considered as competitive technologies for high frequency applications, with cut-off frequencies and maximum oscillation frequencies in the 300 to 400 GHz range **[13–15]**, easily enabling key telecommunications modules at millimeter wave frequencies up to 100 GHz (as will be presented in **Section 1.2**).

For these reasons, advanced PD- and FD-SOI technologies are strong candidates for mm-wave applications in the 5G era.

1.1.4 Multi-V_T and Low-Power FD-SOI

5G is not the only RF sector in which FD-SOI is likely to bloom. Indeed, thanks to low power capabilities, it is a prime candidate for Internet-of-Things (IoT) applications, that will for the most part require low data throughput, but in which low-power is essential, as well as large volume manufacturing capabilities at low costs. Indeed, thanks to its high ratio of transconductance to drive current (g_m/I_D) FD-SOI can significantly reduce consumption in circuits such as power amplifiers and RF dividers **[7]**. The FD flavor of SOI technology can produce very short devices with very low threshold voltages that are desirable for low-power and IoT applications.

For a given off current target, FD-SOI can have a lower threshold voltage (V_T) than bulk MOSFETs. Lower V_T is attractive in order to attain higher overdrive voltage ($V_{OV} = V_{GS} - V_T$) and therefore higher drive current. Alternatively, one can trade-off the drive current with power consumption. In other words, FD-SOI can provide the same drive current at lower supply voltage (V_{DD}), resulting in reduction in both active power (proportional to V_{DD}^2) and standby power (proportional to V_{DD}).

To enable the designs of low power and high-performance Systems on Chip (SoCs), it is essential for a technology platform to offer transistors with a wide range of threshold voltage options V_T **[16]**.

In conventional bulk CMOS, multi-V_T options are mainly achieved through the use of different channel doping options. However, such a technique has disadvantages when implemented in advanced nodes because the (short) channel's electrical behavior becomes more sensitive to random doping fluctuations (RDF).

However, in FD-SOI, devices of various V_T can be built by employing

different doping polarities of the wells created beneath the thin BOX, while preserving an undoped channel (uniform 10 Ωcm P-type from SOI wafer providers) and minimizing RDF.

This scheme is represented in **Figure 1.4**, and switching the polarity of the well produces a shift of approximately 100 mV in the V_T of the transistor **[17–20]**, for usual UTBB-FD-SOI BOX thicknesses of 20 to 25 nm.

Regular V_T devices (RVT) are obtained using conventional wells (well polarity opposite to S/D polarity), while flipped wells (well polarity the same as S/D polarity) are used to obtain low V_T devices (LVT).

These doped wells beneath the BOX layer are electrically connected to define the so-called back-gate contact, as is shown in **Figure 1.2 (b)**. Then, transistor V_T can be tuned even further by applying different well biases. Applying well biases up to ± 3 V produces V_T control of up to ± 250 mV **[21–23]**. Forward biasing a flipped well device will yield a low V_T (LVT) transistor, and reverse biasing a conventional well will yield a high V_T device (HVT).

While a constant well bias produces a fixed V_T, a dynamic biasing scheme may be implemented to manage real-time circuit performance, such as tuning antenna RF matching circuits in a real-time stochastic environment **[24]**.

One major advantage of FD-SOI's back gate functionality if to tune device threshold voltages to compensate for process-voltage-temperature (PVT) variations using adaptive biasing schemes **[14, 25]**. Thanks to the back-gate, ultra-low power devices are offered in FD-SOI, and biasing techniques towards strong energy efficiency optimization are achievable **[25, 26]**.

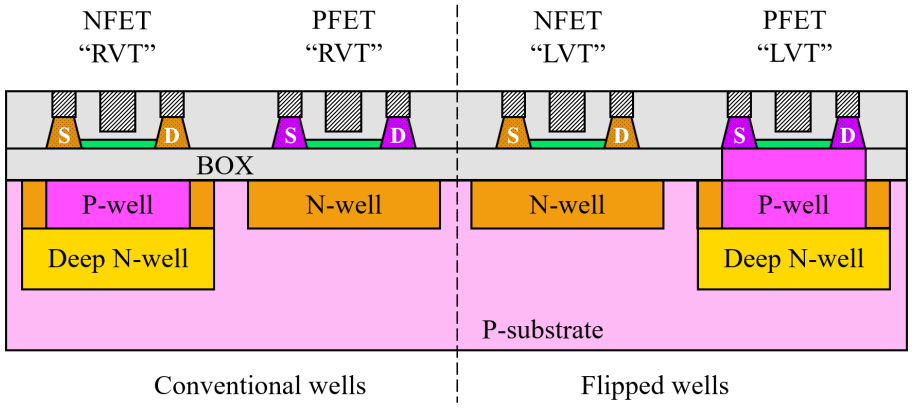


Figure 1.4: FD-SOI transistors built over conventional and flipped wells.

Though the back-gate functionality provides several advantages, in some cases it is worthwhile to avoid its definition in order to reduce parasitics through the substrate. This is the case for mm-wave switch applications at frequencies above 40 GHz in the 22FDX^{TM} technology from GlobalFoundries. Indeed, as shown in **[27–29]**, the back-gate adds shunt admittance between the substrate and the source and drain of the device, adding a shunt leakage path to ground that deteriorates high-end mm-wave performances of SLVT switches. Then, the use of a BFMOAT device is advocated in **[27–29]** for implementing switch modules above 40 GHz instead of SLVT devices. **Figure 1.5** illustrates the three flavors of N-FET FD-SOI devices designed for mm-wave applications, that highlights that the NFET BFMOAT device has no wells implanted below the BOX and therefore no back-gate contact. Though SLVT outperforms BFMOAT below 20 GHz thanks to the back-gate potential which enables a reduction in channel ON-resistance, BFMOAT is the device of choice above 40 GHz as parasitics due to the back-gate begin to seriously impact RF current leakage towards the substrate **[29]**.

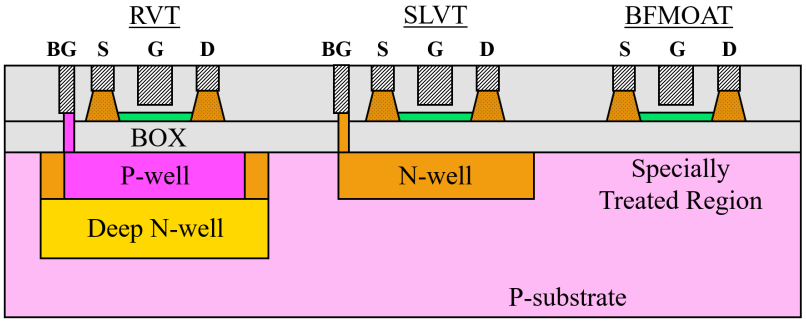


Figure 1.5: Representation of the three different flavours of RF/mm-wave NFET UTBB-FD-SOI devices.

1.2 State of the Art SOI RFICs

1.2.1 RF Front-End Modules: History

In the past decade SOI technology has been hugely successful in the RF world. Indeed, research interest in SOI telecommunication switches started at the dawn of the 21st century.

In these early days of 3G/4G adoption, interest grew in a new technology that could achieve RF switch performances similar to III-V devices, while providing sufficient manufacturing capacity to meet the expected market demand, and at a lower cost than was offered by the III-V industry **[30]**.

In 2008, RF-SOI started to take off, accounting for a modest 10% of switching modules in handsets. Until that point, GaAs based modules and PIN diode technologies were used for RF switching functions.

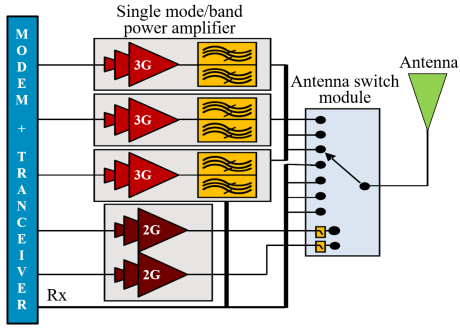
The key characteristics that have solidified RF SOI's role in mobile FEMs are **[30]**:

1. Device stacking ability for higher voltage handling.
2. Low on-resistance (R_{on}) for reduced insertion loss.
3. Low off-capacitance (C_{off}) and substrate parasitics for high isolation.
4. Logic and digital control integration.
5. Lower cost and improved economics over III-V technologies.
6. Large-scale silicon manufacturing capabilities.
7. Development of highly linear and low-loss substrate solutions **[31]** (more on this in **Chapter 2**).

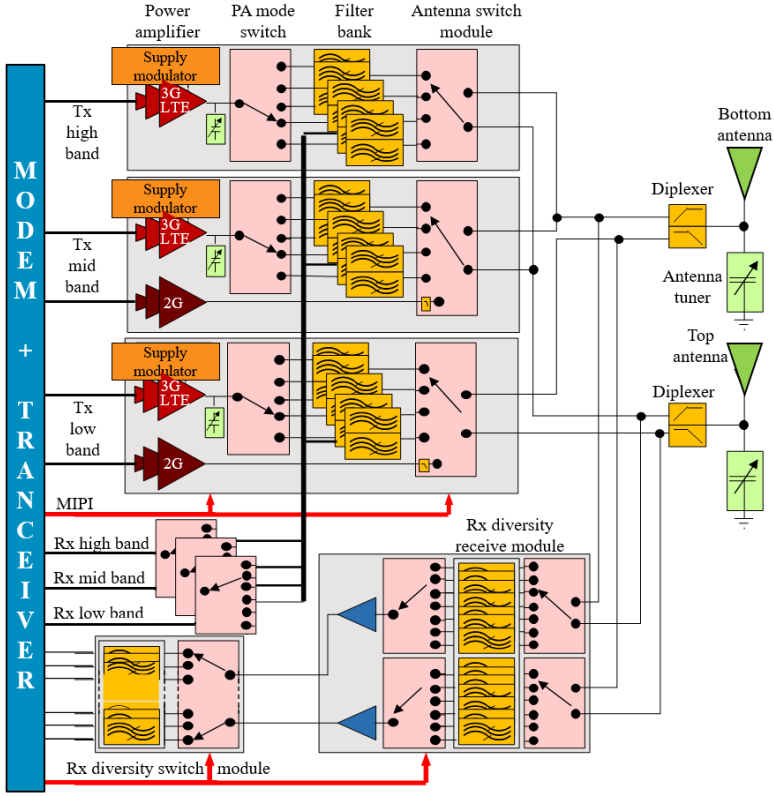
Indeed, stacked RF-SOI FETs on a high-resistivity substrate provides high-quality RF switching modules that have steadily displaced Gallium-Arsenide (GaAs) and other technologies. Today, RF-SOI technology is the mainstream switch option, and can be found in virtually all modern-day smartphones in the switching circuits placed in the signal path to and from the antenna **[8, 32]**.

With the increasing complexity of telecommunication front-end modules (FEMs), and production volumes on the rise for 5G and IoT applications, significant research and development efforts have been made to implement further key RF functions in SOI technology (beyond RF switches), motivated by the impressive RF performance of advanced SOI devices.

Figure 1.6 illustrates the increased complexity in an FEM between the 3G era (2004) and the 4G LTE-Advanced era (2014).



(a) 3G FEM.



(b) 4G LTE-Advanced FEM.

Figure 1.6: Example of front-end module block diagrams. **(a)** for 3G, and **(b)** for 4G LTE-advanced. Courtesy of Soitec.

The advent of more advanced standards requires a higher number of frequency bands to achieve the needed data throughput. In standard communications a single frequency band in the GHz range, which may be up to 20 MHz wide, allows for up to 150 Mbps of downlink throughput. This data rate can be pushed up to the order of 1 Gbps by combining several of these bands into a single data channel. This scheme, called carrier aggregation (CA), is already used in the most advanced 4G LTE standard (FEM diagram represented in **Figure 1.6 (b)**), and will continue to be a technique for the upcoming 5G standard. Since the bands are very close in the frequency domain, CA poses several challenges with regards to band isolation. An increased number of bands necessitates an increased number of filters and switches, and aggregation of spectra with close frequencies imposes higher performance requirements from RF components, especially in term of isolation and linearity, both of which are sources of spectral cross-contamination between bands.

As a consequence, tougher linearity specifications are required for the most advanced network standards **[33–35]**, and they are summarized in **Table 1.1**.

Network	Linearity IIP3 [dBm]
2G	55
3G	65
4G LTE	72
4G LTE + CA	Up to 90

Table 1.1: Linearity Requirements by Network Standard **[33, 34]**.

At the circuit level, these requirements translate into increased complexity in the architecture of the smartphone's FEM, as depicted by the block diagrams in **Figure 1.6**. Support for multiple bands in a mobile device requires a complex array of filters and switches with high throw counts to route signals to and from the antenna to the main RF transceiver. Within this array of filters and switches, careful consideration must be given to path loss, isolation, stopband rejection and linearity to ensure the fidelity of the signal being processed **[30]**.

1.2.2 RF Front-End Modules: Future Trends

The FEM complexity increase that comes with higher data-rate communication standards leads to a higher amount of RF content in smartphone devices. This is highlighted in **Figure 1.7** that presents the evolution of the smartphone's RF content and value throughout the network standard generations **[36]**.

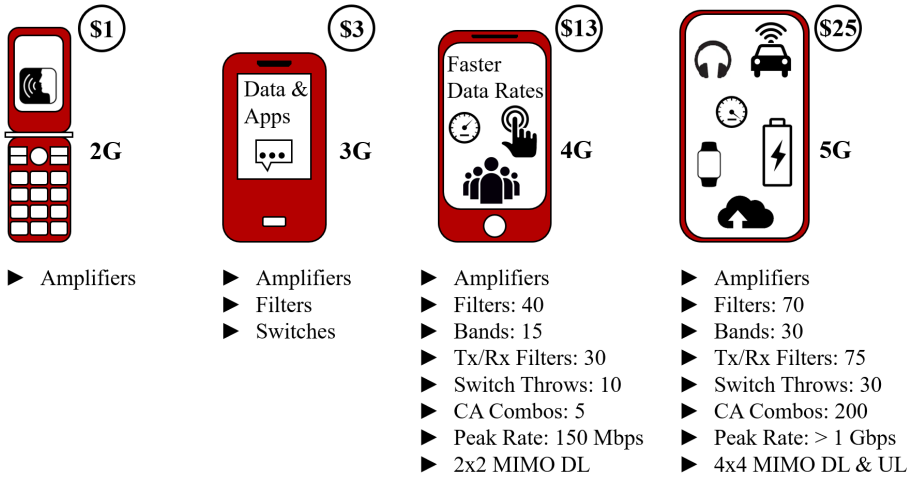


Figure 1.7: Evolution of RF content in smartphones over the generations of communication network standards. Source: **[36]**.

The RF content in a single phone has grown from approximately $1 for 2G cellular handsets, to $3 for the first generation of 3G enabled smartphones, up to $13 for the next 4G generation, and reaching $25 of RF content today in the most advanced 4G-LTE-advanced devices of 2020 **[36]**. The growth in the RF content, and hence in the RF industry, is directly related to the evolution of the FEM's complexity (**Figure 1.6**).

To support it, the RF industry requires a technology with high-volume manufacturing capability **[37]**, for each element of the FEM.

SOI technology fits the bill, and this need has prompted the development of a wide range of high frequency SOI circuit modules, motivated by the impressive RF characteristics of advanced SOI FETs, and by the enablement of 300 mm SOI wafers. Tremendous research effort has been dedicated to RF-SOI, driven by large volume applications requiring inexpensive single-chip transceivers (switches, LNAs, PAs, etc.), including both at the base-band and

the RF front ends. To highlight this, **Figure 1.8** presents a historical literature review of SOI technologies for RF and mm-wave applications.

As previously discussed, integrated switches were the first SOI modules for RF applications, hitting the market around 2007 and dominating it for handsets by 2012. Today (2020), most RF switches found in smartphones in consumer hands are implemented in the 180 nm and 130 nm nodes on *specially engineered RF substrates*.

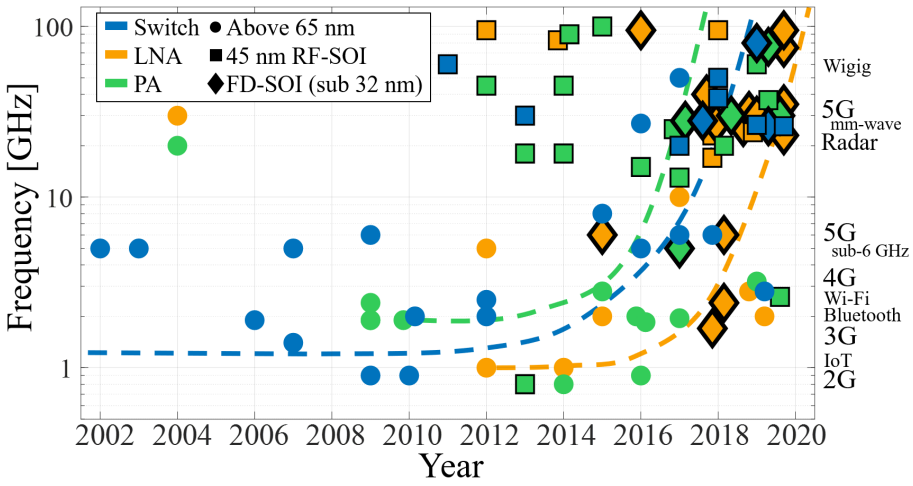


Figure 1.8: Literature review over time of SOI technologies for RF and millimeter wave circuit elements of FEMs.

Significant research interest and industry development pushed the RF SOI nodes even further, down to the 45 nm PD-SOI node, truly optimized for RF performance, and beyond, to sub-30 nm FD-SOI nodes[1].

With these performances other key RF circuit elements emerged in the literature, starting from around 2010-2012 for low-noise amplifiers (LNA) and power amplifiers (PA).

[1] As shown in the previous section, these advanced PD-SOI and FD-SOI technologies boast cutoff and oscillation frequencies in the range of 400 GHz.

The partially depleted 45 nm RF-SOI process from GlobalFoundries **[38, 39]** has demonstrated its strong potential for RF and mm-wave circuits. **Figure 1.8** shows the emergence of this technology around 2012, implementing RF functions such as VCOs, LNAs, PAs and switches at millimeter wave frequencies up to 100 GHz, and this process is commercially available to the industry as of late 2017. Integrated on low-loss and highly linear *trap-rich substrates* from Soitec, this process is truly optimized for RF purposes allowing high-quality interconnects, transmission lines and passives (inductors, transformers, etc.) along with strong substrate isolation and linearity. These RF substrate metrics will be discussed in detail in the next section of this chapter.

Around 2015, IC demonstrator circuits in 22 nm and 28 nm UTBB FD-SOI processes (from GlobalFoundries and STMicroelectronics or Samsung, respectively) were developed, and interest in these technologies for high frequency applications has increased significantly since then **[40]**. In particular, **Figure 1.8** clearly reveals a focus at 28 GHz in the recent FD-SOI research literature.

While 45 nm RF-SOI has a strong application focus at the millimeter wave (above approximately 20 GHz) bands (due to its high speed and optimized substrate and process), FD-SOI nodes also find applications at lower frequencies (sub 6 GHz) where their RF performances can be tuned down to remain sufficient for IoT type RF applications but at ultra-low power consumption.

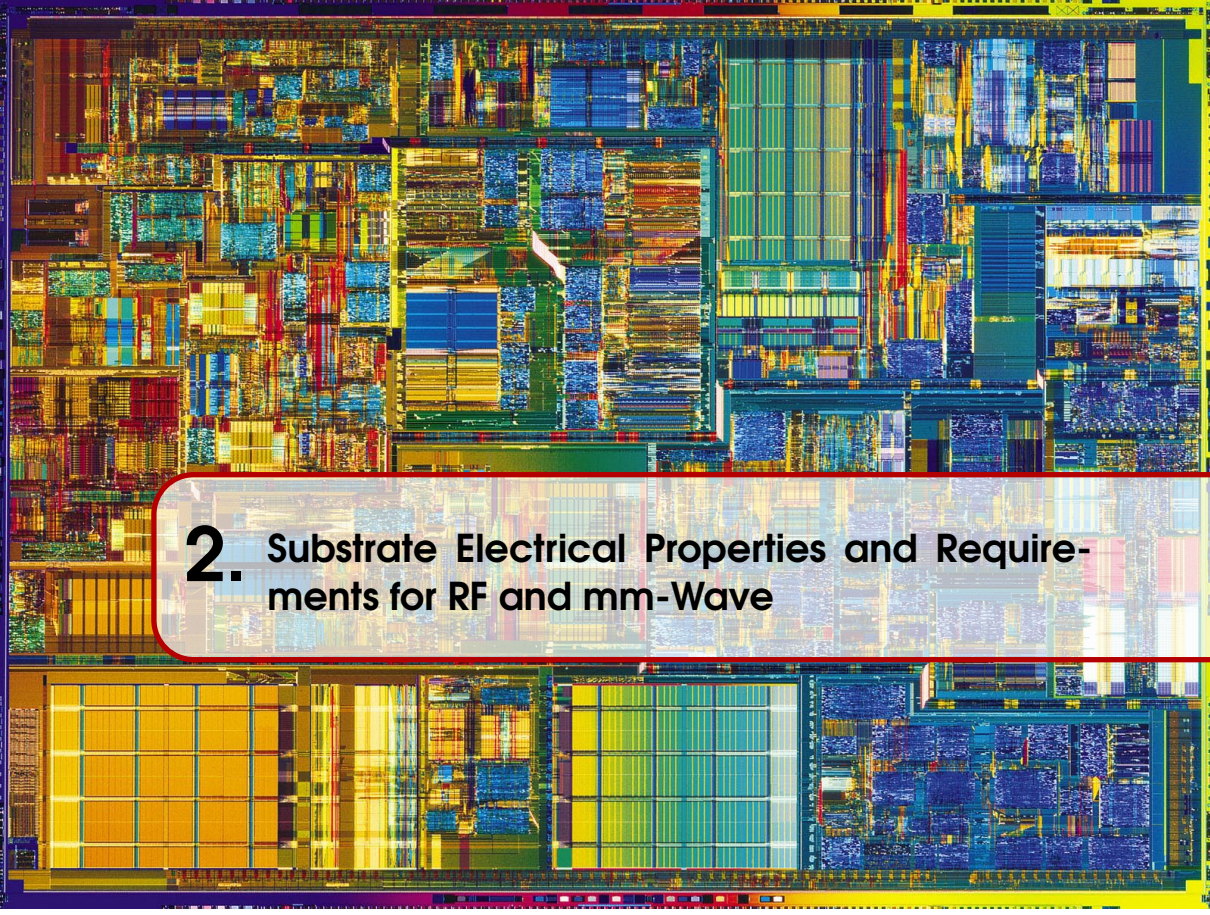
1.3 Chapter Summary

The high-volume production capabilities offered by the silicon industry has motivated the development of RF- PD-SOI and FD-SOI nodes, that are now demonstrating their potential for all kinds of RF and millimeter wave functional blocks towards full SOI front-end module integration.

The success of SOI as an RF platform is due to significant technological improvements made at both the transistor level as well as at the level of the substrate. Today (2020), the 130 nm and 180 nm PD-SOI nodes on optimized RF substrates dominate the RF switch market in handheld smartphone devices.

The more advanced PD-SOI nodes (sub-100 nm) as well as the most advanced FD-SOI nodes (sub-30 nm) are demonstrating their potential for all kinds of functional blocks beyond RF switches (LNAs, PAs, VCOs, etc.) towards full SOI front-end module integration. High speed performance metrics --f_t and f_{max} in the 400 GHz range— are enabled by continuous gate downscaling and SOI's low parasitic architecture, making SOI a promising technology for 5G and mm-wave applications, while at the same time providing advanced digital processing capabilities on the same technological platform. Furthermore, FD-SOI's ultra-low power capabilities are of significant interest toward RF-IoT types of applications.

As a result, significant industrial research and development is being performed toward fully integrated SOI front-end-modules. Notably, the 45 nm PD-SOI and 28 nm and 22 nm FD-SOI nodes are being extensively designed with to develop 5G mm-wave low-noise amplifiers (LNA), power amplifiers (PA) and switches, in particular at 28 GHz and 39 GHz.



2. Substrate Electrical Properties and Requirements for RF and mm-Wave

The electrical properties of the physical substrate have a strong impact on device and circuit performance, and this is especially true at RF and mm-wave frequencies. At high-frequencies the thin dielectric layers isolating the metal interconnects, passives, and transistors[1] from the substrate become transparent by their capacitive nature, and significant electric fields from these devices penetrate into the silicon substrate, inducing losses and strongly impacting the values of parasitic coupling elements.

Today's success of PD-SOI technology is due to significant technological improvements made at both the transistor level as well as at the level of the substrate **[41]**.

Indeed, the so-called *trap-rich* substrates, invented at UCLouvain in the early 2000's **[42, 43]** and developed by Soitec **[44, 45]**, are engineered and optimized for high electromagnetic performance for RF applications **[31, 46]**. Integrating multiple functionalities (such as multiple RF functions as well as digital) on a single chip is a main driving force behind the progress of ICs, and today the high-quality trap-rich SOI substrates are used in front-end switching

[1] At least in the case of SOI.

modules of virtually all modern-day smartphones in consumer hands (2020).

It is worth noting however that FD-SOI, a technology that is showing high device-level performance for mm-wave applications, is still only supported on standard-resistivity wafers that are lossy, non-linear, and facilitate substrate noise propagation. This is due to intrinsic incompatibilities between the trap-rich substrates and below-BOX features of FD-SOI platforms, such as diodes to the substrate (of which electrostatic-discharge (ESD) protection devices), back-gate well definitions, and bipolar junction devices, to name a few.

A thick back-end of line can partly make up for the substrate's influence by using the lower metal layers to shield the interconnects and passive devices from the substrate parasitic effects. This gives rise to lines and passives of acceptable quality (though usually high capacitance), but some designs remain a challenge under these constraints, notably spiral inductors, transformers and transmission-lines **[47]**.

Without careful substrate considerations, losses, coupling and linearity issues of key RF blocks can easily be dominated by the substrate's properties **[48, 49]**, and we shall see how the industry has adapted to overcome and mitigate such issues.

In this chapter, we overview the substrate impact on RF-ICs, and present the principle types of SOI substrates found in today's foundry options.

To evaluate the substrate's small-signal performance, the concept of *effective resistivity* is employed, which serves as a metric that can be related to interconnect losses, passive quality factors and substrate noise coupling. Throughout the rest of this thesis, the effective resistivity will be considered as a figure of merit (FoM) of RF substrates, and in this chapter a section is dedicated to its mathematical definitions and its extraction procedure from measured (or simulated) *coplanar waveguide (CPW)* devices.

Measurements of integrated CPW lines, spiral inductors, antennas, mm-wave filters and crosstalk devices are presented in this chapter on the most common types of SOI substrates.

A small-signal simulation methodology combining an electromagnetic field-solver tool and a TCAD semiconductor solver tool is presented and is applied to accurately model all aforementioned passive devices with good correlation to their measurements on all considered substrates.

Finally, the concept of substrate-induced signal distortion due to substrate non-linearity is introduced, and its importance is discussed in the context of front-end module circuitry.

2.1 Substrate Impact on Coplanar Technology

2.1.1 From Standard Silicon to High-Resistivity and Trap-Rich SOI

In RF integrated circuits (ICs) signals propagate in a conductive metal layer atop an insulator-semiconductor stack. A coplanar waveguide (CPW) is depicted in **Figure 2.1** above such a stack of materials.

Ideally, a transmission line or waveguide would have a unity transmission coefficient, with 100% of the input power reaching the output. However, materials always have some degree of loss associated to them. Due to a finite metal conductivity, the propagation of the signal through the metal lines leads to energy dissipations within the metals. Another source of loss is due to a finite substrate resistivity, as RF fields penetrating into these materials induce RF currents within them. In lossy materials, be it metals or semiconductors, part of the signal's power is dissipated within by Joule effect, and only a portion of the power is retrieved at the output.

To avoid losses in such lines, and also to mitigate coupling between them, it is important for the underlying substrate to have a high *effective resistivity*.

Furthermore, the substrate should be as linear as possible to minimize distortion of the electrical signals. The standard-doped (10-20 Ωcm) silicon substrate –widespread among digital applications– is therefore unsuited to wireless systems, RF devices and power circuits due to its high conductivity, high RF losses and low linearity. Low-doped silicon is then favoured with high *nominal resistivity* (ρ_{nom}) above 1 kΩcm **[50]**. However, the *effective resistivity* (ρ_{eff}), i.e. which is sensed by the overlying planar circuits, can differ strongly from the nominal resistivity ρ_{nom} due to band bending effects at the semiconductor/insulator interface that severely reduce the local resistivity, greatly impacting the overall sensed ρ_{eff}. The resistivity of semiconductors is by nature dependent on the local electric field (and we call this the *field-effect*). Low-doped high-resistivity (HR) substrates are particularly field-sensitive, and it is typical for the semiconductor volume beneath the insulator to be in a conductive state due to (even low-level) parasitic fields present in the multilayer. The most common parasitic fields originate from fixed charges (positive in Si/SiO_2 heterostructures **[51–59]**) that are present at the insulator/semiconductor interface. Then, a highly conductive channel-like layer is induced beneath the insulator, as depicted in **Figure 2.1**. These fixed charges (represented by "+" symbols in **Figure 2.1**), are inevitable in the IC fabrication process, and induce free electrons at the interface in very high concentrations, locally lowering the resistivity beneath the circuits by a factor of 10^3 to 10^6. This in turn lowers

the sensed effective resistivity by a factor of 10 to 10^4, to values as low as 1 Ωcm. This is referred to as the parasitic surface conduction (PSC) effect that renders the use of a HR substrate ineffective for improving the performance of overlying RF-ICs as compared to standard-doped silicon ($\rho_{nom} \approx 10$ Ωcm) [60].

A breakthrough in this area was made in the early 2000's with the introduction of a thin polysilicon layer rich in defects (traps) beneath the buried oxide in SOI technology [42]. This layer effectively mitigates the PSC effect by pinning the Fermi level near mid-gap at the interface in a highly resistive state, enabling ρ_{eff} values of over 1 kΩcm. Physical details of these mechanisms will be given in the next chapter (in Section 3.2).

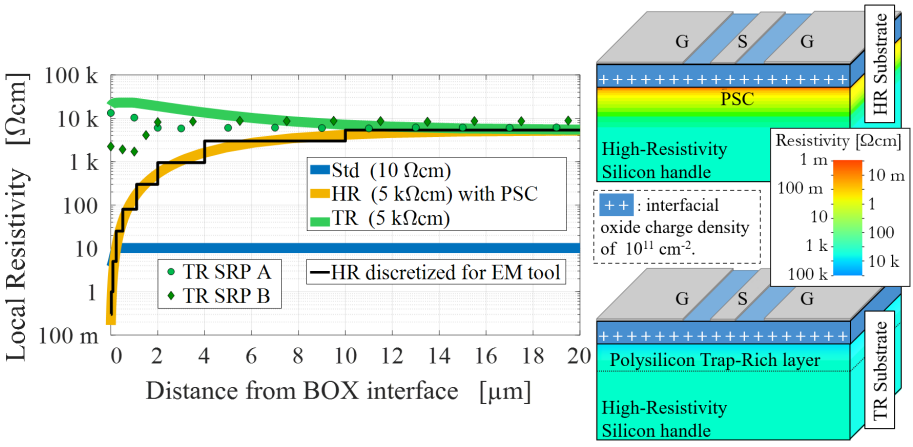


Figure 2.1: Resistivity profiles in the semiconductor volume beneath the BOX layer for an N-type standard-resistivity substrate (10 Ωcm), an N-type high-resistivity substrate (5 kΩcm), and a trap-rich substrate (5 kΩcm bulk + 2 µm-thick polysilicon rich in traps at BOX interface). All profiles include the presence of interfacial oxide charges with a density of $1 \cdot 10^{11}$ cm^{-2}.

High-resistivity wafers suffering from the PSC effect have resistivity profiles from the BOX interface that are highly non-uniform, as depicted by the orange curve of Figure 2.1.

Though trap-rich SOI overcomes the PSC effect by introducing a thin (up to 3 μm) polysilicon layer below the BOX, the resulting resistivity profile in such substrates cannot be said to be uniform. Indeed, the local resistivity in the polysilicon layer may be higher or lower than in the bulk of the Si handle

substrate, depending on the exact process parameters of the trap-rich wafer. One example is partial recrystallization of the polysilicon layer due to the thermal budget of the foundry process that may cause a significant decrease in the total number of trapping centers. Another example is impurity contamination of the polysilicon layer that diffuses much faster in the polysilicon along grain boundaries than in the bulk crystalline silicon. Both of these situations arise in practice and have an effect on the local resistivity profiles in TR substrates[2]. Measured data, obtained from the spreading resistance profile (SRP) technique is also plotted in **Figure 2.1**, for two TR samples. Both samples illustrate the range of polysilicon resistivities that may arise in practice below the BOX of TR SOI[3,4]. The green curve in **Figure 2.1** represents the resistivity profile beneath the BOX in a high-quality TR-SOI substrate, while the blue curve illustrates the profile in a standard resistivity (10 Ωcm) substrate (Std).

The results of **Figure 2.1** were obtained using the finite element semiconductor simulation tool ATLAS from Silvaco **[61]** which solves for Poisson's and semiconductor equations in the Si-based substrates and at the Si/SiO_2 interfaces, allowing for physical parameters such as fixed oxide charges, interface and volume traps to be accurately simulated along with their impact on the free carrier distributions in the semiconductor regions. In all simulated substrates an interfacial oxide charge density of $1 \cdot 10^{11}$ cm^{-2} was defined. For the TR sample tail-type distributions for the acceptor and donor traps were used to model the polysilicon layers according to **[62]**. The details of these trap distributions, as well as the physical mechanisms by which their presence significantly increase both ρ_{eff} and linearity will be given in **Section 3.2**.

The TCAD simulations resulting in the curves of **Figure 2.1** considered N-type silicon bulks[5].

[2] In **Chapter 5**, we will present several industrial trap-rich SOI samples, with the aim of fitting the small- and large-signal models developed in this thesis to the measured sample's data. Some samples have undergone strong thermal anneal steps, and present lower trap density. Other samples have significant Boron contamination in the polysilicon layer, confirmed by measured SIMS data. Both of these phenomena must be taken into account for accurate modelling, as they can both impact (degrade) TR substrate RF performance, as will be discussed in **Sections 5.4 and 5.5**.

[3] The principle of the SRP measurement is detailed in **Appendix 7.2**.

[4] Please note that no SRP data was plotted for the HR and Std samples, as the SRP technique is not sensitive to oxide charge effects due to the large bevel angle. Therefore, SRP data of HR and Std samples are simply flat, at a value equal to that determined by the nominal doping.

[5] In the case of P-type substrates, a depletion region is present between the PSC layer and the silicon bulk, and the resistivity profile peaks strongly in that region.

Three reference SOI substrates, a standard-resistivity (Std), a high-resistivity (HR) and a trap-rich (TR) were fabricated with pertinent passive RF devices defined above the BOX in order to compare the RF measurements of the various devices to simulation data. Both the HR and TR samples were fabricated starting from high-resistivity float-zone wafers characterized by a nominal resistivity above 5 kΩcm, while a 10 Ωcm starting silicon wafer was used for the Std sample. A 500 nm polysilicon layer was deposited for the TR sample. Finally, a 500 nm oxide was deposited by PECVD for all three samples, followed by a 1 µm aluminium metallization and front-side lithography and etch to pattern the RF structures.

The first RF structure considered is a simple coplanar waveguide (CPW) transmission line. From RF measurements and/or simulations of these lines the effective substrate electrical parameters can easily be computed. Indeed, the RF engineer requires the knowledge of substrate permittivity and resistivity to perform accurate RF circuit designs. However, because the substrate is a heterostructure, made up of several materials, and because the semiconductor materials present non-uniform properties, it is not straightforward to estimate the impact of the substrate beneath a given device. For these reasons, the concept of effective resistivity and permittivity are employed.

2.1.2 Concept of Effective Resistivity and Permittivity

Referring to **Figure 2.2** the effective substrate parameters ρ_{eff} and ε_{eff} are defined as follows: they are the homogenized electrical parameters of an equivalent material such that the CPW line implemented on this equivalent material has exactly the same electrical behavior (i.e. the same S-parameters) as an identical CPW line implemented on the real non-uniform substrate. This equivalence is highlighted in **Figure 2.2**.

Extraction Procedure

The extraction procedure of ρ_{eff} and ε_{eff} of the substrate material stack below the CPW line is as follows.

It starts from the measured or simulated total lineic admittance data C_{data} and G_{data}. Such data can be simulated for directly using TCAD tools or can be converted from S-parameter results **[63]** (measured data or simulated results using EM tools). In that case, it is important to point out that the transformation of S-parameters into the lineic *RLGC* parameters is non-trivial for low-loss substrates at high frequencies. A new method was developed in **[64]** to enable

this conversion in such challenging conditions. In any case, C_{data} and G_{data} englobe contributions from the material substrate stack of interest, below the CPW line, but also contributions from materials above (and between) the CPW line. Referring to **Figure 2.2**, these contributing terms are expressed as:

$$C_{data} = C_{top} + C_{bot} \quad [\mathrm{F/m}] \quad \textbf{(2.1)}$$
$$G_{data} = G_{top} + G_{bot} \quad [\mathrm{S/m}] \quad \textbf{(2.2)}$$

To extract the effective resistivity, the substrate below the CPW line is equated to a uniform material, as depicted by **Figure 2.2**. We are interested in the electrical parameters of the substrate stack below the CPW line C_{bot} and G_{bot}. They can extracted from the data if the material parameters of the material above the CPW line are known[6]. To extract the effective electrical properties of the material stack below the line, the extraction procedure requires the knowledge material parameters above the line. We then write:

$$C_{bot} = C_{data} - C_{top} \quad [\mathrm{F/m}] \quad \textbf{(2.3)}$$
$$G_{bot} = G_{data} - G_{top} \quad [\mathrm{S/m}] \quad \textbf{(2.4)}$$

Knowing the dimensions of the CPW line, the impedance parameters C_{top}, G_{top}, C_{bot}, G_{bot}, can be related to the material parameters, in the case of uniform materials, using the closed form expressions from **[65]**:

$$C_{top} = \varepsilon_0 \varepsilon_{r,eff,top} \cdot F_{top}(DIMS) \quad [\mathrm{F/m}] \quad \textbf{(2.5)}$$
$$G_{top} = \frac{1}{\rho_{eff,top}} \cdot F_{top}(DIMS) \quad [\mathrm{S/m}] \quad \textbf{(2.6)}$$
$$C_{bot} = \varepsilon_0 \varepsilon_{r,eff,bot} \cdot F_{bot}(DIMS) \quad [\mathrm{F/m}] \quad \textbf{(2.7)}$$
$$G_{bot} = \frac{1}{\rho_{eff,bot}} \cdot F_{bot}(DIMS) \quad [\mathrm{S/m}] \quad \textbf{(2.8)}$$

where F_{top} and F_{bot} are geometrical functions of the dimensions $DIMS$ of the

[6] This is generally the case. For most samples presented in this thesis, the above material is air, so $\varepsilon_{r,eff,top} = 1$ and $\sigma_{top} = 1/\rho_{top} = 0$. Some samples come from industrial processes, and BEOL dielectrics may be above the CPW line. But, in this case again, the material parameters are usually well known. A dedicated EM type of simulation can be run considering the known stack of above dielectrics to extract $\varepsilon_{r,eff,top}$. Note that the extraction of ρ_{eff} does not depend on $\varepsilon_{r,eff,top}$ (see **Equation 2.10**), though the extraction of $\varepsilon_{r,eff}$ does.

CPW line (conductor width, spacing and thickness)[7], calculated according to [65].

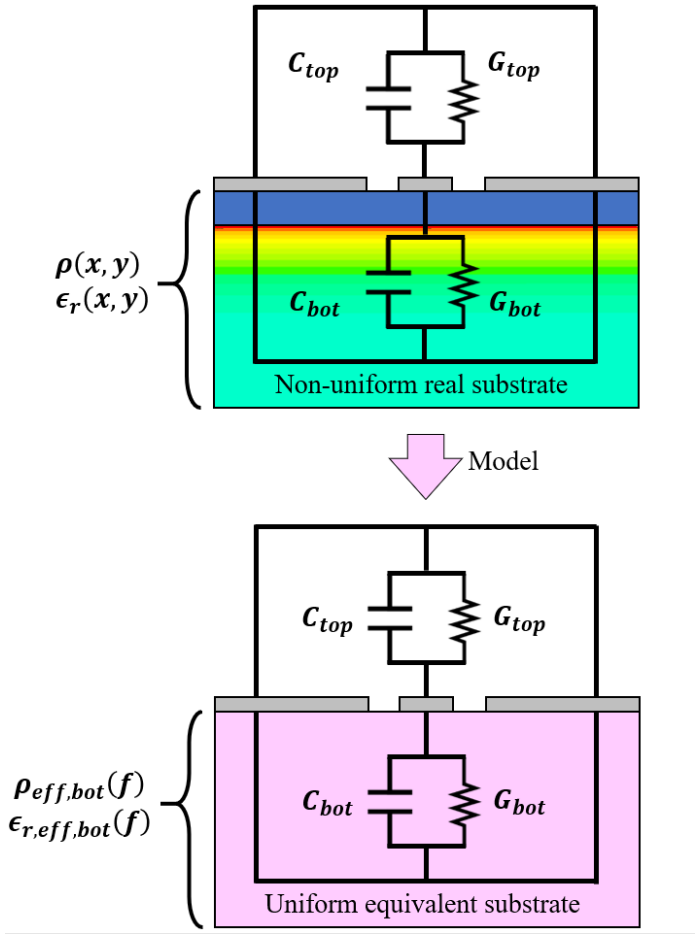


Figure 2.2: Concept and definition of effective resistivity ρ_{eff} and effective relative permittivity $\varepsilon_{r,eff}$.

[7] Analogous example: for a parallel plate capacitor, C is related to ε through the following well-known formula: $C = \varepsilon \cdot F(DIMS) = \varepsilon \cdot F(A,d) = \varepsilon \cdot A/d$, where A is the area of the parallel plates, and d is the separation between the two plates. In that case, the geometrical factor is $F = A/d$ (with fringing fields neglected).

we finally write:

$$\varepsilon_{r,eff,bot} = \frac{C_{data} - \varepsilon_0 \varepsilon_{r,eff,top} \cdot F_{top}(DIMS)}{\varepsilon_0 \cdot F_{bot}(DIMS)} \quad [\mathrm{F/m}] \quad \textbf{(2.9)}$$

$$\rho_{eff,bot} = \frac{F_{bot}(DIMS)}{G_{data} - \sigma_{eff,top} \cdot F_{top}(DIMS)} \quad [\Omega\mathrm{m}] \quad \textbf{(2.10)}$$

These equations are equivalent to the original formulation from **[66]**[8], and require the knowledge of the electrical parameters of the top material, along with the CPW line geometry.

With reference to **Figure 2.2** it should be noted that the effective resistivity $\rho_{eff,bot}(f)$ and permittivity $\varepsilon_{r,eff,bot}(f)$ of the equivalent uniform substrate are in general frequency dependent, while the local material parameters $\rho(x,y)$ and $\varepsilon(x,y)$ at each point in the real non-uniform substrate can usually be considered as frequency-independent (at least in the sub-6 GHz range, though at high-end mm-wave frequencies dependencies are expected in material dielectric behavior).

Measurement Data

To compare substrate performance and extract the equivalent electrical substrate parameters, CPW lines are measured and simulated on the three considered SOI wafers. Both the measurements and the simulations yield the S-parameters of the CPW line, and these are converted into the line *RLGC* parameters, and then subsequently into the substrate's effective resistivity and permittivity as described in above.

The RF measurements were performed on-wafer using a high-frequency vector network analyzer (VNA) and a pair of ground-signal-ground (GSG) microwave probes. This is the case for all on-wafer measurements presented throughout this chapter, and for more information on the measurement techniques, calibration and de-embedding, the interested reader is invited to find details in **[64, 66–71]**.

The substrate and line parameters obtained from the extractions of S-parameter measurements on the three types of SOI substrates are shown in solid lines in **Figure 2.3**.

[8] In that work, parameter C_0 and q (filling factor) are used together instead of F_{top} and F_{bot}. They are linked in the following way: $C_0 = \varepsilon_0 \cdot F_{bot}$, $q = F_{bot}/(F_{bot} + F_{top})$. Furthermore, in the original paper, $\varepsilon_{r,eff,top}$ was assumed to be equal to unity and $\sigma_{eff,top}$ was assumed to be zero.

The CPW lines on standard (Std) resistivity SOI substrates present an effective resistivity in the range of 10 Ωcm. As a consequence, the lineic RF losses of the lines on Std substrates are in the range of 3.0 dB/mm at 10 GHz.

The effective resistivity and RF losses of the CPW lines on a high-resistivity (HR) substrate are of similarly poor performance as the Std substrate's. The extracted value of around 30 Ωcm for the HR substrate is due to the PSC effect induced by fixed charges in the BOX **[60, 66]**. The high nominal resistivity of the HR substrate is counteracted by a thin, high carrier density, highly conductive region formed at the Si/SiO_2 interface (see **Figure 2.1**). The interfacial fixed oxide charge density is positive and usually in the range of $2 \cdot 10^{10}$ to $1 \cdot 10^{12}$ units of elementary charge per cm^2. This value depends on the nature of the oxide, and on the process parameters leading to the Si/SiO_2 heterostructure. The induced free electron density at the interface is then in the range of $1 \cdot 10^{15}$ to $2 \cdot 10^{18}$ per cm^2, which translates into a local resistivity at the surface of approximately 5 Ωcm to 25 mΩcm. Consequently, effective resistivities sensed by coplanar circuits in HR substrates vary from a few hundred Ωcm to less than 10 Ωcm. In the sample presented here, a fixed oxide charge density of around $3 \cdot 10^{11}$ cm^{-2} is present at the interface[9], which induces an electron surface density of around $2.5 \cdot 10^{17}$ cm^{-3}. This corresponds to a local resistivity at the surface of approximately 90 mΩcm, and as a consequence the effective resistivity is around 30 Ωcm. The lineic RF losses of the CPWs on the HR sample are therefore in the range of 1.4 dB/mm at 10 GHz, as can be seen from **Figure 2.3**.

Trap-rich (TR) substrates eliminate the PSC effect with the addition of a thin polysilicon layer, rich in defects, beneath the BOX and above a high nominal resistivity silicon bulk **[42, 72]**. These defects, or traps, capture the large number of induced carriers present in the PSC layer and effectively pin the Fermi level near mid-gap at the BOX interface, ensuring a state of strong depletion and high resistivity[10]. The extraction of the effective parameters from the CPW line measurements show a substantial increase of the effective resistivity to values of the order of 6.5 kΩcm[11], and as a consequence the RF line losses at 10 GHz are at the low value of 0.24 dB/mm. Practically all of these losses are due to resistive losses inside the metal lines themselves, and

[9] Extracted from measured CV data of a MOS capacitor.

[10] Details on the physics of trapping mechanisms are given in **Chapter 3**, **Section 3.2**

[11] Representative and approximate value, as the measured TR data is quite noisy, which is typical of low-loss substrates (measured *G* parameter of the line is very low).

not to dissipation within the substrate.

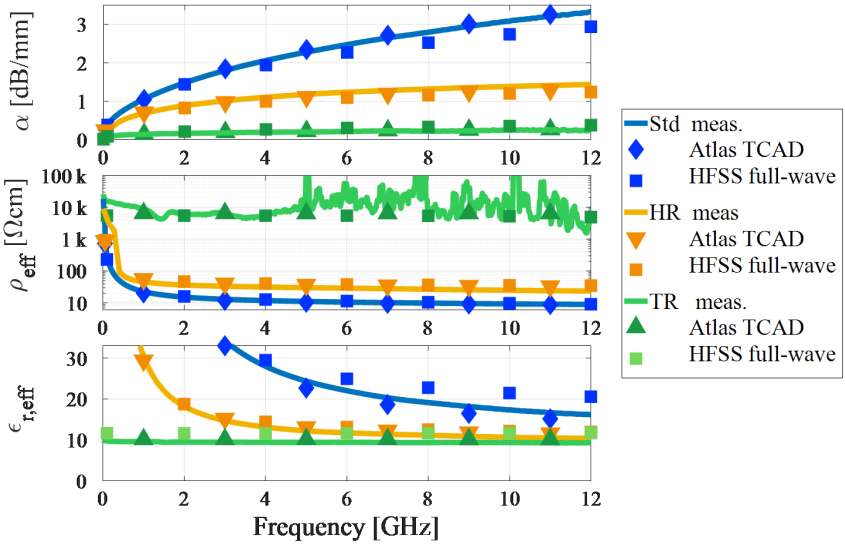


Figure 2.3: Effective electrical substrate parameters extracted from CPW-lines S-parameters obtained by (i) on-wafer measurements, (ii) Atlas TCAD simulations and (iii) HFSS full-wave simulations.

In all cases the extracted effective resistivity and effective relative permittivity are frequency-independent at high enough frequencies. At low frequencies, the propagation is the *slow-wave* mode due to the presence of an insulator layer, and the fields are then mainly concentrated within this insulator material and the silicon under-layer acts basically as an equipotential node. The substrate admittance is then almost purely capacitive, with a negligibly small real part, and hence very high ρ_{eff}. The ε_{eff} becomes very high at low frequency, as the insulator layer is usually thin.

Throughout this work, we shall usually (unless explicitly stated otherwise) seek to extract the effective substrate parameters at sufficiently high frequency (above slow-wave mode) such that they are frequency independent.

The transition frequency out of the slow-wave mode depends on the isolating dielectric parameters as well as on the effective resistivity of the substrate, and this transition occurs at higher frequencies for lower resistivity substrates. For this reason, the effective parameters of highly resistive substrates such as trap-

rich can be extracted starting from a few tens of MHz. However, the mode of propagation in the CPW lines on the highly conductive substrates, HR and Std, only transits out of the slow-wave mode at 5 or 10 GHz, and the effective electrical parameters of the substrate will usually be extracted above these frequencies in this text.

2.1.3 Small-Signal Substrate Modelling

Superimposed upon the measurement curves of **Figure 2.3** are plotted the small-signal effective parameters extracted from simulations of CPW lines using two methods:

1. Closed-form *RLGC* CPW transmission line modeling with substrate terms (*G* and *C*) provided by Technology Computer Aided Design (TCAD) -based method (using Atlas from Silvaco).
2. Full-wave electromagnetic solver with the local resistivity profiles provided by TCAD (Atlas from Silvaco).

The first method is based entirely on Atlas TCAD software that solves semiconductor transport equations. They are solved for using Finite Element Methods (FEM) in the case of the three substrates to obtain the 2D (or even 3D, if required) resistivity profile at all points in the substrates, taking into account oxide charges, traps, and other material and interface parameters. This type of TCAD solver does not however solve for electromagnetic propagation, i.e. does not solve Maxwell's equations. To model a CPW line, a 2D TCAD simulation is employed to obtain the lineic capacitance *C* and conductance *G* between the signal electrode of the CPW line and the two ground electrodes (see **Figure 2.2**). Then, the lineic resistance *R* and lineic inductance *L* of the CPW line can be obtained from accurate close-forms analytical expressions given in **[65]**. These *R* and *L* parameters depend on the metal's thickness, width and material properties, but are independent of the substrate parameters[12]. Two port S-parameters of the CPW line can be reconstructed straightforwardly from these *RLGC* elements.

[12] Strictly speaking, *L* depends on the effective permeability of the material stack. In this thesis, all substrate and BEOL material layers considered have a relative permeability of 1, and for this reason, *L* only depends on the metal parameters in this work. Furthermore, mutual inductive coupling and eddy currents are neglected, which is a reasonable assumption for modelling substrates with effective resistivities above 1 Ωcm. In fact, lumped models of integrated inductors only include mutual inductive coupling to substrates that are highly conductive (such as epitaxial-silicon), and such elements are not necessary in inductor models on substrates of standard resistivity or above **[73–79]**.

This method of simulation gives insight into the substrate material's physical behavior. The independent contributions of fundamental material parameters on the RF quality of the substrate can be studied and evaluated, such as nominal doping, quantity and polarity of interface charges, quantity and energy position of trapping centers, etc. The resistivity profiles obtained from these simulations have already been presented in **Figure 2.1**, and the small-signal simulation results (triangular symbols) show good fitting to the measured data for all three substrates, as shown in **Figure 2.3**.

This method is based on a TCAD simulation in 2D and therefore is quite fast. Nevertheless, such a 2D approach can only be used for structures that are uniform in the third dimension, such as CPW lines, and for which accurate closed form modelling expressions exist **[65]**. However, more complex structures such as inductors, baluns, couplers, antennas and many others cannot be simulated by such an approach, especially since TCAD tools do not solve Maxwell's equations of electromagnetic (EM) propagation.

For these reasons, RF engineers rely on EM tools to design their RF circuit layouts. Software such as Momentum ADS from Keysight, HFSS from Ansys, CST Studio Suite or Sonnet are indispensable tools for RF design[13], and are usually based on either a full-wave Finite Element Method (FEM), or on the Method of Moments (MoM), which is a Boundary Element Method (BEM) **[81]**.

These reasons motivate the second simulation method, which combines an EM field solver with a TCAD solver. The circle symbols in **Figure 2.3** plot the modelling using this approach based on the HFSS tool. The EM tool does not solve for semiconductor transport equations, and cannot have as input the fundamental material parameters such as interface charge, trapping centers, etc., and as a consequence band bending effects and space charge distributions in semiconductor volumes are not solved for. The input parameters of each material block of the simulation set-up are basically its local resistivity, permittivity and permeability. Therefore, to set-up the material stack in such simulations, the non-uniform resistivity profiles provided by TCAD are discretized into a finite number of uniform layers. The resistivity profiles presented in **Figure 2.1** are reprinted here below in **Figure 2.4**, and the highly non-uniform profile

[13] It is pertinent to point out that Momentum from Keysight is available as a plugin to the Cadence Virtuoso software that is the IC design platform for most foundries. Over 200 commercial Process Design Kits (PDK) from foundries support an extension to Momentum for RFIC design enablement **[80]**.

associated to the HR substrate (orange curve) is discretized into a series of 9 uniform silicon materials of different resistivities (black curve). By stacking these 9 material layers, the HR substrate's non-uniformity and therefore its real electrical behavior are approximated. **Figure 2.4** shows the material stack used to simulate the CPW lines on a HR substrate, whose results are plotted as the orange square symbols in **Figure 2.3**. Similar approaches where used to set-up the material stack and simulate the Std and TR substrates. **Figure 2.3** shows that good fitting is achieved between the EM simulations (square symbols) and the measured data (solid lines) and the TCAD simulations (triangular symbols).

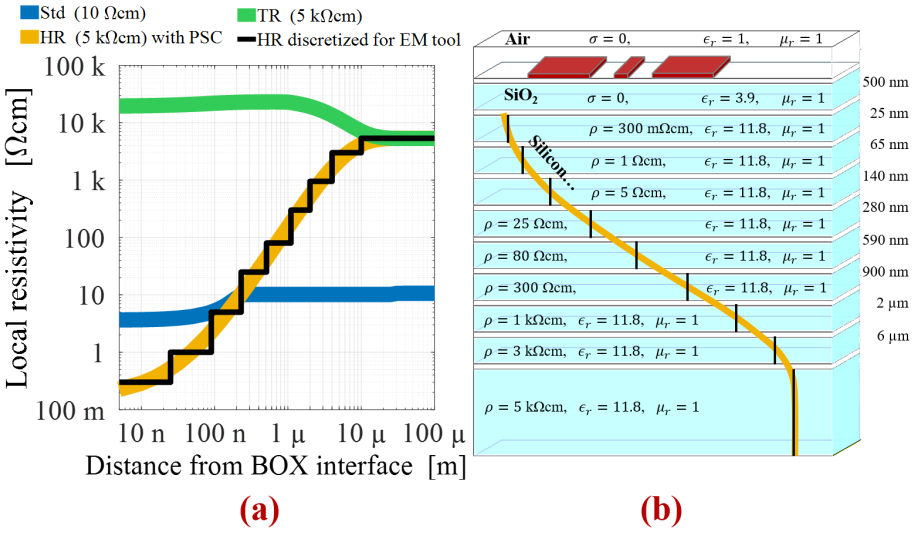


Figure 2.4: (a) Resistivity profiles in the semiconductor volume beneath the BOX layer for the three considered SOI substrates. An example of profile discretization is shown for the case of the HR substrate. **(b)** Example of material stack definition for EM solver tools to capture the non-uniformity of an N-type HR substrate suffering from the PSC effect.

Calibration of the Non-Uniform Material Stack

This methodology is powerful as the EM tool is fed by the TCAD simulator to provide an accurate description of the substrate.

It is then relevant to consider how to extract the resistivity profile $\rho(y)$ of an RF substrate sample from electrical measurements.

In general, the effective resistivity and permittivity depend on the layout and dimensions of the device under consideration. For example, a 50 Ω CPW line characterized by a spacing of 5 microns does not sense the same effective resistivity as one with a spacing of 50 microns, due to the different distribution of the electrical fields in the non-uniform substrate. This is schematically represented in **Figure 2.5**, that illustrates the CPW's electric field distribution in a substrate that is characterized by inhomogeneous properties below the oxide layer, presented as a bilayered model in which *Layer X* and *Layer Y* possess significantly different resistivities ρ_X and ρ_Y. Through a simplified analysis, we can say that wide CPW lines (relative to the thickness of *Layer X*) will have a larger proportion of their E-field in *Layer Y*, than the narrow CPWs. Therefore, the effective resistivity sensed by wide lines will be closer to ρ_Y, while that of narrow CPWs will be closer to ρ_X.

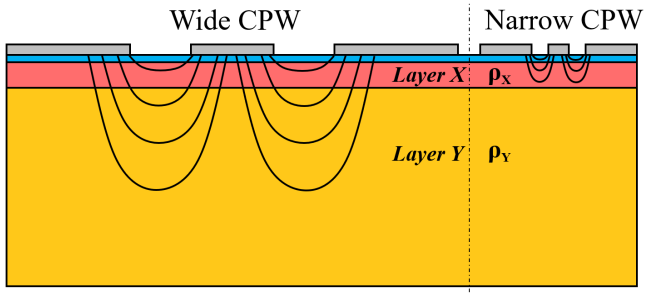


Figure 2.5: Schematical representation of the electric field line distributions in a given non-uniform substrate for two CPW lines of different dimensions.

Measurement results confirmed these effects. Several 50 Ω CPW lines were fabricated on four substrate samples: A TR-U and a HR-U sample from a university process, along with a TR-GF and a HR-GF from the GlobalFoundries 45 nm RF-SOI process **[82]**. The effective resistivity is extracted for all measured CPW lines on these four substrates. Several CPW line spacings S and central conductor widths W_c were designed to attain a 50 Ω characteristic impedance.

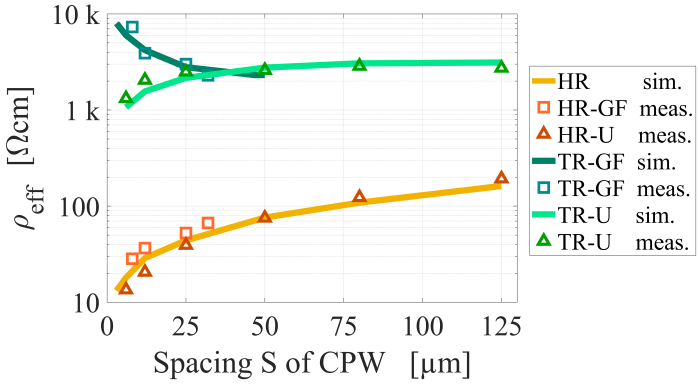


Figure 2.6: Measured and simulated effective resistivity values sensed by CPWs at 10 GHz on various substrates as a function of CPW line dimensions.

The W_c/S pairs that were fabricated are 10/6, 11/8, 26/12, 45/25, 70/32, 95/50, 150/80, 240/125, where all numbers are given in microns.

The results of measured and simulated effective resistivities are given in **Figure 2.6**, where ρ_{eff} extracted above slow-wave mode is plotted against the CPW spacing parameter S.

The simplified bilayered analysis (**Figure 2.5**) enables us to easily comprehend the trends obtained from the measurements and simulations performed on the non-uniform HR and TR samples. Substrates that present lower resistivity at the interface than deep in the bulk show higher effective resistivities for wider devices. This is illustrated by the HR-GF and HR-U samples, whose simulation ("HR sim." curve) employed the resistivity profile given in **Figure 2.4 (b)**. Sample TR-U has a similar trend, as its resistivity is also lower at the BOX interface than in the bulk (the used profile is not shown, but it is close to that of curve "TR SRP B" plotted in **Figure 2.1** on **pg. 30**). Conversely, substrates that present higher resistivity at the interface than deep in the bulk present the opposite trend. This is illustrated by the TR-GF sample, whose simulation employs the TR resistivity profile (green) given in **Figure 2.4 (a)**.

Measurements of CPW lines with various cross-section dimensions can then be leveraged to determine a resistivity profile $\rho(y)$ such that all CPW structures simulated on this determined substrate fit to the measured data. In general, independent CV measurements of MOS-capacitors enable a good estimation of the interfacial fixed oxide charge density. Then, using a TCAD tool we

can determine a fairly good first approximation of $\rho(y)$. Fine tuning can then be performed on the oxide charge density and/or the silicon mobility at the interface to achieve simulation fitting to all CPW dimension measurements. Furthermore, SRP data is very useful for determining the $\rho(y)$ in TR substrates.

The important point is that once an accurate stack of materials is set-up for a given substrate, such as the stack presented in **Figure 2.4** (**(b)** for a HR sample, any passive device or interconnect with any layout should be accurately simulated by the EM tool[14].

[14]To put it another way, if we had set-up the substrate in the EM tool to be a single silicon semiconductor region below the BOX defined by a resistivity of 30 Ωcm, the simulation of our CPW line of dimensions $W_C = 26\,\mu m$ and a $S = 12\,\mu m$ would have yielded S-parameters close to the measurement data, because the value of 30 Ωcm was indeed extracted from the measurements of this exact line (see $\rho_{eff}(S = 12)$ in **Figure 2.6**). However, when simulating a CPW line of different dimensions or even another RF passive with an entirely different topology and characteristic dimensions (inductor, coupler, balun, antenna, etc.), then the results would likely not fit well to the measured data. The accurate substrate definition, given in **Figure 2.4 (b)** for the case of a HR sample, overcomes this problem, and should really be considered as the best way to perform EM simulations during layout design.

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2.2 Quality of Integrated Passive Devices

In this section, the second simulation methodology combining an EM solver and a TCAD solver on calibrated substrates is put to use towards the modelling of a variety of passive RF structures, such as integrated inductors, coupled line filters, monopole antennas, and two-port crosstalk coupling structures.

2.2.1 Integrated Inductors

Inductors are critical components to RF systems, and are widely used in applications of impedance matching, RF filters, transformers, RF transceivers, voltage-controlled oscillators, power amplifiers and low noise amplifiers. They are also in general large devices (at least a few hundred microns in diameter) with respect to the BEOL dielectric stack (up to 10-15 µm for the most advanced industrial BEOL options of 2020) that isolates them from the underlying semiconductor substrate, and so at high frequencies their performances are strongly impacted by the electrical parameters of the substrate.

To evaluate the quality of inductors integrated on each SOI substrate, a 3.6 nH passive spiral inductor is implemented and measured on each of the wafers. The inductor's layout is shown in **Figure 2.7 (a)**). It has 3.75 turns with an outer diameter of 400 µm and is implemented using a 1 µm-thick aluminum layer. The trace width is 40 µm with a spacing of 10 µm between turns.

The measured S-parameters of the one-port inductors are converted into the inductor quality factor according to the following equation **[83]**:

$$Q = -\Im\{1/Y_{11}\}/\Re\{1/Y_{11}\} \tag{2.11}$$

Where Y_{11} is the measured scalar admittance parameter of the 1-port inductor device. The quality factor of the spiral inductor on the HR and TR substrates are plotted in **Figure 2.7 (b)**). The inductor presents a self-resonant frequency at approximately 10.5 GHz on both wafers (points when $Q = 0$).

The quality of the device on the TR sample is significantly higher than on the HR sample, due to significant substrate coupling (and losses) caused by the PSC effect that degrades HR's performances. Similar studies with similar conclusions were conducted in **[79, 84]** comparing integrated inductors on HR and TR samples.

EM modeling of the spiral inductors on the two types of substrates were also performed to compare with the measured data. The substrate stack definitions (profiles such as the one presented in **Figure 2.4 (b)**) for both the HR and

TR samples were tuned using RF measurements of various CPW lines of different geometries and based on TCAD simulations [82]. These substrate stacks (calibrated to fit for a wide range of CPW line measurements as described above) are then used in the EM tool to simulate the spiral inductors, and the results are superimposed on their measurements in **Figure 2.7**. Good agreement is achieved in terms of quality factor and also in terms of inductance value (3.6 nH, not shown), validating the substrate stacks and demonstrating in practice the validity of this approach.

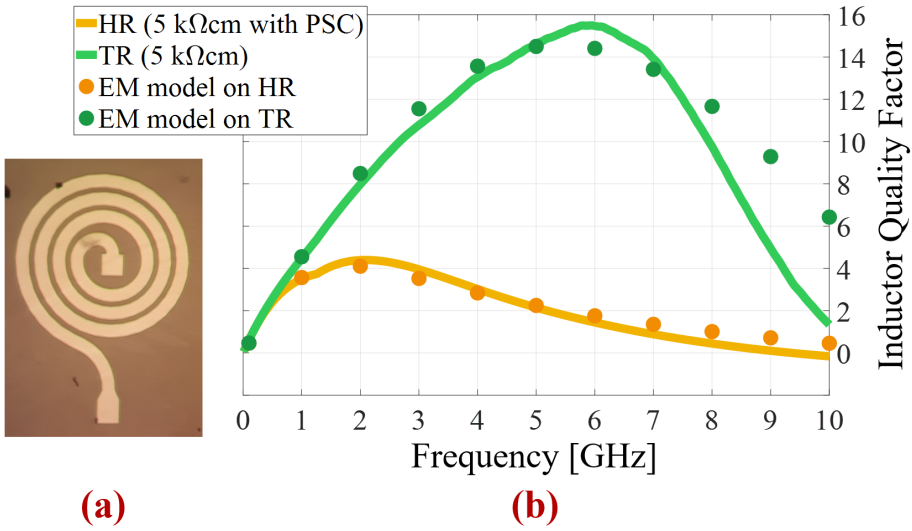


Figure 2.7: (a) Photograph of the measured spiral inductor implemented on the SOI substrates. The one-port devices were measured using a GS on-wafer probe with 375 µm pitch. **(b)** Comparison of the measured and simulated spiral inductor quality factor on the HR-SOI and TR-SOI samples.

2.2.2 Integrated mm-Wave Filters

Two types of millimeter wave passive bandpass filters in CPW topology [85, 86] were implemented on the same SOI wafers. Their layouts are given in Figure 2.8 (a) and (c), along with their respective S-parameter measurement and simulation results in (b) and (d). By using the same EM substrate definition as for the CPW lines and integrated spiral inductor, good simulation agreement is achieved once more for both millimeter wave filters on all substrates.

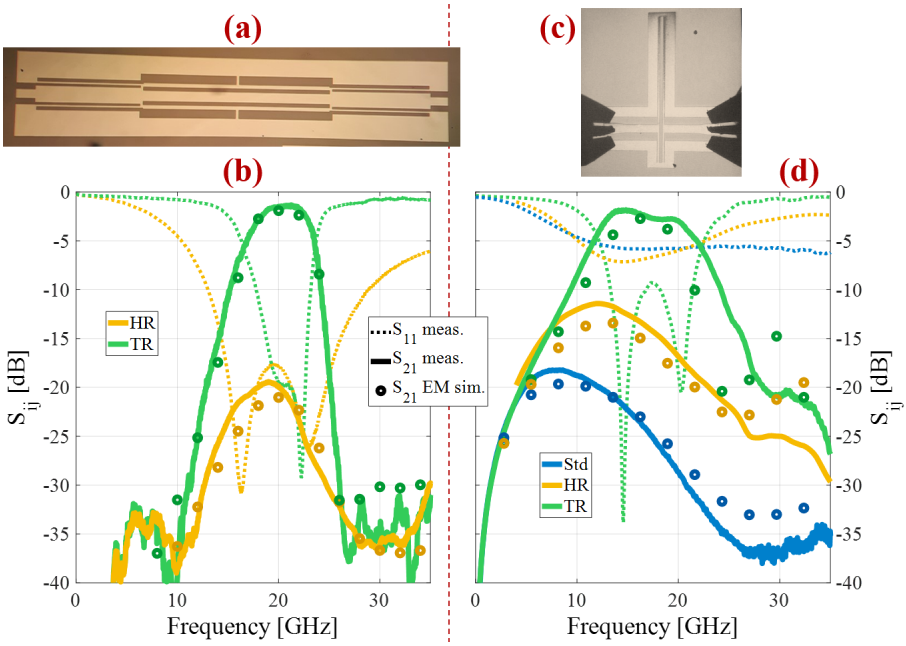


Figure 2.8: (a) Layout and (b) frequency response of a third-order edge-coupled CPW bandpass filter (topology and dimension in [85]). (c) Layout and (d) frequency response of a second-order interdigital CPW bandpass filter (topology and dimension in [86]).

The S_{21} parameter characterizes the power transmission from port 1 to port 2. The filters on the TR substrate show excellent bandpass response in the 15-20 GHz range with around 2 dB insertion loss that is almost entirely attributed to the metallic losses of the 1 µm-thick aluminium conductor.

The HR and Std substrates show poor performance with high insertion loss even in the filter passband, due to the lossy nature of these substrates.

2.2.3 On-Chip Antennas

High-quality RF substrates also enable the option of integrated antennas, that are of particular interest as operation frequencies increase toward mm-wave bands, as antenna sizes scale down to the order of 1 mm and the prospect of including them on-chip becomes a real consideration.

The study of substrate impact on integrated monopole antennae from [87] is depicted in **Figure 2.9**. The antennae were fabricated on the three main silicon-based substrates: Std, HR and TR.

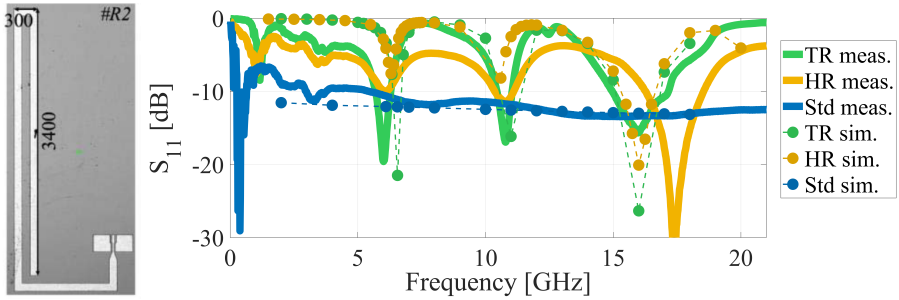


Figure 2.9: On-chip integrated UWB monopole antenna [87]. **(a)** Photograph of the fabricated antenna (units given in µm). **(b)** Measured (solid lines) and simulated (dashed lines) return loss of the integrated antenna on different Si substrates.

Figure 2.9 plots the return loss S_{11} of the measured device on each substrate, and the data pertaining to the TR sample clearly shows resonant behavior at 6.1 GHz, 11.8 GHz and 16.7 GHz. On that sample, few losses can be deduced by noticing that the out of band reflection coefficient S_{11} is large (i.e. close to 0 dB).

For the HR substrate, the resonant peaks are less deep and the out of band reflection is lower, indicating power loss in the substrate material as compared to the TR.

Substrate impact further degrades the antenna performance when considering the Std silicon substrate, in which substrate dissipations (Joule effect) overshadow any radiated energy.

2.3 Substrate Noise Coupling: Crosstalk and Isolation

In order to allow for high levels of cointegration in the RF and millimeter wave bands, it is of critical importance to minimize the crosstalk levels that propagate through the substrates themselves to interfere with neighboring devices and systems.

To evaluate these crosstalk levels in each substrate, the passive structure shown in **Figure 2.10 (a)** is implemented and measured on each of the SOI samples. It is a two-port device made up of two large metallic pads, accessed by short CPW lines **[88–90]**.

With reference to the parameters presented in **Figure 2.10 (b)**, the designed crosstalk pads have a length L of 150 µm, a width W of 50 µm, and a spacing S between them of 50 µm.

The substrate coupling is evaluated through the magnitude of the measured S_{21} parameter on all substrates, and these are plotted in **Figure 2.10 (c)**.

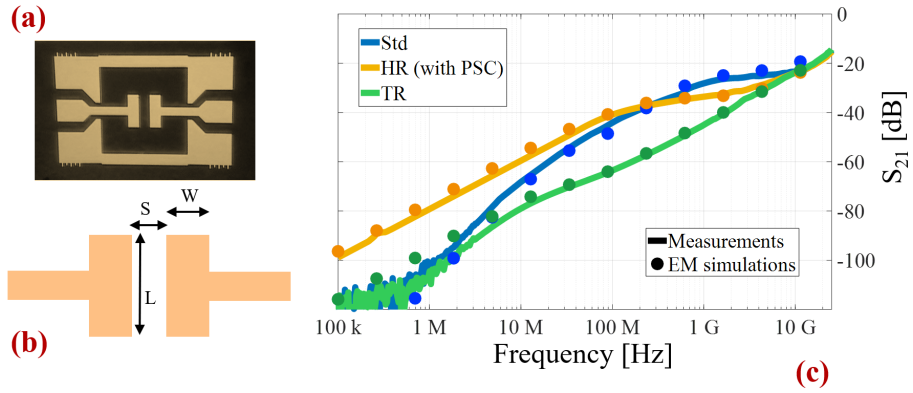


Figure 2.10: Measured and simulated passive two-port crosstalk structure. **(a)** Photograph of the physical structure defined on all substrates. **(b)** Dimension parameters of the crosstalk structure: L=150 µm, W=50 µm, S=50 µm. **(c)** Comparison of the crosstalk levels and frequency behavior on the three SOI substrates under consideration.

The Std and HR substrates present the highest coupling levels. The HR coupling curve shows a strong flattening tendency (resistive behavior) between 100 MHz and 4 GHz that is due to its low effective resistivity. The Std coupling curve shows the same behavior at slightly higher frequencies, between 1 and 10 GHz, which is due to its slightly lower effective resistivity. The TR on the

other hand shows a flattening behavior at much lower frequencies, between 15 MHz and 60 MHz, which in turn is due to a much higher effective resistivity, which agrees well with the electrical parameters extracted from CPW line measurements from **Figure 2.3**.

At very high frequencies all substrates eventually stop acting as resistive elements, and all the coupling is predominantly capacitive[15].

EM simulations of the full layout using the calibrated material stack agree well with the measured data.

[15] To further reduce the coupling level, lower permittivity is required, and an alternative porous-silicon substrate solution is presented in **Section 8.5** to this effect, yielding very high-quality substrate properties for RF applications.

2.4 Substrate Linearity: Signal Distortion Induced by Silicon-Based Substrate Materials

RF circuits that behave in a non-linear fashion are usually undesirable in a system chain. Indeed, a non-linear transfer function associated to a device, circuit, interconnect or module translates into signal distortion between the input waveform and the output waveform. In the frequency domain, this corresponds to a smearing of the spectral content, with distortion components being generated outside of the initially allocated band.

As the latest communication standards (such as 4G LTE-Advanced and 5G) require devices in the RF front-end modules to perform with higher linearity (see **Table 1.1**), the linearity burden is also increased at all levels of RF chip: from system design and RF circuit modules down to engineered substrate design **[34, 91]**.

As discussed in **Section 1.2.1**, carrier aggregation (CA) techniques employing multiple frequency bands close to each other impose higher performance requirements on RF components **[33, 35]**, especially in terms of crosstalk isolation and linearity, both of which are sources of spectral cross-contamination between bands.

Linearity of front-end circuitry is therefore of first importance, and a significant amount of the overall distortion can originate from the silicon-substrate itself. Indeed, in **[92]** it was shown that substrate non-linearity was dominating over transistor non-linearity for the case of an integrated DC-5 GHz SOI SPDT switch module on a HR substrate.

Semiconductor materials are non-linear by nature, as their local electrical properties depend on the electric field that penetrates them, and for these reasons, it is important to take substrate non-linearities into account when working at high frequencies and/or with sensitive modulation techniques (CA for example).

In order to evaluate harmonic distortion originating from the substrate, a simple CPW line structure is employed. Large-signal measurements of the CPW lines are performed on-wafer using a dedicated setup **[93, 94]** based usually on a Performance Network Analyzer (PNA) or on a spectrum analyzer and signal generator.

In general, when a circuit element described by a non-linear transfer function is fed a pure single tone of frequency f_0 at its input, the output signal can be described as having frequency components at integer multiples of the fundamental frequency f_0.

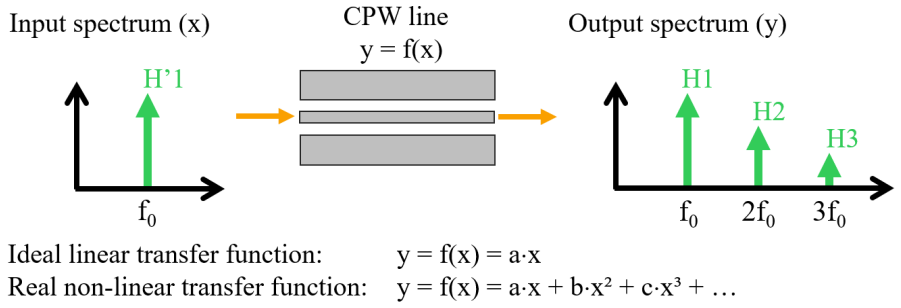


Figure 2.11: Principle of harmonic distortion from non-linear devices (under single-tone excitation). The CPW line is used to evaluate and benchmark substrate linearity.

To investigate and compare substrate non-linearities, a single tone with fundamental frequency f_0 of 900 MHz is injected into one port of the CPW line. The power of this input tone, which we shall denote as *H'1*, is swept from -30 dBm to +25 dBm using 50 Ω reference port impedances, and the output signal is retrieved and analyzed in terms of its frequency components. This principle is illustrated in **Figure 2.11**. Due to the non-linear behavior of silicon-based substrates signal distortion is introduced and the output signal is in general a multi-tone signal, with a fundamental component (f_0 of 900 MHz in our case), denoted as *H1*, along with harmonic components at all integer multiples of this fundamental frequency, denoted as *H2* (at 1.8 GHz), *H3* (at 2.7 GHz) and so on. In general, *H2* is the dominant component in CPW lines[16], and it is sufficient to compare substrate linearity performance in terms of generated *H2*. **Figure 2.12** then plots the *H2* component for increasing fundamental output power *H1* obtained from on-wafer measurements of a 2.1 mm-long CPW line on the three types of SOI substrates under consideration.

The practical implementation of the on-wafer large-signal measurement setup up to +25 dB of input power is described in **Appendix 7.3**.

The electrical characteristics of Std and HR substrates are strongly voltage-dependent **[94–97]**, and consequently these two substrates show high levels of harmonic distortion (HD). This occurs as the substrate impedance associated to these substrates varies as a function of the applied signal. Large amplitude voltage signals modify the free carrier distributions in the underlying silicon substrate, as it is pulsed through inversion/depletion/accumulation states over

[16] For usual power ranges, up to 1 W (30 dBm), for most silicon-based substrates.

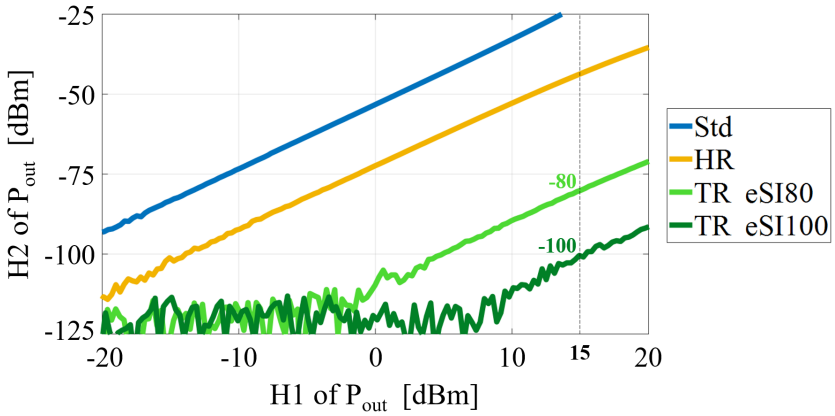


Figure 2.12: Power of second harmonic (at 1.8 GHz) component *H2* plotted versus power of fundamental component *H1* (at 900 MHz) of the output signal of a 2.1 mm CPW line (central conductor width of 26 µm and a spacing of 12 µm between conductors) implemented on the considered types of SOI substrates. The applied bias on the CPW line relative to the substrate is $V_{DC} = 0$ Volts.

time in response to the large signal (the field effect). This leads to relatively high harmonic distortion at the output of the CPW line, induced by the voltage-sensitive Std and HR silicon substrates.

The introduction of the polysilicon trap-rich layer beneath the BOX of a nominally high resistivity substrate brings 40 to 60 dB reductions of distortion over the measured power range **[94, 98, 99]**. The traps at the Si/SiO_2 interface effectively pin the Fermi level near mid-gap[17]. Contained to a narrow energy range by these traps, the position of the Fermi level is rendered much less voltage-sensitive, improving the linearity of the substrate and reducing the substrate-induced distortion of signals propagating through overlying transmission lines. For this reason, trap-rich (TR) SOI substrates provided by Soitec are also named "RFeSI^{TM}", which stands for "*RF enhanced Signal-Integrity*" **[34, 45]**. Different flavors of RFeSI^{TM} wafers can be found on today's market. The RFeSI80^{TM} product presents a low *H2* distortion level at -80 dBm for a fundamental component *H1* of +15 dBm **[100]**, while the RFeSI100^{TM} boasts an even lower level at -100 dBm[18], thanks to a combination of a higher quality

[17] Details on the physics of trapping mechanisms is given in **Chapter 3**, **Section 3.2**.

[18] For the reference CPW device used for substrate linearity benchmarking, which has a signal

polysilicon layer and a lower doping level of the substrate handle[19].

In today's market (2020), 300 mm diameter TR wafers are commercially available for the most advanced PD-SOI nodes (180 nm to 45 nm) and are truly optimized with their high linearity (and low losses) to enable RF and telecommunication applications.

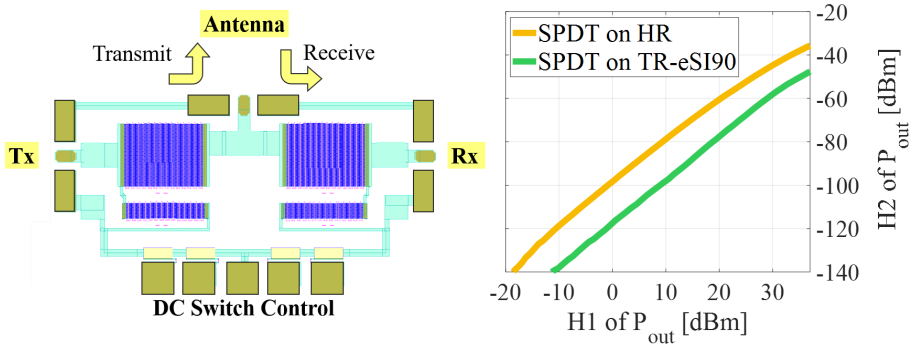
line width of $W_C = 26$ µm, a spacing to ground lines of $S = 12$ µm, and a line length of 22.1mm.

[19] Material parameter impact on substrate linearity will be studied in **Chapter 5**.

2.5 Substrate Linearity Impact on an RF-SOI Switch Module

Substrate linearity impact is directly observed on switch performance. The DC-5 GHz SPDT switch module from **[92]**, implemented using a 180 nm PD-SOI technology node from TowerJazz[20], is depicted in **Figure 2.13 (a)**.

The switch is measured using the same harmonic distortion setup **[93, 94]** as the CPW lines for substrate benchmarking (see **Appendix 7.3**).



(a) **(b)**

Figure 2.13: Harmonic distortion of a DC-5 GHz SPDT module in 180 nm PD-SOI technology on two types of substrate, HR and TR SOI **[92]**. **(a)** Switch layout. **(b)** Power of second harmonic (at 1.8 GHz) component *H2* plotted versus power of fundamental component (at 900 MHz) of the output of an SPDT RF switch PD-SOI implemented on HR and TR SOI substrates. The switch is in the state that connects Tx to Antenna. The large signal is introduced at the Tx port, and the harmonics are measured at the Antenna port. The Rx port is loaded to 50 Ω.

Identical SPDT circuit modules are implemented on two types of SOI substrates, a HR SOI and an RFeSI90^{TM} TR-SOI. The switch is measured under large signal at 900 MHz in the ON-state from the Tx port to the Antenna port, while the Rx port is loaded to 50 Ω. The harmonic distortion results are given in **Figure 2.13 (b)**.

It is shown that approximately 20 dB of linearity increase is achieved by substituting the HR substrate with a TR RFeSI90^{TM} substrate, highlighting the substrate's impact on overall signal distortion in RF modules.

[20] Rebranded as *Tower Semiconductor* as of March 2020.

2.6 Impact of DC Bias on RF Substrate Performance

Because the semiconductor substrates are voltage sensitive, their performance, in terms of both small signal ρ_{eff} and large signal HD, depend on the DC bias conditions.

These RF substrate figures of merit are plotted in **Figure 2.14**, where **(a)** plots the second harmonic curves $H2$ as a function of fundamental output power at various DC bias points. The DC bias is applied to the central signal line with respect to the substrate and CPW ground lines that are set as the potential reference. Measurements of a HR substrate show that substrate linearity varies by more than 30 dB as a function of the applied bias, as presented in **(c)**, while **(b)** plots the bias dependency on effective resistivity.

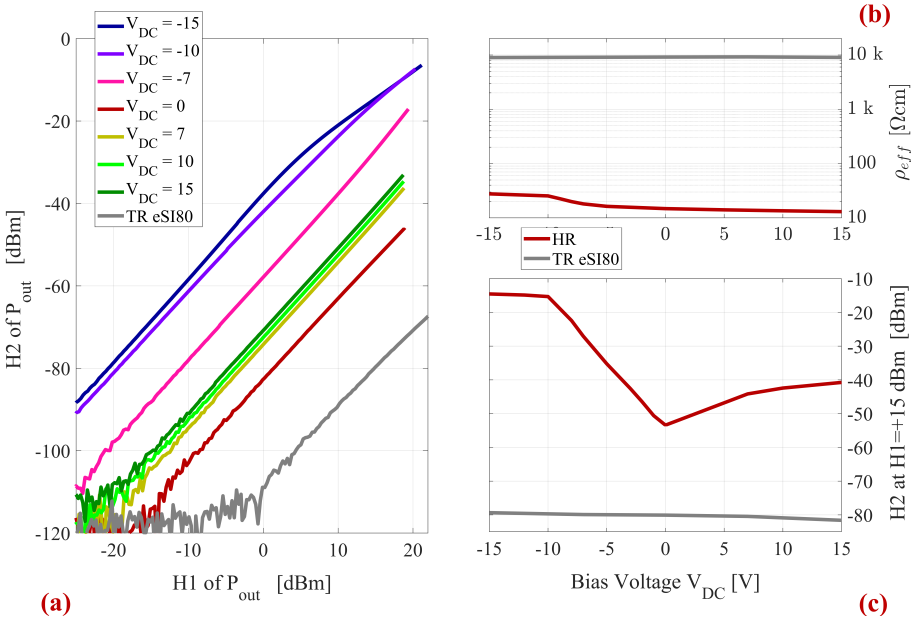


Figure 2.14: **(a)** Power $H2$ of second harmonic component vs fundamental component $H1$ at the output of a 2.1 mm CPW line at 900 MHz, on a HR and TR substrate at various DC line bias conditions relative to the substrate. **(b)** Effective resistivity (extracted above slow wave mode) vs DC line bias. **(c)** $H2$ at +15 dBm of $H1$ vs DC line bias.

TR samples present flat $\rho_{eff}(V_{DC})$ and $H2(V_{DC})$ curves, as presented in **Figure 2.14**.

Physical explanations for all bias dependencies will be given in **Chapter 3**.

In general throughout this thesis, harmonic levels will be analyzed at a fundamental output power of $H1 = +15$ dBm, and plotted against the DC bias, in both presented measurements and simulations.

2.7 Chapter Summary

At high frequency, the accurate modelling of parasitic elements is crucial to IC design. This is especially true in advanced nodes that are usually expensive, and it is therefore a cost requirement to minimize the number of fabrication iterations before obtaining a functional product. Substrate behavior is a significant contributor to such parasitics, and its modelling is a challenge, as non-uniform resistivity profiles are expected in semiconductor materials.

In this chapter, *substrate impact* on RFICs was overviewed, based on on-wafer measurements of integrated CPW lines, spiral inductors, mm-wave filters, antennas and crosstalk devices that were fabricated on several types of substrates.

The need for a low-loss and linear silicon-based substrate at RF was highlighted to open up the RF design space to a wider range of high-quality passive elements.

To facilitate substrate analysis, the concept of *effective resistivity* was introduced and its mathematical definition and extraction procedure, from CPW line S-parameter data (measured or simulated), was reviewed.

The *parasitic surface conduction (PSC)* effect was presented, demonstrating that in practice obtaining low-loss substrates requires more than simply reducing the nominal doping, as PSC counteracts the HR bulk properties. The trap-rich SOI wafer technology was developed to tackle this particular PSC problematic by passivating the interface with a polysilicon layer rich in defects, and has been widely adopted for high-quality RF-SOI applications. PD-SOI technology has a unique compatibility with the trap-rich substrate solutions as optimizations and engineering at the substrate-level, below the BOX, can be made without affecting the device level silicon above it.

This chapter also presented a small-signal simulation methodology, combining an EM solver with a semiconductor TCAD tool.

The TCAD tool is employed to obtain the resistivity profile throughout the substrate, capable of accounting for interface charge, traps, dopant profiles and other material considerations. Such a profile is then discretized into a finite number of uniform material layers that serve to define the electromagnetic environment of the EM solver. With this approach, good simulation to hardware correlation was obtained for the wide range of aforementioned integrated RF passive devices.

Finally, the importance of substrate linearity was highlighted in this chapter as a key figure of merit that is imposed by the stringent requirements of advanced generations of telecommunication standards. Large-signal modelling of semiconductor substrates at RF frequencies is a challenge, and is the main object of the next three chapters of this thesis.

II Substrate Modelling Techniques

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Overview of Part II

Part II describes the core work of this thesis: modelling and understanding the physical mechanisms at play in a semiconductor substrate under large-amplitude RF excitation.

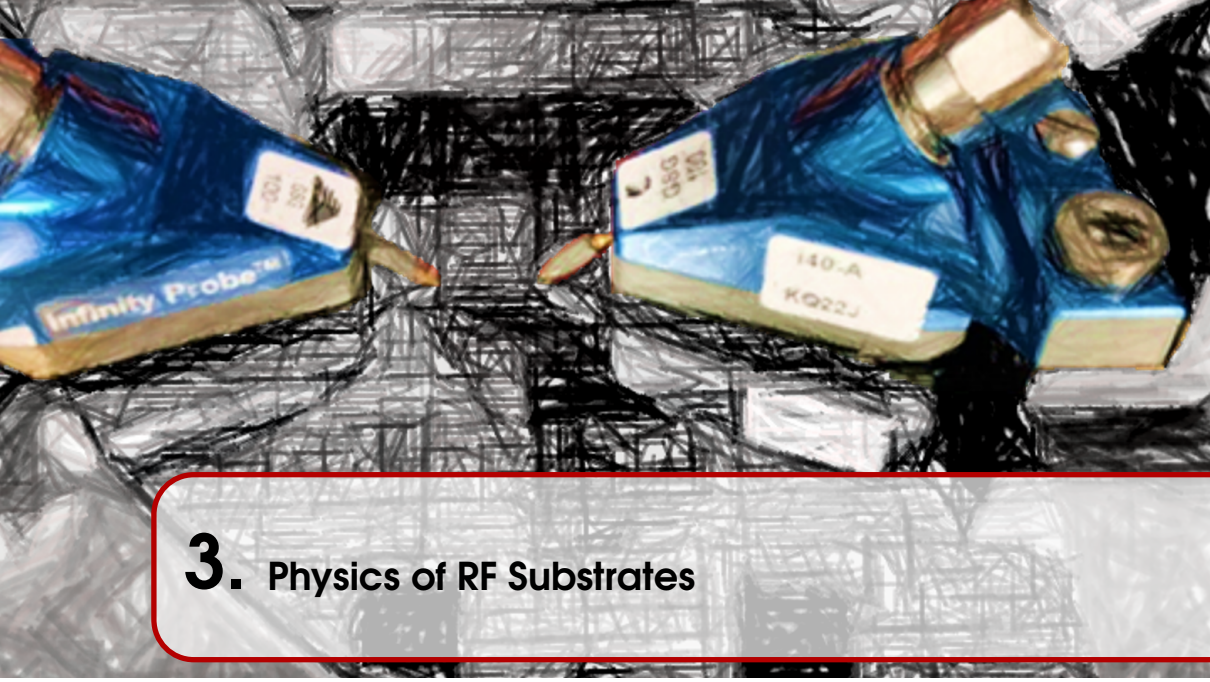
In order to model the impact of substrate non-linearities in metal-insulator-semiconductor (MIS) devices, a solid understanding of semiconductor physics is required.

Chapter 3 starts by presenting the definitions and equations associated to interface charge and acceptor and donor traps. Static analysis based on TCAD tools give strong insight into the charge-balance interplay between a PSC layer and trap-rich types of surface passivation.

Rigorous RF dynamic analyses are then considered, which deliver strong physical understanding of carrier and trap inertia and finite response times.

The main results of this chapter have been published in **[101]**.

Chapter 4 builds on this understanding to develop a large-signal model capable of evaluating substrate-induced harmonics at the output of a CPW line that is excited by a large-amplitude RF signal at its input.



3. Physics of RF Substrates

In order to model the impact of substrate non-linearities in metal-insulator-semiconductor (MIS) devices, a solid understanding of semiconductor physics is required.

This chapter then starts by presenting the definitions and equations associated to interface charge and acceptor and donor traps. It follows suit by laying out semiconductor transport equations, and generation/recombination statistics, as well a formulating charge-balance equations as a function of applied voltage (DC or RF), ionized traps and fixed oxide charge.

Following from that, these equations are put to use in a TCAD solver in order to simulate pertinent examples that give strong insight into the impact of such semiconductor material and interface properties on the RF substrate FoMs.

First, a static analysis is considered in order to illustrate the working principle of how a trap-rich type of interface passivation can overcome the PSC effect. The concept of Fermi-level pinning is introduced for such trap-rich interfaces.

Next, substrates are analyzed in response to dynamic excitation signals.

Using step functions to pulse a MIS structure from a strong negative applied charge to a strong positive applied charge provides physical insight into carrier dynamics. The characteristic time constants associated to variations in trap occupancy and/or to variations in free carrier densities are discussed.

Then, large-amplitude sinusoidal RF signals are considered. Such excitations enable us to analyze the harmonic distortion for various types of substrates. The practical implementation of the HD simulation methodology developed in this thesis is detailed in **Chapter 4**, though the core underlying physical principles and their interpretation are discussed in this chapter.

3.1 Interface Charges

Interfaces between silicon dioxide and silicon are imperfect, and suffer from structural defects, traps, and contamination. These effects lead to a net charge density associated to such interfaces.

Such charge is usually undesirable, and is commonly qualified as *parasitic*, as it is not a well controlled parameter during the fabrication process.

It can have the impact of shifting MOSFET behavior form its intended electrical characteristics (uncontrolled shift in threshold voltage). Furthermore, as discussed in the previous chapter, fixed oxide charges are responsible for inducing a parasitic surface conduction layer (PSC) at the oxide interface with the substrate, that significantly degrades its RF performance.

There are several physical contributions to charges associated to a material interface or volume:

- **Fixed Oxide Charge Q_f cm^{-2}**. This charge is primarily due to structural defects at the oxide surface, such as positively ionized silicon, and is typically located less than 2.5 nm from the Si/SiO_2 interface **[102]**. The density of fixed charge is strongly related to the oxidation process, and depends on crystal orientation, on process temperatures, as well as on the cooling conditions **[103]**. It is important to note that the atomic centers associated to fixed charge do not interact with free carriers to either charge or discharge (as is the case for trapped charge), and Q_f is therefore considered as independent from any electrical stimulus. Fixed charge associated to Si/SiO_2 interfaces is invariably positive.
- **Mobile Ionic Charge Q_m cm^{-3}**. As opposed to fixed charges, the positions of mobile charges can change within the dielectric layer in response to some electrical stimulus **[104]**. They are primarily due to ionic impurities in the oxide layer[1].
- **Interface Trapped Charge Q_{it} cm^{-2}**. The imperfections at the material interface introduce new energy states into the forbidden energy gap at the surface. The origin of such states can be due to structural defect or atomic impurities. Because theses states are located at the Si/SiO_2 interface, they can interact easily with free carriers in the silicon, and so, unlike fixed charge, the atomic centers associated with trapped charge may charge or discharge through capture and emission processes of free

[1] Such as Li^+, Na^+, K^+, and H^+. Negative ions and heavy metals may also contribute to such charge even though they are not mobile below approximately 500 °C **[102]**.

electrons and holes. The net interface trapped charge is therefore the difference between the charge of positively ionized trap centers, Q_{it}^{+}, and the charge of negatively ionized trap centers, Q_{it}^{-}. These ionized densities depend on the total density of trapping centers, along with the trap's energy position relative to the surface potential.

- **Oxide Trapped Charge Q_{ot} cm^{-3}**. Theses charges represent ionized trap centers that are not located at the interface, but that are in the bulk of the oxide layer. By this physical separation from the silicon, these traps do not interact easily with free carriers in the substrate. These states may still charge and discharge due to processes such as ionizing radiation or avalanche injection **[102]**.
- **Polarization Charge Q_{pol} cm^{-2}**. Polarization effects include spontaneous and piezoelectric polarization. The spontaneous polarization refers to the built-in polarization field present in an unstrained crystal. This occurs in polar crystals that lack inversion symmetry. The Wurtzite-structure of AlGaN and GaN is an example of a polar crystal. The piezoelectric polarization results from an elastic distortion of a polar crystal lattice **[105, 106]**. Such a mechanical distortion can arise in heterostructures, where materials of different lattice parameters are stacked. Conversely, an applied electric field can induce an elastic distortion. This means that the equivalent sheet charge associated with a polarization effect may depend on electrical stimuli.

In this work

In the context of this thesis, we shall not encounter any physical processes capable of significantly altering the ionized oxide trap densities, and Q_{ot} will be treated as constant for all presented experiments.

Mobile charges are typically quite slow, and their effects can certainly be neglected at RF frequencies and beyond. For these reasons, their contributions are also considered constant in our RF experiments[2].

[2]Some samples considered in this work present hysteresis effects in C-V measurements of vertical MOS capacitor structures (not printed in this text). It should be noted that such hysteresis effects in C-V measurements are quite a rare occurrence in the most common types of HR and TR substrates that we shall consider. It is likely that they are due to mobile charges in the dielectric layer above the silicon bulk. A full C-V sweep can be seen as a transient large-signal with a time period in the order of a few seconds, during which mobile charges have time to significantly move in response to the applied stimulus and alter the effective dielectric charge density.

We then define an *equivalent fixed interfacial oxide charge density*:

$$Q_{ox} = Q_f + \int_0^{t_{ox}} Q_m(y) + Q_{ot}(y)\, dy \quad [\mathrm{cm}^{-2}] \tag{3.1}$$

that is considered constant and fixed, i.e. independent of the applied electrical stimulus of our experiments and simulations.

Such an assumption should not be made for Q_{it} and Q_{pol} as they may depend strongly on the electrical signals during our experiments.

Traps at the Si/SiO_2 interface play an instrumental physical role enabling high quality RF trap-rich substrates, and their dependence on applied signals is crucial. For this reason, the entire next section is dedicated to the physics of trapped charge. The name Q_{it} is generally reserved for interface traps. In the next section, the nomenclature will change to Q_{trap}, as volumetric traps within a polysilicon layer will be the primary focus. Know that Q_{it} can be associated to Q_{trap} in a totally similar way.

Spontaneous polarization or strain-induced piezoelectric effect will not be considered, and this charge contribution term is then assumed to be zero for all experiments (measured or simulated substrates) of this thesis[3].

[3]This charge contribution should be accounted for in GaN on Si type technology, involving polar crystal materials **[107]**. In terms of modelling, it is then convenient to represent polarization charge as two sheet layers of interface charge of equal magnitude and opposite sign at each interface of the polar crystal **[108]**.

3.2 Traps

3.2.1 Trapping Equations and Physics

In general, all semiconductor materials exhibit crystal flaws. These can originate from the presence of impurities in the substrate or by unsatisfied dangling bonds at material interfaces. Polysilicon presents many grain boundary interfaces along which high densities of trapping states are present, which is why it is used in the so called *trap-rich* substrates.

The presence of these defect centers, or traps, in semiconductor substrates may significantly influence the electrical characteristics of the material. In the case of *trap-rich*, the large-amount of traps pin the Fermi level near midgap, in a highly resistive state. This has the effect of eliminating the parasitic surface conduction (PSC) present in high-resistivity samples thereby reducing substrate loss and improving linearity.

Indeed, trap centers, whose associated energy level lies in the forbidden gap, exchange charge with the conduction and valence bands through the emission and capture of electrons. The trap centers contribute to the density of space charge in the semiconductor. Poisson's equation relates the electric potential $\phi(\bar{r})$ to the space charge distribution $\rho_q(\bar{r})$ at each spatial coordinate $\bar{r} = [x, y, z]$. Poisson's equation and space charge density are expressed as:

$$\nabla^2\phi = -\rho_q/\varepsilon \qquad [\mathrm{V}\cdot\mathrm{cm}^{-2}] \qquad (3.2)$$

$$\begin{aligned}\rho_q &= q\cdot\left(p - n + N_{tD}^{+} - N_{tA}^{-}\right)\\ &= Q_{free} + Q_{ionized} = Q_{free} + Q_{trap} \qquad [\mathrm{C}\cdot\mathrm{cm}^{-3}] \qquad (3.3)\end{aligned}$$

$$Q_{free} = q\cdot\left(p - n\right) \qquad [\mathrm{C}\cdot\mathrm{cm}^{-3}] \qquad (3.4)$$

$$Q_{trap} = q\cdot\left(N_{tD}^{+} - N_{tA}^{-}\right) \qquad [\mathrm{C}\cdot\mathrm{cm}^{-3}] \qquad (3.5)$$

where ε is the electrical permittivity, q is the elementary charge, p and n are the free carrier densities, for holes and electrons respectively, and N_{tD}^{+} and N_{tA}^{-} are the densities of ionized donor and acceptor traps, respectively.

The charge density has been separated into two terms that will be useful for the analysis to come. The first term, Q_{free}, is the net charge density of free carriers. The second is the charge density of ionized centers $Q_{ionized}$. It will be convenient in later sections of this text to analyze the proportion of charge that is trapped, and the proportion of charge that is free, and that therefore contributes to substrate impedance. Note that $Q_{ionized} = Q_{trap}$ englobes all types of ionized

centers, including dopants[4].

In order to solve the semiconductor physics equations taking into account trap centers, their effect on generation and recombination statistics must be included **[109]**. **Figure 3.1 (a)** illustrates the four different charge exchange mechanisms between the trapping center, at a discrete energy position E_t, and the valence and conduction bands, whose edges are denoted as E_V and E_C, respectively.

[4]Dopants are merely a particular case of trap. A donor (acceptor) dopant is merely a trap center that is energetically close, with respect to the thermal energy kT, to the conduction (valence) band edge.

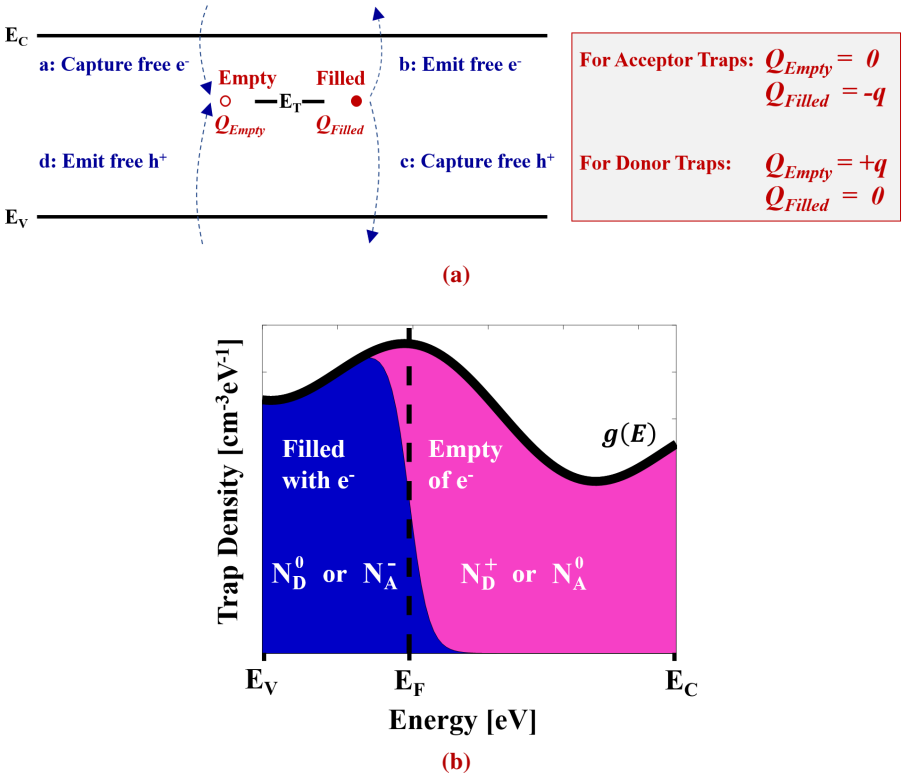


Figure 3.1: Principle of trapping states in the forbidden semiconductor band gap. **(a)** The four electronic capture and emission interactions of the trap with the conduction and valence bands. All arrows represent movements of electrons. **(b)** Example of the filled and empty trap states for an arbitrary trap distribution function $g(E)$. The trap's empty and filled charge that depends on the trap's type (donor or acceptor). The exponential roll-off (25 meV) in trap occupancy around E_F is due to Fermi-Dirac statistics (taken at 300 K in this example).

An empty trap can capture a free electron from the conduction band (mechanism **a**), or can capture an electron from the valence band, which creates a free hole (mechanism **d**).

A filled trap can do the opposite: it can either emit a free electron to the conduction band (mechanism **b**) or emit an electron to the valence band, which is equivalent to capturing a free hole (mechanism **c**).

Traps are organised into two categories: acceptors and donors. The differ-

ence between them is simply their net charge when filled and empty, as shown by the values for Q_{Filled} and Q_{Empty} in **Figure 3.1 (a)**. An empty acceptor trap has no charge and is negative when filled, while an empty donor is positively charged and is neutral when filled.

Often, trap states are not located at discrete energy positions but rather there is a continuous distribution of traps over the band gap. This is the case for traps in polysilicon, and an example is given in **Figure 3.1 (b)**, in which an arbitrary trap distribution function $g(E)$ is plotted.

Roughly speaking, at any given point in the material, trap states that are below the Fermi level E_F are filled, and traps above E_F are empty. This means that occupied (by an electron) acceptor states below E_F are negatively charged, while empty (of an electron) donor states above E_F are positively charged, and these terms contribute to the charge balance equations.

The ionized densities N_{tD}^{+} and N_{tA}^{-} depend upon the trap density, and on the probability of ionization, meaning the trap energy position E relative to the Fermi level E_F. For donor-type and acceptor-type traps respectively, the ionized densities are calculated as:

$$N_{tD}^{+}(\bar{r}) = \int_{E_V}^{E_C} g_D(E,\bar{r}) \cdot \big(1 - F(E,\bar{r})\big)\, dE \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.6)}$$

$$N_{tA}^{-}(\bar{r}) = \int_{E_V}^{E_C} g_A(E,\bar{r}) \cdot F(E,\bar{r})\, dE \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.7)}$$

and the non-ionized trap densities as:

$$N_{tD}^{0}(\bar{r}) = \int_{E_V}^{E_C} g_D(E,\bar{r}) \cdot F(E,\bar{r})\, dE \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.8)}$$

$$N_{tA}^{0}(\bar{r}) = \int_{E_V}^{E_C} g_A(E,\bar{r}) \cdot \big(1 - F(E,\bar{r})\big)\, dE \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.9)}$$

where $g_D(E)$ and $g_A(E)$ are the donor and acceptor trap-energy distributions, and $F(E)$ is the Fermi-Dirac occupation function given by:

$$F(E,\bar{r}) = \frac{1}{1 + \exp\left\{\frac{E - E_F(\bar{r})}{kT}\right\}} \qquad [\,/\,] \qquad \textbf{(3.10)}$$

and k is the Boltzmann constant, T is the crystal lattice temperature, and $E_F(\bar{r})$ is the local position of the Fermi level at spatial coordinates $\bar{r}$.

Graphically, N_{tD}^{+}, N_{tA}^{-}, N_{tD}^{0} and N_{tA}^{0} correspond to the blue and/or purple areas below the arbitrary trap distribution $g(E)$ of **Figure 3.1 (b)**.

The free carrier densities can be expressed in a similar formulation:

$$n(\bar{r}) = \int_{E_C}^{E_{MC}} N_C(E) \cdot F(E,\bar{r})\, dE \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.11)}$$

$$p(\bar{r}) = \int_{E_{mV}}^{E_V} N_V(E) \cdot \left(1 - F(E,\bar{r})\right) dE \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.12)}$$

where the density of permitted energy states in the conduction band and valence band $N_C(E)$ and $N_V(E)$ are multiplied by the occupation function and integrated over energy. For electrons (holes), the integration takes place from the minimum conduction (valence) band edge E_C (E_{mV}) to the maximum conduction (valance) band edge E_{MC} (E_V).

Close to the band edges, $N_C(E)$ and $N_V(E)$ can be approximated by **[110]**:

$$N_C(E) = \frac{\sqrt{m_C^3 (E - E_C)}}{\sqrt{2}\pi^2\hbar^3} \qquad [\mathrm{cm}^{-3} \cdot \mathrm{eV}^{-1}] \qquad \textbf{(3.13)}$$

$$N_V(E) = \frac{\sqrt{m_V^3 (E_V - E)}}{\sqrt{2}\pi^2\hbar^3} \qquad [\mathrm{cm}^{-3} \cdot \mathrm{eV}^{-1}] \qquad \textbf{(3.14)}$$

where $\hbar$ is the reduced Planck constant, and m_C and m_V are the effective masses of carriers in the conduction band and in the valence band, respectively.

In order to solve for $E_F(\bar{r})$, the trapping statistics equations need to be taken into account. In general, a trap is fully characterized by its energy level E_t and by its *electron capture cross-section* σ_n and *hole capture cross-section* σ_p. These parameters characterize the probability of the trap to capture or emit a carrier.

The capture cross-sections are expressed in cm^2 and are related to the carrier lifetimes by **[111]**:

$$\tau_n = \left(v_n \sigma_n p_t\right)^{-1} \qquad [\mathrm{s}] \qquad \textbf{(3.15)}$$

$$\tau_p = \left(v_p \sigma_p n_t\right)^{-1} \qquad [\mathrm{s}] \qquad \textbf{(3.16)}$$

where v_n and v_p are the thermal velocities for electrons and holes, respectively. n_t and p_t are the concentrations of filled and empty traps, respectively, calculated from the trap density N_t at energy E_t as follows:

$$N_t = n_t + p_t \qquad [\mathrm{cm}^{-3}] \qquad (3.17)$$

$$n_t = N_t F(E_t) \qquad [\mathrm{cm}^{-3}] \qquad (3.18)$$

$$p_t = N_t\big(1 - F(E_t)\big) \qquad [\mathrm{cm}^{-3}] \qquad (3.19)$$

It is therefore shown that τ_n and τ_p depend on the trap energy position E_t. Parameters n_t and p_t are linked to the previously defined filled/empty trap densities N_{tD}^{+}, N_{tA}^{-}, N_{tD}^{0} and N_{tA}^{0} in the following manner[5].

The lifetime of an electron τ_n (hole τ_p) is the mean time before an electron (hole) is captured. It is not an inherent property of the carrier, as it depends on the number of traps empty of electrons p_t (of holes n_t)[6].

The time constants of a trap can be expressed in a similar way:

$$\tau_{tn} = \big(v_n \sigma_n n\big)^{-1} \qquad [\mathrm{s}] \qquad (3.20)$$

$$\tau_{tp} = \big(v_p \sigma_p p\big)^{-1} \qquad [\mathrm{s}] \qquad (3.21)$$

τ_{tn} is the mean time before an empty (of electron) trap captures an electron. τ_{tp} is the mean time before an empty (of hole) trap captures a free hole. These trap time constants are not inherent properties of the trap, but depend on the free carriers concentrations.

Referring to **Figure 3.1 (a)**, the emission and capture rates associated to the

[5] If multiple trap levels or continuous state distributions are considered, then τ_n and τ_p are not unique, but rather depend on energy such that a carrier lifetime is associated to each trap level. As an example, **Equation 3.7** can be rewritten as: $N_{tA}^{-} = \int_{E_V}^{E_C} n_{tA}\, dE_t$, where we define $n_{tA} = N_{tA} F(E_t) = g_A(E_t) F(E_t)$. Similarly, **Equation 3.8** can be rewritten as: $N_{tD}^{0} = \int_{E_V}^{E_C} n_{tD}\, dE_t$, where we define $n_{tD} = N_{tD} F(E_t) = g_D(E_t) F(E_t)$. There are then time constants of the form of those given by **Equations 3.15 and 3.16** that writes for electrons as $\tau_{nX}(E_t) = \big(v_n \sigma_{nX} n_{tX}(E_t)\big)^{-1} = \big(v_n \sigma_{nX} N_{tX} F(E_t)\big)^{-1}$, where X represents a unique trap species, acceptor or donor, with density N_{tx} at energy E_t with electron capture cross section σ_{nX} (which may in general not be single valued for a given distribution but may also depend on energy). Each trap species at each energy level provides a unique $\tau_{nX}(E_t)$.

[6] In **Section 3.4** we shall consider large amplitude transient simulations in time-domain. Ultimately, thermal generation and recombination processes, governed by such time constants, will provide the free carriers necessary to reach equilibrium. We can note here already that, in general, these lifetimes will not remain constant valued over the entire transient response time, as they depend on trap occupancy n_t and p_t that will also change over time.

four electron exchange processes with the trap can be expressed as [109]:

$$r_a = n \cdot p_t \cdot v_n \sigma_n \qquad [\mathrm{cm}^{-3} \cdot \mathrm{s}^{-1}] \qquad (3.22)$$

$$r_b = n_t \cdot N_C \cdot v_n \sigma_n \cdot \exp\left\{\frac{E_t - E_C}{kT}\right\} \qquad [\mathrm{cm}^{-3} \cdot \mathrm{s}^{-1}] \qquad (3.23)$$

$$r_c = n_t \cdot p \cdot v_p \sigma_p \qquad [\mathrm{cm}^{-3} \cdot \mathrm{s}^{-1}] \qquad (3.24)$$

$$r_d = N_V \cdot p_t \cdot v_p \sigma_p \cdot \exp\left\{\frac{E_V - E_t}{kT}\right\} \qquad [\mathrm{cm}^{-3} \cdot \mathrm{s}^{-1}] \qquad (3.25)$$

where N_C and N_V are the effective densities of states in the conduction band and in the valence band, respectively (not to be confused with the energy state distribution functions $N_C(E)$ and $N_V(E)$ of **Equations 3.13 and 3.14**). N_C and N_V and are also useful in rewriting **Equations 3.11 and 3.12** of n and p:

$$n = N_C \cdot \exp\left\{\frac{E_F - E_C}{kT}\right\} \qquad [\mathrm{cm}^{-3}] \qquad (3.26)$$

$$p = N_V \cdot \exp\left\{\frac{E_V - E_F}{kT}\right\} \qquad [\mathrm{cm}^{-3}] \qquad (3.27)$$

$$n_i = \sqrt{np} = \sqrt{N_C N_V} \cdot \exp\left\{\frac{-E_g}{2kT}\right\} \qquad [\mathrm{cm}^{-3}] \qquad (3.28)$$

where n_i is the *intrinsic carrier density* in the semiconductor under equilibrium, and $E_g = E_C - E_V$ is the *band gap* energy.

Table 3.1 decomposes these rate equations into their fundamental terms. Each process involves an electron moving from a first energy level, *State 1*, to a second energy level, *State 2*. Each rate equation is the product of the number of electrons in *State 1* by the number of vacancies in *State 2* by the trap's emission/capture probability ($v\sigma$).

Processes **b** and **d** involve an electron being transferred to a higher energy state. For these processes, an additional term appears in the rate equations to take into account the probability of the necessary thermal energy being available to the electron[7].

Equilibrium is reached when the generation rate is equal to the recombination rate for both electrons and holes:

$$r_a = r_b \qquad \text{at equilibrium} \qquad [\mathrm{cm}^{-3} \cdot \mathrm{s}^{-1}] \qquad (3.29)$$

$$r_c = r_d \qquad \text{at equilibrium} \qquad [\mathrm{cm}^{-3} \cdot \mathrm{s}^{-1}] \qquad (3.30)$$

[7] This $\exp\{\Delta E/kT\}$ term is simply the Boltzmann approximation of the Fermi-Dirac function.

Process	State 1	State 2	Number of Electrons in State 1	Number of Vacancies in State 2	Cstn	Probability of Required Energy
a	E_C	E_t	n	p_t	$v_n\sigma_n$	1
b	E_t	E_C	n_t	N_C	$v_n\sigma_n$	$\exp\left\{\frac{E_t-E_C}{kT}\right\}$
c	E_t	E_V	n_t	p	$v_p\sigma_p$	1
d	E_V	E_t	N_V	p_t	$v_p\sigma_p$	$\exp\left\{\frac{E_V-E_t}{kT}\right\}$

Table 3.1: Decomposition of the four trap-assisted generation/recombination processes represented in **Figure 3.1 (a)**. In general, each process involves transferring an electron from *State 1* to *State 2*.

The rates expressed by **Equations 3.22-3.25** contribute to the electron and hole continuity equations, as expressed by:

$$\frac{\partial n}{\partial t} = +\frac{1}{q}\nabla\cdot\overline{J_n} + G_n - U_n \qquad [\mathrm{cm}^{-3}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.31)}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\nabla\cdot\overline{J_p} + G_p - U_p \qquad [\mathrm{cm}^{-3}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.32)}$$

$$U_n = r_a - r_b \qquad [\mathrm{cm}^{-3}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.33)}$$

$$U_p = r_c - r_d \qquad [\mathrm{cm}^{-3}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.34)}$$

$$\overline{J_n} = q\left(n\mu_n\overline{\mathscr{E}} + D_n\nabla n\right) \qquad [\mathrm{C}\cdot\mathrm{cm}^{-2}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.35)}$$

$$\overline{J_p} = q\left(p\mu_p\overline{\mathscr{E}} - D_p\nabla p\right) \qquad [\mathrm{C}\cdot\mathrm{cm}^{-2}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.36)}$$

$$D_n = \mu_n\frac{kT}{q} \qquad [\mathrm{cm}^{2}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.37)}$$

$$D_p = \mu_p\frac{kT}{q} \qquad [\mathrm{cm}^{2}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.38)}$$

where U_n and U_p represent the net recombination rate of electrons and holes respectively through trapping centers.

G_n and G_p represent external generation mechanisms, such as photogeneration and impact ionization. Throughout this thesis, no such phenomena will be considered, and so for all presented experiments we will have $G_n = G_p = 0$.

$\overline{J_n}$ and $\overline{J_p}$ are the electron and hole current densities, respectively. They are made up of a drift current term, proportional to the electric field $\overline{\mathscr{E}}$, and of a diffusion current term. This latter term is equal to the concentration gradient multiplied by the diffusivity $D_{n,p}$.

A continuity equation for each trap center can also be written, pertaining to the filled and empty trap densities and there rates of variation:

$$\frac{\partial n_t}{\partial t} = -\frac{\partial p_t}{\partial t} = U_p - U_n = r_b + r_c - r_a - r_d \qquad [\mathrm{cm}^{-3}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.39)}$$

Equations 3.31-3.39 will be useful in later sections of this text, particularly in **Section 3.4** for analyzing carrier dynamics in silicon substrates in response to a large amplitude RF signal.

A convenient way of rewriting **Equation 3.39**, using **Equations 3.22-3.25**, is the following **[111, 112]**:

$$\frac{\partial n_t}{\partial t} = \left(\frac{n}{\tau_n} - \frac{n_t}{\tau_n^{'}}\right) - \left(\frac{p}{\tau_p} - \frac{p_t}{\tau_p^{'}}\right) \qquad [\mathrm{cm}^{-3}\cdot\mathrm{s}^{-1}] \qquad \textbf{(3.40)}$$

where the following parameters have been developed:

$$\tau_n^{'} = (\sigma_n v_n n_1)^{-1} \qquad [\mathrm{s}] \qquad \textbf{(3.41)}$$

$$\tau_p^{'} = (\sigma_p v_p p_1)^{-1} \qquad [\mathrm{s}] \qquad \textbf{(3.42)}$$

$$n_1 = N_C \cdot \exp\{(E_t - E_C)/kT\} \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.43)}$$

$$p_1 = N_V \cdot \exp\{(E_V - E_t)/kT\} \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.44)}$$

In this formulation, parameters n_1 and p_1 contain information about the trap energy position E_t. n_1 (p_1) is the density of free electrons (holes) in the conduction (valence) band when the Fermi level falls at E_t.

It is shown that the lifetime parameters τ_n, τ_p, τ_{tn}, τ_{tp} (see **Equations 3.15, 3.16, 3.20 and 3.21**), $\tau_n^{'}$ and $\tau_p^{'}$ depend on the carrier concentrations and on the trap occupancy. This makes response times tricky to analyze analytically[8].

[8] In **Section 3.4.3** we shall see how a *steady-state* approximation can be useful in determining analytically the thermal generation time constants, at least to the first order, in the context of non-equilibrium transient voltage simulations.

3.2.2 Typical Trap Distributions in Polysilicon

The trap characteristics of polysilicon are of particular interest in this work, towards the small- and large-signal modelling of trap-rich RF substrates.

It is generally accepted that polysilicon presents a continuous distribution of trapping states over its band gap, made up of a combination of exponentially decaying *Tail* distributions and of *Gaussian* distributions close to mid-gap [61, 62, 113–117]. These distribution functions are given by Equations 3.45 to 3.48, and are graphically represented in Figure 3.2. Acceptor and donor type traps are considered with both Tail and Gaussian distributions:

$$g_{GA}(E) = NGA \cdot \exp\left\{-\left(\frac{EGA - E}{WGA}\right)^2\right\} \qquad [\mathrm{cm}^{-3}\cdot\mathrm{eV}^{-1}] \qquad (3.45)$$

$$g_{GD}(E) = NGD \cdot \exp\left\{-\left(\frac{EGD - E}{WGD}\right)^2\right\} \qquad [\mathrm{cm}^{-3}\cdot\mathrm{eV}^{-1}] \qquad (3.46)$$

$$g_{TA}(E) = NTA \cdot \exp\left\{\frac{E - E_C}{WTA}\right\} \qquad [\mathrm{cm}^{-3}\cdot\mathrm{eV}^{-1}] \qquad (3.47)$$

$$g_{TD}(E) = NTD \cdot \exp\left\{\frac{E_V - E}{WTD}\right\} \qquad [\mathrm{cm}^{-3}\cdot\mathrm{eV}^{-1}] \qquad (3.48)$$

The parameters of these equations are detailed in Table 3.2, and are also represented graphically in Figure 3.2. These equations describe four *species* of traps, where a species is defined as a set of traps that have the same capture cross-sections (regardless of the trap's energy)[9].

Each trap species will have its own quasi-Fermi trap level in a non-equilibrium situation, and therefore its own occupation function [109, 118]. For example, the quasi-Fermi trap levels $E_{QF_{GA}}$ and $E_{QF_{TA}}$ are in general different, and one may be used to analyze the occupation proportion of the $g_{GA}(E)$ distribution, while the other to analyze the occupation proportion of the $g_{TA}(E)$ distribution. This is because the dynamic trapping/detrapping of each species of traps is different, due to different capture cross-sections, i.e., there is a continuity equation (3.39) for each species governed by different trap/detrap rates[10].

[9] To be rigorously accurate, traps are part of the same species if they have the same ratio of σ_e/σ_h. In that case, they share the same quasi-Fermi level.

[10] Note that therefore, writing for example a total acceptor trap distribution profile as $g_{totA}(E) = g_{GA}(E) + g_{TA}(E)$ is in general not helpful outside of steady-state equilibrium.

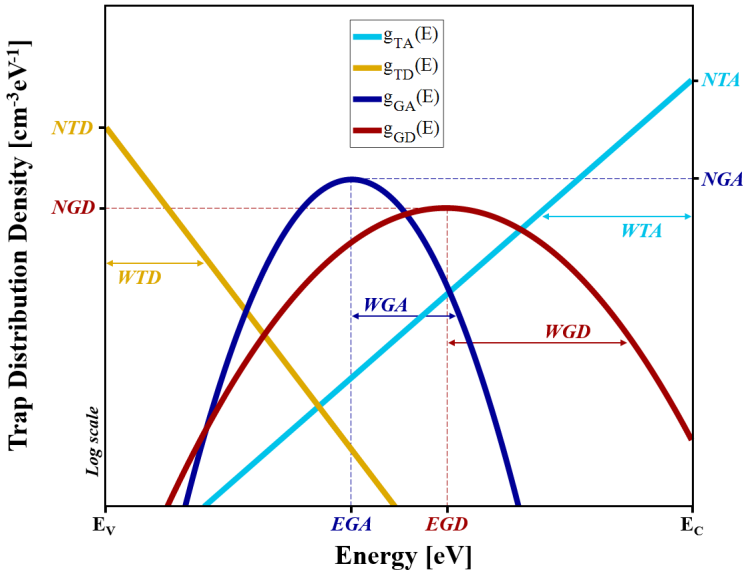


Figure 3.2: The four types of trap distributions considered for the modelling of polysilicon.

Values typically associated to *NTA* and *NTD* are usually in the range of 10^{20} to 10^{22} $cm^{-3}eV^{-1}$ for polysilicon **[61, 116]**, while *NGA* and *NGD* usual ranges are between 10^{15} and 10^{18} $cm^{-3}eV^{-1}$ **[61, 114–116]**.

Table 3.2 list the values of all parameters taken from **[61]**[11] to model polysilicon trap distributions according to **Equations 3.45 to 3.48**. **Table 3.3** gives the capture cross-sections for electrons and holes for the four considered families of traps **[61]**[11].

[11] In **[61]** see "TFT Example" in the DEFECTS statement section, page 1006.

Parameter	Description	Value	
NGA	Peak value of the Gaussian acceptor trap distribution $g_{GA}(E)$.	$1.5 \cdot 10^{15}$	cm^{-3}/eV
EGA	Energy position from the conduction band edge of the peak of the Gaussian acceptor trap distribution $g_{GA}(E)$.	0.62	eV
WGA	Characteristic decay energy of the Gaussian acceptor trap distribution $g_{GA}(E)$.	0.15	eV
NGD	Peak value of the Gaussian donor trap distribution $g_{GD}(E)$.	$1.5 \cdot 10^{15}$	cm^{-3}/eV
EGD	Energy position from the valence band edge of the peak of the Gaussian donor trap distribution $g_{GD}(E)$.	0.78	eV
WGD	Characteristic decay energy of the Gaussian donor trap distribution $g_{GD}(E)$.	0.15	eV
NTA	Value of the Tail acceptor trap distribution $g_{TA}(E)$ at the conduction band edge.	$1.0 \cdot 10^{21}$	cm^{-3}/eV
WTA	Characteristic decay energy of the Tail acceptor trap distribution $g_{TA}(E)$.	33	meV
NTD	Value of the Tail donor trap distribution $g_{TD}(E)$ at the valence band edge.	$1.0 \cdot 10^{21}$	cm^{-3}/eV
WTD	Characteristic decay energy of the Tail donor trap distribution $g_{TD}(E)$.	49	meV

Table 3.2: Typical tail and Gaussian trap distribution parameters associated with polysilicon, taken from **[61]**[11]. Refer to **Figure 3.2** that depicts graphically the meaning of these parameters.

Parameter	Description	Value
σ_{GAe}	Capture cross-section for electrons of the acceptor traps of the Gaussian distribution.	$2.0 \cdot 10^{-16}$ cm^2
σ_{GAh}	Capture cross-section for holes of the acceptor traps of the Gaussian distribution.	$2.0 \cdot 10^{-15}$ cm^2
σ_{GDe}	Capture cross-section for electrons of the donor traps of the Gaussian distribution.	$2.0 \cdot 10^{-15}$ cm^2
σ_{GDh}	Capture cross-section for holes of the donor traps of the Gaussian distribution.	$2.0 \cdot 10^{-16}$ cm^2
σ_{TAe}	Capture cross-section for electrons of the acceptor traps of the Tail distribution.	$1.0 \cdot 10^{-17}$ cm^2
σ_{TAh}	Capture cross-section for holes of the acceptor traps of the Tail distribution.	$1.0 \cdot 10^{-15}$ cm^2
σ_{TDe}	Capture cross-section for electrons of the donor traps of the Tail distribution.	$1.0 \cdot 10^{-15}$ cm^2
σ_{TDh}	Capture cross-section for holes of the donor traps of the Tail distribution.	$1.0 \cdot 10^{-17}$ cm^2

Table 3.3: Typical capture cross-sections of the tail and Gaussian type trap distribution associated with polysilicon, taken from **[61]**[11].

3.3 Charge Compensation in Semiconductor Substrates

3.3.1 Free Carriers, Ionized Traps and Fermi level Pinning

Traps can be leveraged to passivate SiO_2/Si interfaces that suffer from the Parasitic Surface Conduction (PSC) effect (see **Section 2.1** for more details). This is achieved by depositing a polysilicon layer between the oxide and the high-resistivity silicon substrate. Such a polysilicon layer is usually a few hundred nanometers to several microns thick and is characterized by a large number of defects or traps, hence its name: the polysilicon trap-rich layer.

As a reminder, the PSC effect is caused by fixed positive oxide charge Q_{ox} that induce strong band bending at the SiO_2/Si interface. The Fermi level at the interface is bent close to the conduction band edge, inducing many free electrons that compensate the oxide charge. The result is a highly conductive PSC sheet layer that is seen in parallel to the high resistivity bulk by coplanar circuits, and therefore counteract the highly resistive nominal properties of the substrate (see **Section 2.1**).

The working principle of the trap-rich layer is to provide a different charge compensation mechanism. Positive (negative) Q_{ox} charge must be compensated by negative (positive) charges in the semiconductor, but to maintain high resistivity it is desired that the compensating charge not be made up of free carriers that contribute to conduction. Instead, ionized traps balance the charge, preferably such that the interface Fermi level is deep in the band gap, so that the free carrier concentrations remain low, ensuring a state of high resistivity.

As an example, let us consider a MOS capacitor structure defined on a semiconductor material, that may in general include donor and acceptor trap distributions $g_D(E)$ and $g_A(E)$ defined within the bulk volume. Such a structure is illustrated in **Figure 3.3**.

The total charge applied to this structure $Q_{Applied}$ can be computed as:

$$Q_{Applied} = Q_{DC} + Q_{ox} - Q_{MS} \quad [\mathrm{C\cdot cm^{-2}}] \quad \textbf{(3.49)}$$

$$= (V_{DC} - \phi_s)\, C_{ox} + Q_{ox} - V_{MS} C_{ox} \quad [\mathrm{C\cdot cm^{-2}}] \quad \textbf{(3.50)}$$

where Q_{DC} is the charge density on the metallic top electrode induced by an applied DC voltage V_{DC} relative to the substrate, whose surface at the oxide interface is at the *surface potential* denoted by ϕ_s. The term $Q_{MS} = V_{MS} C_{ox}$ accounts for the charge induced by the difference between the work function of the metal and that of the semiconductor. $C_{ox} = \varepsilon_{ox}/t_{ox}$ is the normalized oxide capacitance per unit area, expressed in F/cm^2, with ε_{ox} and t_{ox} defined as the oxide permittivity and thickness, respectively.

At equilibrium, a compensation charge Q_{comp} will be induced in the substrate, to exactly counter-balance this applied charge:

$$Q_{comp} = -Q_{Applied} \qquad \text{at equilibrium} \qquad [\mathrm{C \cdot cm^{-2}}] \qquad \textbf{(3.51)}$$

Equation 3.50 can be solved to yield the *flatband voltage* V_{FB} of the structure. V_{FB} is defined as the applied V_{DC} that results in a total applied charge to the substrate $Q_{Applied}$ equal to zero. At flatband, the substrate is therefore not required to provide any compensation charge, and the Fermi level is flat as a function of depth in a usual MOS capacitor (hence the name of this voltage).

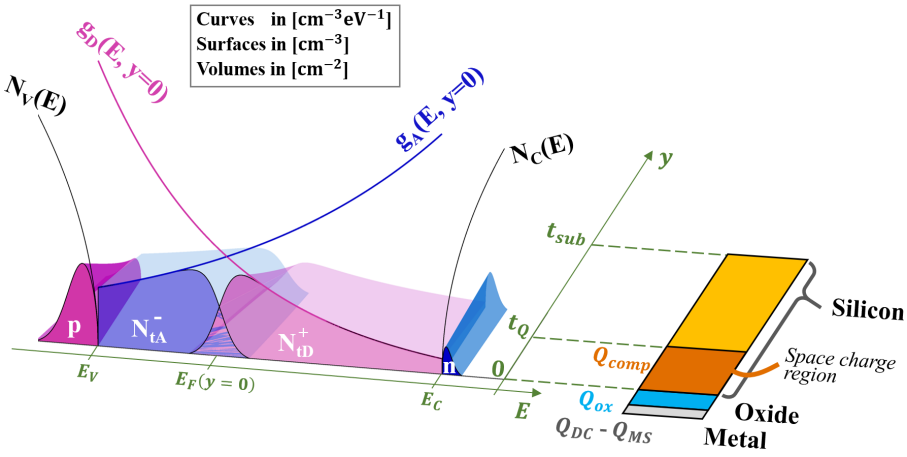


Figure 3.3: Graphical representation of charge density distributions, in energy and depth, in a general MOS capacitor structure on a semiconductor substrate including arbitrary trap distributions.

This compensation charge can be made of either free carriers, or of ionized trap centers. Using **Equations 3.3 to 3.5** we can write:

$$\begin{aligned} Q_{comp} &= \int_0^{t_Q} \rho_q \, dy \\ &= \int_0^{t_Q} Q_{free} \, dy \quad + \int_0^{t_Q} Q_{trap} \, dy \\ &= \int_0^{t_Q} q \cdot (p - n) \, dy \quad + \int_0^{t_Q} q \cdot \left(N_{tD}^{+} - N_{tA}^{-}\right) dy \\ &= Q_{free_{INT}} \quad + Q_{trap_{INT}} \qquad [\mathrm{C \cdot cm^{-2}}] \quad \textbf{(3.52)} \end{aligned}$$

where we have defined the free and trapped interfacial charge densities $Q_{free_{INT}}$ and $Q_{trap_{INT}}$ obtained by integrating over the *space charge depth* t_Q, to yield a charge density per unit interface area, expressed in units of $\mathrm{C}\cdot\mathrm{cm}^{-2}$.

Beyond the space charge region, there is no net charge[12]:

$$p(y) - n(y) + N_{tD}^{+}(y) - N_{tA}^{-}(y) = 0 \quad \text{for } y > t_Q \qquad [\mathrm{cm}^{-3}] \qquad \textbf{(3.53)}$$

Figure 3.3 graphically represents the key components of **Equation 3.52** for the case of a MOS capacitor defined on an arbitrary substrate that includes donor and acceptor trap distributions $g_D(E,y)$ and $g_A(E,y)$[13].

The distributions of energy states available to electrons, holes, ionized donor traps and ionized acceptor traps are $N_C(E)$, $N_V(E)$, $g_D(E)$ and $g_A(E)$, respectively. These four curves are plotted at the Si/SiO_2 interface in the $y = 0$ plane. Each of these curves is then multiplied by the occupation function[14] and integrated over energy. The resulting area plots in the $y = 0$ plane represent the charge densities n, p, N_{tA}^{-} and N_{tD}^{+} in cm^{-3} at the interface (see **Equations 3.6, 3.7, 3.11, 3.12**).

The interfacial trapped charge density $Q_{trap_{INT}}$ can be computed graphically as the difference between the purple and blue volumes situated between E_V and E_C and between $y = 0$ and $y = t_Q$.

Similarly, the interfacial free charge density $Q_{free_{INT}}$ can be computed graphically as the difference between the purple volume situated below E_V and below $y = t_Q$ and the blue volume situated above E_C and below $y = t_Q$.

In the example provided in this figure, the total positive substrate charge per cm^2 (pink volume) is larger than the total negative charge per cm^2 (blue volume) in the space charge region, because $Q_{Applied}$ is negative in this example.

[12] As a reminder, terms N_{tD}^{+} and N_{tA}^{-} include charge contributions from ionized dopants (that are shallow traps).

[13] In general, these distributions can be space dependent of the form $g(E,\bar{r})$. In real trap-rich substrates the polysilicon trap layer is uniform in the plane of the BOX/Si interface, but it may depend on depth as partial recrystallization is expected in polysilicon in contact with the crystalline bulk during high thermal budget processes.Then $g(E,y)$ is the appropriate dependency. In general, the polysilicon layer in a trap-rich substrate is a few microns thick at most.

[14] $N_C(E)$ and $g_A(E)$ are multiplied by $F(E)$, and $N_V(E)$ and $g_D(E)$ are multiplied by $(1 - F(E))$.

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Charge Compensation Analysis

Now, let us analyze the charge compensation mechanisms of a MOS capacitor in two distinct substrates of interest:

HR. A HR substrate, without any traps: $g_D(E) = g_A(E) = 0$.
TR. A TR substrate, with strong trap distributions $g_D(E)$ and $g_A(E)$.

For both substrates, we will consider two cases:

(1). A highly negative charge density $Q_{Applied-}$ is imposed.
(2). A highly positive charge density $Q_{Applied+}$ is imposed.

For any given case **(1)** or **(2)**, both substrates must provide the same compensation charge $Q_{comp} = Q_{free_{INT}} + Q_{trap_{INT}} = -Q_{Applied}$.

In case **(1)**, we denote as E_{F-} the position of the Fermi level at the Si/SiO_2 interface ($y = 0$). Please note that E_{F-} is different for the two considered substrates.

Then, **Figure 3.4 HR(1)** and **TR(1)** show the charge densities at the interface for both substrates, where the energy configuration is $E_F(y = 0) = E_{F-}$.

For the **HR** substrate, the compensation charge is entirely made up of the term $Q_{free_{INT}}$. Therefore, in order to compensate the highly negative applied charge $Q_{Applied-}$, the Fermi level has moved close to the valence band edge, and a large free hole concentration p (purple area) is induced at the interface to provide the compensation.

For the **TR** substrate, trapped charge also contributes to Q_{comp}. **Figure 3.4 TR(1)** highlights this, where large valued functions $g_D(E)$ and $g_A(E)$ have been introduced. One can see that the charge balance is mainly provided by the ionized trap densities N_{tA}^- and N_{tD}^+ (blue and purple areas in the band gap, respectively). Free carrier densities n and p are inevitably present, but are in negligible quantity compared to the ionized trap terms in **TR** substrates. This is because many deep-level traps close to the interface provide the necessary compensation charge and maintain the Fermi level deep in the band gap.

Note that in response to the negative $Q_{Applied-}$, both **HR(1)** substrate and the **TR(1)** substrate must provide the same net positive compensation charge Q_{comp}. The net charge density at the interface ($y = 0$) can be calculated graphically as the difference between the total purple area and the total blue area: $p + N_{tD}^+ - (n + N_{tA}^-)$.

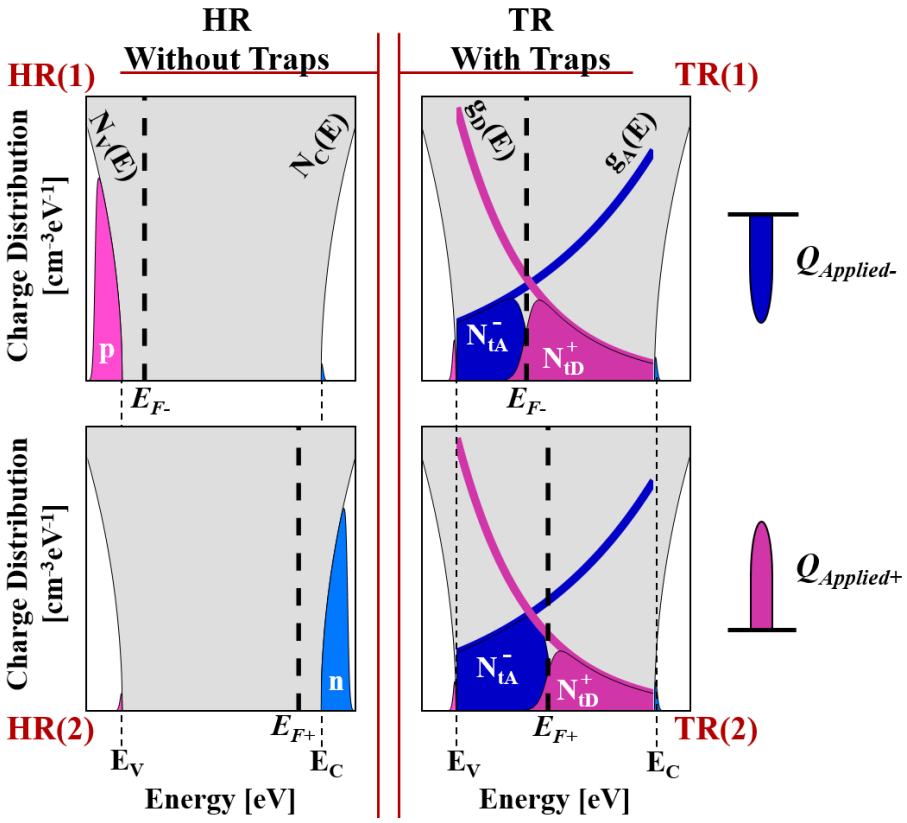


Figure 3.4: Example of trap occupancy and free carrier density variation at the surface in response to a shift in the Fermi level from E_{F-} to E_{F+}. **HR(1)** and **TR(1)** Initial configuration at E_{F-}. **HR(2)** and **TR(2)** Second configuration at E_{F+} after some band bending has occurred due to some introduced positive charge (applied positive bias for example).

In case **(2)**, we denote as E_{F+} the position of the Fermi level at the Si/SiO_2 interface. E_{F+} is different for the two considered substrates.

For the **HR** substrate the Fermi level has moved close to the conduction band edge, and a large free electron concentration n (blue area) is induced at the interface to provide the compensation.

For the **TR** substrate, a Fermi level E_{F+} that is situated deep in the band gap is able to provide a charge configuration that compensates $Q_{Applied+}$. And so once again, free carrier densities (that contribute to $Q_{free_{INT}}$) are in negligible

quantity.

In terms of RF substrate performance, with low values of Q_{free} comes high effective substrate resistivity and strong substrate linearity. For TR substrates, Q_{free} remains low for usual values of $Q_{Applied}$[15], meaning that TR's RF performance depends little on the DC bias voltage or on the RF signal's amplitude.

To sum up, we can say that a charge $Q_{Applied}$ introduced to the system must be compensated for by an induced charge $Q_{comp} = Q_{free_{INT}} + Q_{trap_{INT}}$, that can be made up of a combination of free carriers and of ionized traps[16].

In **HR** substrates, Q_{free} is the dominating (only) compensation mechanism, requiring large swings in E_F and allowing for large swings in n and p, from strong accumulation to strong inversion. This allows the substrate interface to be in highly conductive states and the substrate to be lossy. Furthermore, a time varying RF signal on such substrates will induce applied charge variations $\Delta Q_{Applied}$, that will strongly influence the substrate's electrical parameters. Strong variations in substrate conductance and capacitance flow from strong variations in free carrier densities n and p that determine substrate impedance, rendering HR substrates highly non-linear.

In **TR** substrates, Q_{trap} is the dominating compensation mechanism. In response to a time varying $\Delta Q_{Applied}$, compensation is achieved with only a small variation in E_F deep in the band gap that produces large variations in N_{tD}^{+} and N_{tA}^{-}. Therefore, large values of the free carrier densities n and p are avoided. The Fermi level at the interface is said to be *deeply pinned*, locking the interface in a state of high resistivity, with little dependency on the $Q_{Applied}$. Therefore, TR substrates present low-loss and are highly linear[17].

[15] By *usual values* of $Q_{Applied}$ it is meant charge densities that will typically be encountered in this thesis. For example the charge density originating from a few volts on a MOS capacitor's electrode with and oxide thickness in the range of 1 micron. And/or originating from fixed oxide charge densities at Si/SiO_2 interfaces in the range of 10^{11} cm^{-2}.

[16] Let's remind ourselves here one last time that ionized dopants are incorporated into the $Q_{trap_{INT}}$ term.

[17] This discussion holds true in the framework of a DC analysis, but for AC and RF signals, the response times available to the compensation charge terms Q_{free} and Q_{trap} must be accounted for. These dynamic considerations will be tackled further on in this work in **Section 3.4**.

In some substrates, neither charge compensation (free carriers or traps) is really dominant, but rather both types of mechanism play an important role. This is the case in gold-doped substrates, developed for high RF performance, that will be presented and discussed in **Section 8.4**

Summary of charge compensation mechanisms in silicon-based substrates in response to an increase in positive charge $+\Delta Q_{Applied}$ (voltage on electrode or fixed interface charges for example):

- n ↗
- p ↘

} Dominant (only) charge compensation mechanism in HR substrates.
Large swings in E_F.

- N_{tA}^{-} ↗
- N_{tD}^{+} ↘

} Dominant charge compensation mechanism in TR substrates.
Fundamentals of Fermi level pinning.

It is important to note here already that when considering high-frequency large-amplitude signals, the substrate will generally be out of equilibrium as electron capture and emission processes to and from trapped states and/or the valence and conduction bands have finite response times. In this case, **Equation 3.51** no longer holds true. This will be discussed in **Section 3.4**.

3.3.2 Impact of the Trap-Rich Layer on RF Substrate Performance

To evaluate the impact of a trap-rich layer on the RF substrate performances, TCAD simulations were run on a CPW line structure[18]. With reference to **Figure 3.5**, the physical parameters of the structure are:

- Metal thickness of the CPW line $t_{metal} = 1$ µm.
  - Aluminum, with metal work function $\phi_M = 4.1$ eV.
  - The CPW dimensions are defined as $W_C = 26$ µm, $S = 12$ µm, and $W_G = 208$ µm.
- Oxide thickness $t_{ox} = 400$ nm.
  - With interfacial charge density $N_{ox} = Q_{ox}/q = +10^{11}$ cm^{-2}.
- Polysilicon thickness $t_{poly} = 1$ µm using tail distributions $g_{TA}(E)$ and $g_{TD}(E)$, described by **Equations 3.47** and **3.48**.
  - The characteristic energies WTA and WTD were set to 40 meV.
  - The density parameters NTA and NTD are set as a simulation variable.
  - Background doping and type the same as the handle substrate ($N_A = 2.8 \cdot 10^{12}$ cm^{-3}).
- Silicon substrate thickness $t_{sub} = 500$ µm.
  - P-type and of nominal resistivity $\rho_{nom} = 5$ kΩcm ($N_A = 2.8 \cdot 10^{12}$ cm^{-3}).

Based on this CPW device, substrate performances were simulated for a range of trap densities $NTA = NTD = NT$, from 10^{16} to 10^{22} cm^{-3}eV^{-1}, and are presented in **Figure 3.6**[19].

Below NT of 10^{18} cm^{-3}eV^{-1} the traps are in negligible quantity and the substrate can be considered as a HR. In that case, **Figure 3.6 (a)** shows that the Fermi level at the SiO_2 interface is close to the conduction band, at around $E_V + 0.87$ eV. As a consequence, a parasitic surface conduction layer made

[18] Atlas from Silvaco was used. The small-signal simulation of a CPW line using this tool was described in **Section 2.1.3**.

[19] These values for NT may seem quite large, but actually the following few calculations will show that they are reasonable for $WTA = WTD = 40$ meV. Indeed, for $NT = 10^{22}$ cm^{-3}eV^{-1}, the overall density of trap states from 0.15 eV above the valence band edge to 0.15 eV below the conduction band edge is $\int_{E_V+0.15}^{E_C-0.15} g_{A/D}(E)\, dE = 9.4 \cdot 10^{18}$ cm^{-3}. The reader should keep in mind that NTA and NTD simply represent the maximum values of the $g_A(E)$ and $g_D(E)$ distributions. These maximum points are defined at the band edges, as illustrated in **Figure 3.2**, but these edge states are never filled as the Fermi level never bends that far, especially in such trap-rich substrates, where it is confined close to midgap.

up of many electrons is present at the interface, which translates into a low effective resistivity and high levels of harmonics as shown in **Figure 3.6 (c)** and **(d)**.

From this point onward in this chapter, simulated large-signal distortion results will be presented to help illustrate and understand some key physical mechanisms and parameter impact on substrate linearity performance. We point out that the modelling of the substrate-induced harmonic distortion is not detailed at this stage of the text, but rather the modelling approach will be described in **Chapter 4**, and model validation is reserved for **Chapter 5**.

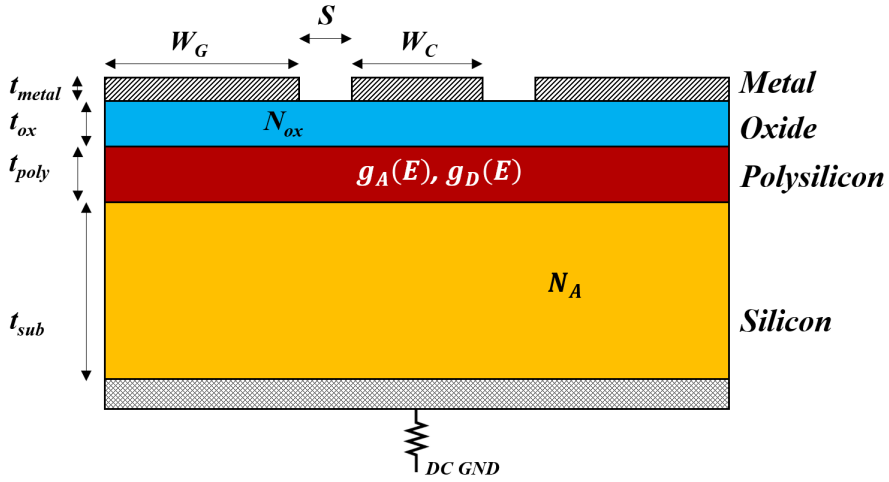


Figure 3.5: Cross-section of the simulated CPW structure on silicon-based substrates. The silicon bulk is DC grounded and RF floating.

Figure 3.6 (b) plots the net interfacial density of free carriers $N_{free_{INT}}$ and the net interfacial density of trapped charges $N_{trap_{INT}}$ directly beneath the signal line of the simulated CPW structure. They are defined as:

$$N_{free_{INT}} = Q_{free_{INT}}/q \triangleq \int_0^{t_{poly}} p(\bar{r}) - n(\bar{r})\, dy \qquad [\mathrm{cm}^{-2}] \qquad \textbf{(3.54)}$$

$$N_{trap_{INT}} = Q_{trap_{INT}}/q \triangleq \int_0^{t_{poly}} N_{tD}^{+}(\bar{r}) - N_{tA}^{-}(\bar{r})\, dy \qquad [\mathrm{cm}^{-2}] \qquad \textbf{(3.55)}$$

$N_{free_{INT}}$ and $N_{trap_{INT}}$ are expressed in units of cm^{-2}, and, at equilibrium,

can be directly compared to $N_{Applied}$. We can write[20]:

$$N_{comp} = N_{free_{INT}} + N_{trap_{INT}} \approx -N_{Applied} \quad [\text{cm}^{-2}] \quad \textbf{(3.56)}$$

$$N_{Applied} = Q_{Applied}/q = N_{ox} + C_{ox}\left(V_{DC} - \phi_s - V_{MS}\right)/q \quad [\text{cm}^{-2}] \quad \textbf{(3.57)}$$

To illustrate the equality of **Equation 3.56**, **Figure 3.6 (b)** plots an approximate evaluation of $-N_{Applied}$ using **Equation 3.57** in which ϕ_s was considered to be zero[21]. The calculations of the different elements of **Equation 3.57** needed to evaluate $-N_{Applied}$ are detailed here below.

V_{MS} can be computed as **[119]**:

$$\begin{aligned}\Phi_{MS} = \Phi_M - \Phi_S &= \Phi_M - \chi - \frac{E_g}{2q} - kT\ln\left(\frac{N_A}{n_i}\right) \\ &= 4.1 - 4.05 - 0.56 - 0.026\ln\left(\frac{2.8\cdot 10^{12}}{1.2\cdot 10^{10}}\right) \\ &= -0.65 \quad [\text{eV}] \quad \textbf{(3.58)} \\ V_{MS} = \Phi_{MS}/q &= -0.65 \quad [\text{V}] \quad \textbf{(3.59)}\end{aligned}$$

where Φ_M and Φ_S are the metal and semiconductor work functions, respectively. χ and E_g are respectively the electron affinity of the semiconductor and the band gap energy. The last term is the bulk potential[22], that is calculated based on the thermal energy kT, the bulk doping level N_A, and the intrinsic carrier concentration n_i.

[20] The second equality of **Equation 3.56** is an approximation as finite integration boundaries were used to calculate the substrate charge, and ionized dopants in depletion regions below the depth t_{poly} are not accounted for. This leads to a small error in the total charge, that is acceptable in the context of the present example to explain the physical mechanisms at play. Indeed, the dashed blue line of **Figure 3.6 (b)** shows that in our present case this equation holds approximately true.

[21] This approximation holds relatively well for large values of NT on resistive substrates, as the interface Fermi-level and the bulk Fermi-level are both relatively deep in the band gap in that case. In general, ϕ_s is different for each simulated substrate, i.e. for each value of NTn and therefore the exact $-N_{Applied}$ curve is not flat as depicted in **(b)**. For the purpose of explaining the different charge compensation mechanisms in the substrate, the use of this approximation is acceptable.

[22] For an N-type substrate, the term $-kT\ln\left(\frac{N_A}{n_i}\right)$ is replaced by $+kT\ln\left(\frac{N_D}{n_i}\right)$.

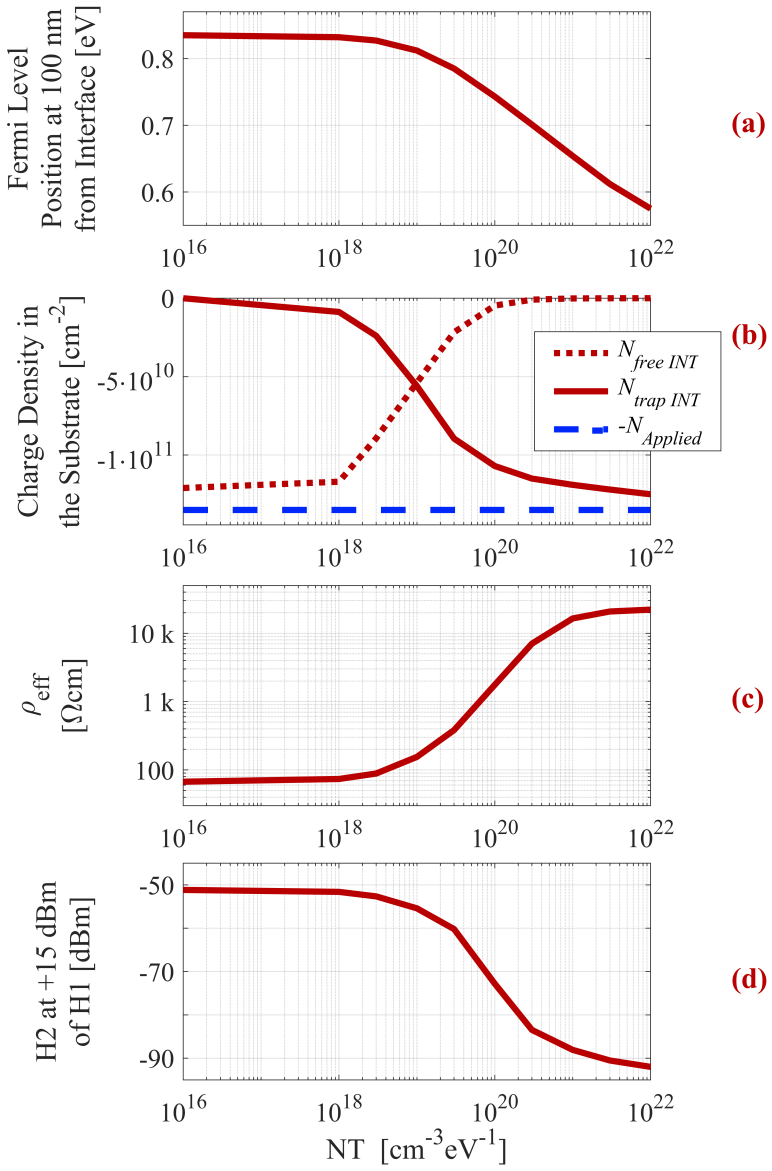


Figure 3.6: Simulated electrical parameters of a CPW line on a trap-rich substrate as a function of trap density NT in the polysilicon passivation layer. The applied DC bias is zero Volts. **(a)** Position of the Fermi level at 100 nm below the oxide layer. **(b)** Interfacial densities of free charge and trapped charge. **(c)** Effective resistivity, extracted above slow-wave mode (> 10 GHz, as discussed in **Section 2.1.2**). **(d)**. Second harmonic level for +15 dBm of output fundamental.

Therefore, at zero DC bias (and considering $\phi_s = 0$ V[21]), we have:

$$\begin{aligned} N_{comp} &\approx -N_{Applied} \\ &= -N_{ox} \quad - C_{ox}\big(0 - -0V_{MS}\big)/q \\ &= -1\cdot 10^{11} - 3.5\cdot 10^{10} = -1.35\cdot 10^{11} \qquad [\text{cm}^{-2}] \end{aligned} \tag{3.60}$$

The dashed blue line in **Figure 3.6 (b)** plots $-N_{Applied}$, and one can observe that the sum of the two curves $N_{free_{INT}}$ and $N_{trap_{INT}}$ approximately equals this value, for all simulated substrates, as expressed by **Equation 3.56**[20].

As the trap density NT is increased in the polysilicon layer, the traps contribute more strongly ($N_{trap_{INT}}$ $\nearrow$) to the compensation of $N_{Applied}$. The Fermi level moves deeper into the band gap (**Figure 3.6 (a)**) and the free carriers contribute less ($N_{free_{INT}}$ $\searrow$). The interface becomes more resistive, and the PSC layer weakens in conductance, which translates into a higher effective resistivity, as illustrated by **Figure 3.6 (c)**. Higher effective resistivity in itself is a source of reduction in harmonic distortion levels **[98]**. On top of this, the traps also limit the Fermi level variation, i.e. the substrate's voltage sensitivity that is concomitant with non-linearity, in response to a large-signal excitation, reducing the HD levels, as can be seen in **Figure 3.6 (d)**. These are two mechanisms by which the traps improve substrate linearity.

When NT increases above the range of $1\cdot 10^{20}$ cm^{-3}eV^{-1}, the polysilicon can really be considered as an effective trap-rich layer for RF applications, as ρ_{eff} increases above 2 kΩcm and the second harmonic $H2$ decreases below -80 dBm[23].

Notice how the total amount of trapped charge $N_{trap_{INT}}$ converges toward $-N_{Applied} = -1.35\cdot 10^{11}$ cm^{-2} as NT increases, to compensate almost entirely the applied charge. When NT is low, it can be seen that $N_{free_{INT}}$ provides entirely this compensation charge $-N_{Applied}$.

The substrate for which $NT = 1\cdot 10^{19}$ cm^{-3}eV^{-1} is quite interesting to analyze. We observe that about half of the compensation is provided by free carriers, and the other half by ionized traps. For this substrate the PSC layer is still present, and it's conductance is roughly halved (compared to the case when $NT < 1\cdot 10^{18}$) thanks to the traps providing partial compensation. Then, it is worth noting that the effective resistivity is approximately doubled. Indeed,

[23]The simulated CPW line is the reference structure (in terms of all of its dimensions) used for the RF performance evaluation of commercial RF substrates. A value of -80 dBm at +15 dBm input power corresponds to the linearity quality of the eSI80^{TM} trap-rich SOI wafers from Soitec (see RFeSI^{TM} samples presented in **Figure 2.12** of **Section 2.4**).

$\rho_{eff}(NT < 1 \cdot 10^{18})$ = 75 Ωcm while $\rho_{eff}(NT = 1 \cdot 10^{19})$ = 153 Ωcm, which of course makes sense, as the PSC layer is mainly determining the value of ρ_{eff} (above the slow-wave mode).

All of the results presented in **Figure 3.6** were obtained without applying any net DC voltage between the CPW test structure and the semiconductor substrate. A DC bias will strongly affect the behavior of semiconductor substrates, by significantly contributing to $N_{Applied}$, as described by **Equation 3.57**.

Figure 3.7 then analyzes the substrate's small- and large-signal RF behavior as a function of varying DC bias voltage. This voltage is applied to the signal line relative to the two ground lines of the CPW. The substrate is also DC grounded (to the same potential as the CPW's ground lines) through a large bias resistor, and is therefore RF floating. This biasing situation is close to the set-up used during on-wafer RF measurements[24].

[24]Though comparison to measurements is reserved for **Chapter 5** for model validation, the attentive reader may remember the experimental data presented in **Figure 2.14 (b)** in **Chapter 2**, that plotted $H2$ against V_{DC} of a few reference silicon substrate samples. Comparing these to the simulation results of **Figure 3.7 (d)** shows already that both HR and TR trends can be well reproduced by the model.

Figure 3.7 (a) shows that, as the trap density NT increases, the interface Fermi level position becomes more tightly pinned. This translates into a smaller variation of $N_{free_{INT}}$ as a function of the line voltage. Ultimately, this leads to lower levels of harmonic distortion.

For the case of a very large value of $NT = 1 \cdot 10^{22}$ cm^{-3}eV^{-1}, the substrate's electrical performances ρ_{eff} and $H2$ have almost no bias dependency, and this is explained by the very tight Fermi level pinning.

It is also worth pointing out that the sum of the curves $N_{free_{INT}}(V_{DC})$ and $N_{trap_{INT}}(V_{DC})$ of **Figure 3.7 (b)** gives the unique curve $-N_{Applied}(V_{DC})$, that is common to all substrates (any NT, and under the approximation that $\phi_s = 0$ V[21]) and is calculated according to **Equation 3.57** plotted as the dashed blue line **Figure 3.7 (b)**.

Figures 3.6 and 3.7 give physical insight into the inner workings of HR and TR substrates, and illustrate the link between the semiconductor physics and the RF performance metrics. Further comments on the results presented are reserved for **Chapters 4 and 5**[25].

[25] Such as commenting on the characteristic dip in the HD curves at zero DC bias, that will be discussed in **Section 5.2.2**.

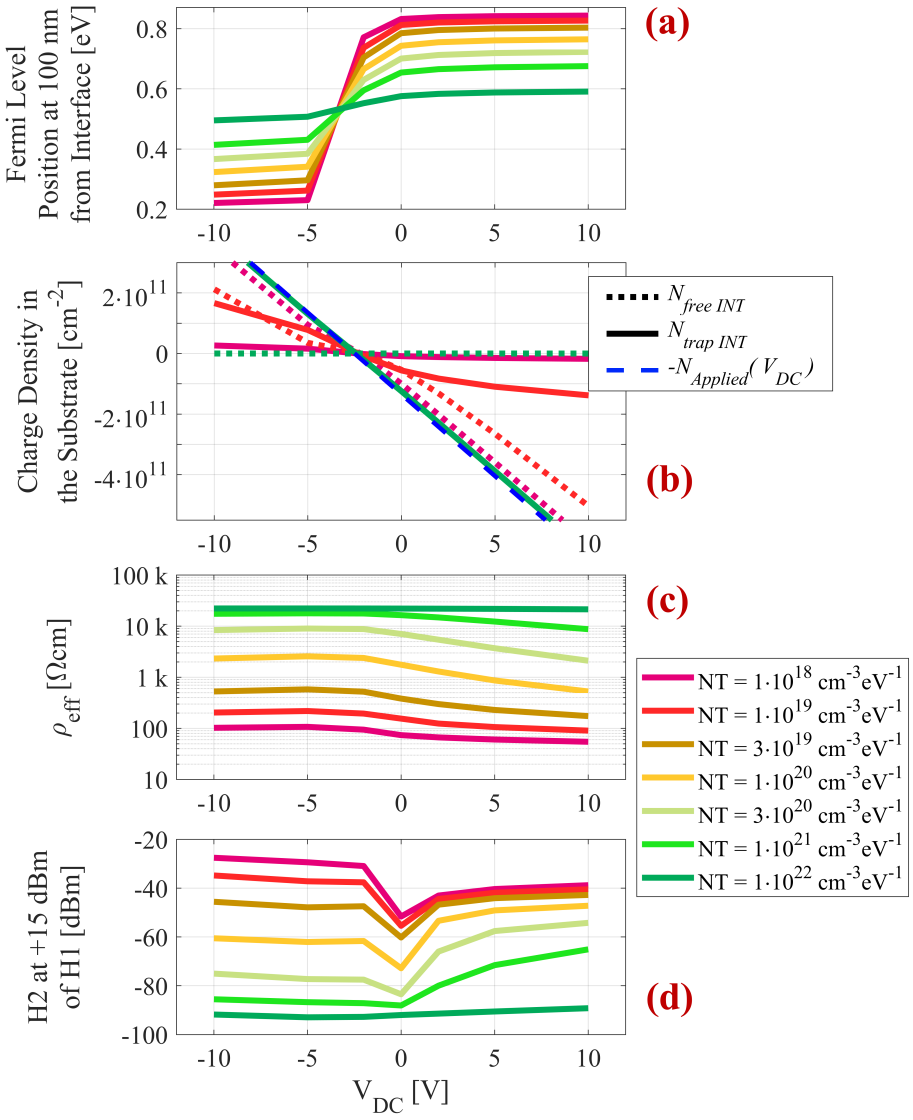


Figure 3.7: Simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC}, for several trap-rich substrates with various trap-densities NT. **(a)** Position of the Fermi level at 100 nm below the oxide layer. **(b)** Interfacial densities of free charge and trapped charge. **(c)** Effective resistivity, extracted above slow-wave mode (> 10 GHz, as discussed in **Section 2.1.2**). **(d)** Second harmonic level for +15 dBm of output fundamental.

3.4 Non-Equilibrium Dynamics

So far, all of the above discussion has been in the framework of semiconductor materials that have reached equilibrium. In particular, all curves from all substrates of **Figure 3.6 (a), (b) and (c)** and **Figure 3.7 (a), (b) and (c)** are at equilibrium.

However, carriers and traps have finite response times, and equilibrium concentrations take time to be reached. This means that in response to a time varying voltage signal, the equilibrium compensation charge in the substrate may not have time to establish itself, and this is particularly the case when considering large-amplitude and high-frequency signals. In general, under such conditions, **Equation 3.51** (**pg. 83**) does not hold true.

To illustrate this finite response time, the CPW structure of **Figure 3.5** (**pg. 91**) is analyzed in a transient time domain simulation. The material substrate parameters are:

- Metal work function of 4.1 eV for the central line of the CPW.
- Neutral electrodes for the ground lines of the CPW.
- Oxide thickness of 400 nm.
- Interfacial oxide charge density N_{ox}, set to 0 or 10^{11} cm^{-2}.
- P-type silicon substrate of nominal resistivity ρ_{Si} (variable), and without any trap-rich layer.
- A single recombination center situated at mid gap, and present in a uniform density of 10^{14} cm^{-3} over the entire silicon substrate.

A transient voltage signal is applied on the central CPW electrode, with the substrate potential set to the reference value of 0 V. Neutral electrodes at 0 V are defined for the two ground lines of the CPW[26]. The applied voltage signal is initially at -10 V, and the substrate's initial equilibrium condition below the CPW central line is therefore an accumulation state. The line voltage is then ramped to +10 V with a 1 ps step time.

An analysis is then made on the carrier response times in the substrate by looking at the evolution of the free interfacial charge densities, defined over a

[26] Therefore, there are no reservoirs of electrons in the system. If we had also set these electrodes to have a 4.1 eV metal work function, an inversion layer would be induced below the 400 nm oxide, and these reservoirs, though 12 µm away from the central CPW line, contribute significantly to minority carrier response time.

1 µm depth as:

$$p_{INT} \triangleq \int_0^{1\,\mu m} p(\bar{r})\, dy \qquad [\mathrm{cm}^{-2}] \qquad \textbf{(3.61)}$$

$$n_{INT} \triangleq \int_0^{1\,\mu m} n(\bar{r})\, dy \qquad [\mathrm{cm}^{-2}] \qquad \textbf{(3.62)}$$

$$N_{free_{INT}} = p_{INT} - n_{INT} \qquad [\mathrm{cm}^{-2}] \qquad \textbf{(3.63)}$$

3.4.1 Response Time Analysis Without Fixed Oxide Charge

Figure 3.8 (a) and (b) then plot the evolution of the interfacial carrier concentrations over time below the signal line $p_{INT}(t)$, $n_{INT}(t)$ and $N_{free_{INT}}(t)$, considering a range of bulk P-type substrate resistivities, and without any fixed oxide charge density: $N_{ox} = 0\ \mathrm{cm}^{-2}$.

The introduced voltage step pulses the structure from a state of strong accumulation to a state of strong inversion, meaning that the large interfacial hole density p_{INT} must be repelled, and a large interfacial electron density n_{INT} must be induced.

It is important to note that the total number of electrons and holes in the system is very different at $t = +\infty$ than at $t = 0$, before and after the voltage step is applied. To reach final equilibrium, free carriers must therefore be generated and recombined.

However, the existing carriers in the substrate may spatially rearrange themselves in response to the voltage step, to minimize the global non-equilibrium as best they can while waiting for thermal generation/recombination of carriers to provide total equilibrium.

Mathematically, one is to understand from **Equations 3.31 and 3.32** that $\partial n/\partial t$ and $\partial p/\partial t$ vary first due to drift and diffusion, and it is only after a longer time period that terms U_n and U_p significantly contribute.

In the present simulations, a single trapping center is defined at mid gap and governs the Shockley-Read-Hall (SRH) generation/recombination rates. Due to the introduced potential energy, with reference to **Figure 3.1 (a)**, rates r_b and r_c become larger than rates r_a and r_d, respectively. Therefore, a net recombination of holes takes place ($U_p > 0$), along with a net generation of electrons ($U_n < 0$)[27]. This process kicks in as soon as the potential energy changes, so starting from 1 ps, though its contribution to $N_{free_{INT}}(t)$ remains small up until a time of approximately τ_{th}, as shown in **Figure 3.8 (b)**.

[27] See **Equations 3.33 and 3.34**.

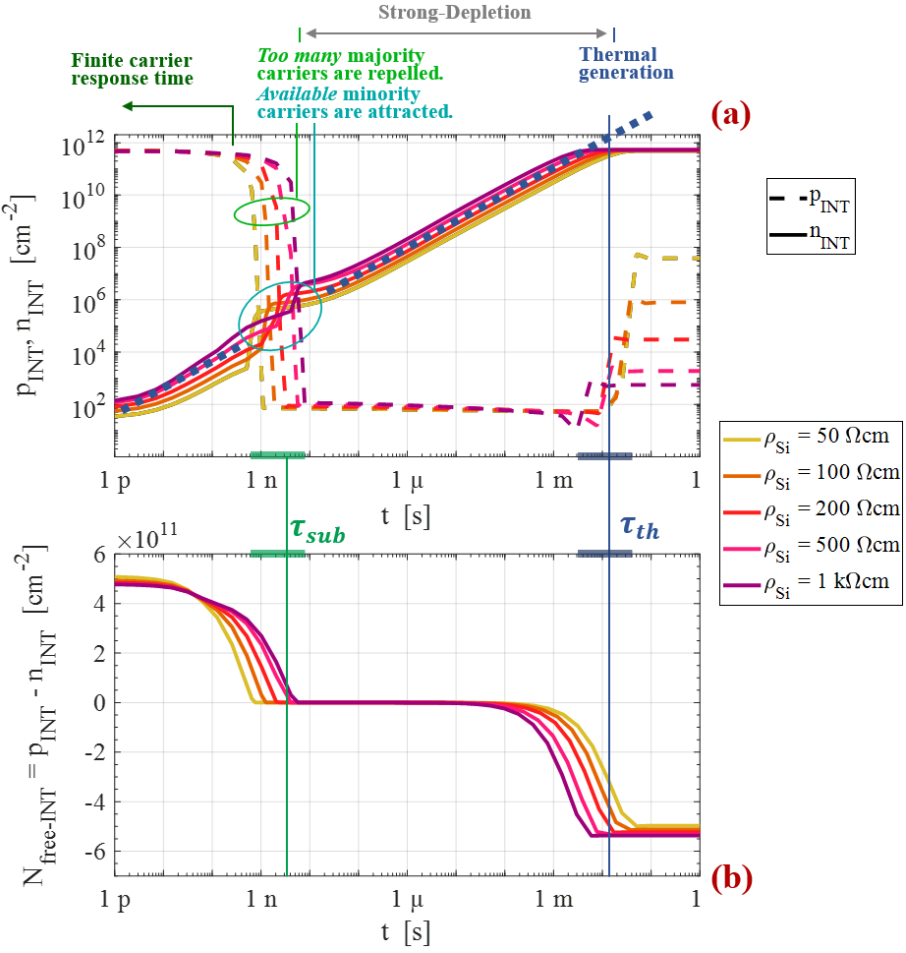


Figure 3.8: Simulations of the evolution over time of interfacial free carrier densities in P-type substrates in response to a transient voltage pulse from -10 V (strong accumulation) to +10 V (strong inversion) with a 1 ps ramp time. No oxide charges are present at the Si/SiO_2 interface $N_{ox} = 0$ cm^{-2}.

This thermal process is approximately a linear function of time, with a slope that is determined by the net generation/recombination rates U_n and U_p. For the present SRH parameters, this gives rise to a thermal equilibrium time τ_{th} in the range of 1-10 ms. This value will be justified based on our SRH parameters in **Section 3.4.3**. Please note that this time is a function of the applied voltage

step amplitude, as it depends on the total amount of carriers that need to be generated an recombined to reach equilibrium. For example, if we had not stepped to a value of +10 V, but to instead +5 V or +50 V, the final equilibrium time τ_{th} would be shifted by a significant factor[28].

Figure 3.8 (a) shows that thermal generation starts immediately, and a dashed blue line is plotted to highlight this mechanism and its response time.

Before final equilibrium is achieved through thermal generation after 1-10 ms, carriers undergo a rearrangement process within the silicon. However, carriers have finite inertia, and cannot respond instantaneously. **Figure 3.8 (a)** shows that the majority carriers in the accumulation layer respond in a finite time τ_{sub}, that is of the order of 1-10 ns. This time constant is the *dielectric relaxation time* of the substrate, and is given by:

$$\tau_{sub} = 2\pi\rho_{Si}\varepsilon_{Si} \qquad [s] \qquad \textbf{(3.64)}$$

For the considered silicon substrates of our study, this characteristic time depends on the bulk nominal resistivity. For the 1 kΩcm and 50 Ωcm substrates, τ_{sub} is 6.5 ns and 320 ps, respectively, and these values agree well with the observable response times from the TCAD results.

τ_{sub} represents the time needed to repel the accumulation layer from the interface and into the substrate (more physical meaning of τ_{sub} is given in **Section 3.4.4**). At the same time as the accumulation layer is repelled, *available* minority carriers from other parts of the substrate are also attracted, with a similar time constant related to their finite inertia through the substrate. Using the TCAD, we can analyze the evolution of carrier densities in the substrate regions below the interface layer pertaining to $p_{INT}(t)$ and $n_{INT}(t)$ (defined from 0 to 1 µm). That data (results not shown) reveals that at the same time as the step increase in $n_{INT}(t)$ occurs at time τ_{sub}, a step decrease occurs in the free electron density in the layer below, confirming that this step increase at the interface is associated to *available* minority carriers flooding to the interface from nearby substrate regions.

Between times τ_{sub} and τ_{th}, we say that the interface region is in a state of *strong-depletion*, and that the silicon below this interface is in a state of *deep-depletion*.

[28] Furthermore, τ_{th} depends heavily on the silicon substrate sample's trap distributions, and may have a value orders of magnitude higher or lower than 1-10 ms. However, it is reasonable to assume that RF signals will always have much shorter time periods than τ_{th}, and so, in the broader context of the goal of this thesis, which focuses mainly on RF signals, the exact value of τ_{th} is not critical, as long as it is significantly larger than 1 ns, which is a reasonable assumption.

- The notion of *strong-depletion* is used to describe the interface at all times t_x for which $N_{free_{INT}}(t_x) \ll N_{free_{INT}}(t = +\infty)$. This is well highlighted in **Figure 3.8**, and it is shown that the interface is *strongly-depleted* from τ_{sub} to τ_{th} approximately.
- The notion of *deep-depletion* is used here to characterize the extent of the space charge region into the substrate. Indeed, the non-equilibrium depletion region is *deeper* than the final equilibrium depletion layer. Physically, this is so that a large space charge region in depletion, negatively charged due to the ionized acceptor dopants, provides some charge compensation to the applied +10 V, while free electrons are thermally generated.

It is noteworthy to point out that *too many holes* are repelled from the interface, in the sense that the free hole density at the interface, from τ_{sub} to τ_{th}, is lower than the final equilibrium value that will be reached at $t = +\infty$, and we have $n \cdot p \ll n_i^2$ in the non-equilibrium depletion region.

Once the time gets close to τ_{th}, and almost enough electrons have been thermally generated, holes then also undergo generation processes[29,30].

[29] In a given region, each generated electron also generates a hole. Note that these processes do not occur solely at the interface region under consideration, and that the generated electrons and/or holes in any semiconductor region of the structure may drift or diffuse to another region. There is a net transient current from the electrodes of the structure to account for variation over time of the total number of electrons and holes in the system.

[30] It is worth noting that in fact around τ_{th}, both the electron density $n_{INT}(t \approx \tau_{th})$ and the hole density $p_{INT}(t \approx \tau_{th})$ slightly overshoot the equilibrium densities $n_{INT}(t = +\infty)$ and $p_{INT}(t = +\infty)$. This is just about observable on the given graphs of **Figure 3.8 (a)** by looking at the yellow $p_{INT}(t)$ at $t = 50$ ms. The surplus of electrons and holes then recombine to yield a final state of equilibrium. This overshooting of the carrier response is supported by similar simulations conducted in **[120]**.

3.4.2 Response Time Analysis With Fixed Oxide Charge

Now, let us perform the same type of analysis on a substrate structure in which an interfacial fixed oxide charge density of $N_{ox} = 10^{11}$ cm^{-2} is defined.

Figure 3.9 (a) and (b) plot the evolution of the interfacial carrier concentrations $p_{INT}(t)$, $n_{INT}(t)$, and $N_{free_{INT}}(t)$.

Once again, the introduced voltage step pulses the structure from a state of strong accumulation to a state of strong inversion for all considered substrates. Once more, the large interfacial hole density p_{INT} must be repelled, and a large interfacial electron density n_{INT} must be induced.

Final equilibrium must once again be obtained by thermal generation and recombination, and will only be established after 1-10 ms for the arbitrary (TCAD Atlas default) SRH parameters used in these simulations, and that will be discussed in the next section.

However, there are large reservoirs of electrons in the system, induced to the left and right of the signal CPW line by the positive N_{ox}. At the initial equilibrium point $t = 0$, there is an electronic PCS layer (inversion in P-type substrates) present over the entire wafer, except beneath the signal line where a state of accumulation is enforced by the initial applied -10 V.

As the voltage is ramped to +10 V, a *partial equilibrium* can be achieved quite rapidly (at least compared to the previous case for $N_{ox} = 0$) because the number of *available* minority carriers is high, as they are present in large quantities in the PSC regions over the entire wafer.

Figure 3.9 shows that at a time close to $t = \tau_{sub}$, the carriers have had time to spatially rearrange themselves in response to the voltage step, to minimize the global non-equilibrium as best they can. The key difference compared to **Figure 3.8** is that the magnitude of electron response is much higher, due to the availability of a much higher number of electrons in the system. The effect is that *strong-depletion* is avoided at the interface, and a *partial equilibrium* is reached instead. Indeed, **Figure 3.8 (b)** shows that *strong-depletion* spans from $t = \tau_{sub}$ to $t = \tau_{th}$, but in **Figure 3.9 (b)** a significant portion of the required electron density can flood to the interface within a few nanoseconds. Though this *partial equilibrium* density $n_{INT}(\tau_{sub} < t < \tau_{th})$ is not the final equilibrium density $n_{INT}(t = +\infty)$, the interface cannot be said to be in a state of depletion, and actually fairly strong inversion is obtained with a fast time response.

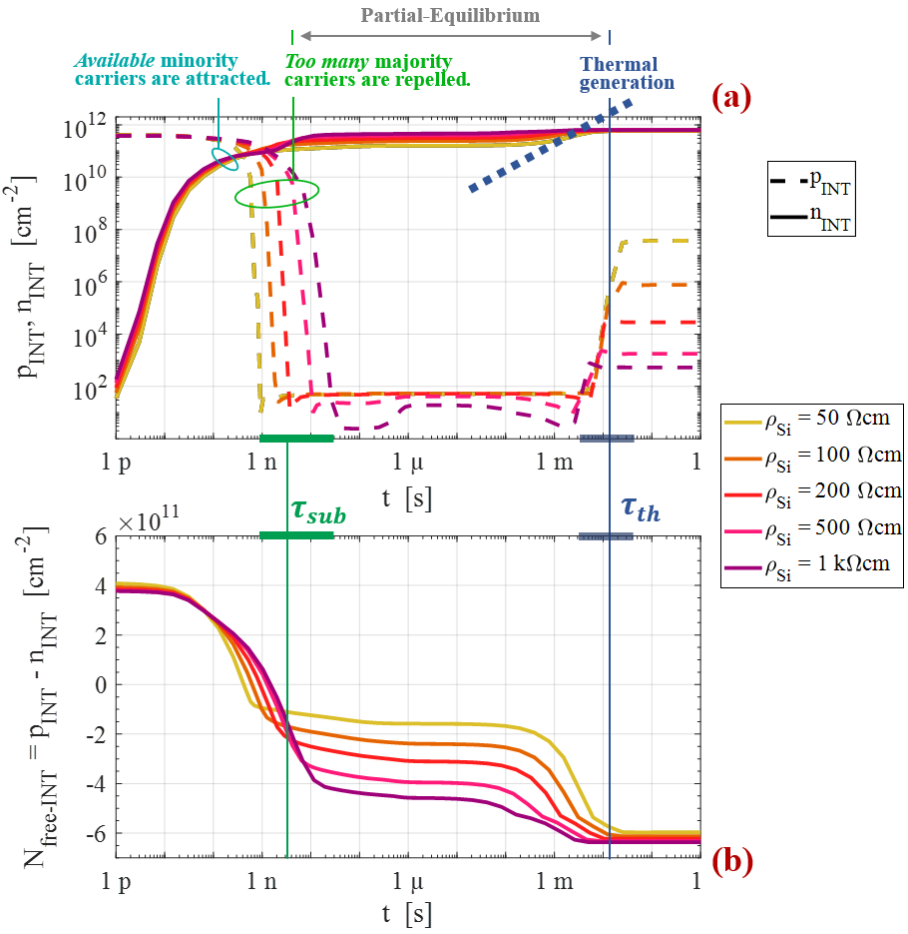


Figure 3.9: Simulations of the evolution over time of interfacial free carrier densities in P-type substrates in response to a transient voltage pulse from -10 V (strong accumulation) to +10 V (strong inversion) with a 1 ps ramp time. A fixed interfacial oxide charge density of $N_{ox} = 10^{11}$ cm^{-2} is present at the Si/SiO_2 interface.

The magnitude response of the attracted inversion layer is larger for lower doped substrates, as the available minority carrier density in the PSC electronic reservoirs is higher. The interfacial PSC density below the BOX, in the regions adjacent to the central CPW line, over 1 µm depth, is approximately equal to:

$$n_{PSC_{INT}} \triangleq \int_0^{1\,\mu m} n(\bar{r})\, dy \qquad [\mathrm{cm}^{-2}] \qquad \textbf{(3.65)}$$

$$\approx N_{ox} - \int_0^{1\,\mu m} N_A\, dy \qquad [\mathrm{cm}^{-2}] \qquad \textbf{(3.66)}$$

where N_A is the nominal substrate doping, in cm^{-3}. This is the available carrier density in the reservoirs adjacent to the CPW's central signal line, and is a function of the doping, as negatively ionized acceptor dopants provide partial charge compensation to N_{ox}, meaning that the free electron PSC density in these reservoirs is lower for higher doped P-type bulks. For the 1 kΩcm silicon, the reservoir density is analytically computed using **Equation 3.66** as $9.8 \cdot 10^{10}$ cm^{-2}, which is basically equal to N_{ox}, as expected. For the 50 Ωcm substrate, $n_{PSC_{INT}}$ is calculated as $6.7 \cdot 10^{10}$ cm^{-2}. Both of these interfacial density values agree well with those extracted from the TCAD solutions (using **Equation 3.65** in the TCAD extraction).

Figure 3.9 (b) highlights the fact that substrates with a higher reservoir density provide carriers in densities closer to the final required equilibrium values. We note that, after 10 ns, the 1 kΩcm substrate has provided 62% of the final strong inversion density, while the 50 Ωcm substrate has provided 19%[31]. Both of these numbers correspond to a significant proportion and therefore to a condition of quite strong inversion, and so we say that *partial equilibrium* is attained below the signal line within a few nanoseconds, thanks to the available minority carriers. This response time is not governed by τ_{sub}, as these carriers do not move through the substrate region characterized by ρ_{Si}, but come instead from the PSC reservoirs. It is therefore observed that the minority carrier response time is fairly independent of the nominal substrate doping, in contrast to the majority carrier response time.

The TCAD simulations also revealed that the deep-depletion effect was extended to the depletion regions below the PSC layers adjacent to the signal electrode location. As minority carriers leave the PSC layer to flood below the signal electrode, some non-equilibrium is propagated to these regions, which then have too few interface minority carriers to balance the oxide charges.

[31] These numbers are simply computed as the ratio of $n_{INT}(\tau_{sub} < t < \tau_{th})$ and $n_{INT}(t = +\infty)$.

The depletion regions below these interfaces are then extended deeper into the substrate, to provide some compensation charge by pushing away majority carrier into the bulk, causing a net negative space charge in these regions due to the ionized acceptor dopants of the P-type silicon. These effects contribute to the responses observed around the time τ_{sub}, as they involve movements of majority carriers into the silicon bulk.

Once more, *too many holes* are repelled from the interface, in the sense that $p_{INT}(\tau_{sub} < t < \tau_{th}) \ll p_{INT}(t = +\infty)$.

3.4.3 Trap-Assisted Recombination Time τ_{th}

In this section, approximate calculations are made to justify the order of magnitude of τ_{th}, observed in the range of 1-10 ms from the TCAD, based on an analytical analysis using the defined SRH parameters.

When considering transient trapping phenomena, it is difficult to come up with practical expressions of the generation rates U_n and U_p without making some approximations. One widely used approximation is to consider carrier generation to be in a *steady-state*, that supposes a constant trap occupancy at any given point in space. Mathematically, constant trap occupancy writes as:

$$\partial n_t/\partial t = -\partial p_t/\partial t = 0 \qquad \text{in steady-state} \qquad [\text{cm}^{-3}\text{s}^{-1}] \quad \textbf{(3.67)}$$

Equation 3.39 then reduces to:

$$U_n = U_p = U_{SRH} \qquad \text{in steady-state} \qquad [\text{cm}^{-3}\text{s}^{-1}] \quad \textbf{(3.68)}$$

And, by plugging the expressions of U_n and U_p into this equation, using **Equations 3.33 and 3.34 and 3.22 to 3.25**, we can solve for an expression of $F(E_t)$. By then inputting this expression of $F(E_t)$ into either U_n or U_p (**Equation 3.33 or 3.34**), the steady state recombination rate, first derived by Shockley, Read and Hall **[121–123]**, can be expressed as:

$$U_{SRH} = \frac{pn - n_i^2}{\tau_{p0}\left(n + n_i \exp\left\{\frac{E_t - E_i}{kT}\right\}\right) + \tau_{n0}\left(p + n_i \exp\left\{\frac{E_i - E_t}{kT}\right\}\right)}$$

$$\text{in steady-state} \qquad [\text{cm}^{-3}\text{s}^{-1}] \quad \textbf{(3.69)}$$

where E_i is the intrinsic energy level[32], and where $\tau_{n0} = 1/(v_n \sigma_n N_t)$ and $\tau_{p0} = 1/(v_p \sigma_p N_t)$. These lifetimes are defined in **[112]** as the lifetime for electrons (holes) injected into a highly p-type (n-type) specimen. Under those conditions, τ_{n0} and τ_{p0} can then be obtained by replacing $p_t = N_t$ in **Equation 3.15** (by replacing $n_t = N_t$ in **Equation 3.16**)[33].

[32] The intrinsic energy level is given by $E_i = E_V + E_g/2 + kT\ln(N_V/N_C)/2$, and is very close to midgap ($E_V + E_g/2$), even at high temperatures.

[33] When no trapping centers are explicitly defined by the user of the TCAD tool (such as defining precise trap distribution functions in a polysilicon layer), and a steady-state simulation is considered, the TCAD default parameters are to set directly the values of τ_{n0} and τ_{p0}, to a value of 10^{-7} s. The information N_t is not required outside of non steady-state simulations. Please note that non-equilibrium may still be simulated using this approach, as long as the structure is in a steady state (examples: DC currents flowing in PN diodes, MOSFETs, etc.).

It is noteworthy to point out that, in steady-state, the electron and hole lifetimes τ_n and τ_p become constant, as they depend on trap occupancy (see **Equations 3.15 and 3.20**).

Though an approximation, this expression of U_{SRH} will enable the rough analytical evaluation of τ_{th} obtained through the transient TCAD simulations. The TCAD did not assume steady-state, but instead solved for the fully coupled continuity equations of both carriers and traps. To justify this approach, we can cite the work in **[120]**, in which time domain large-signal stepped transient voltages were also applied to a MOS structure. In that work, it was shown that though the steady state approximation affects the carrier responses between times τ_{sub} and τ_{th}, it does not really affect the value of τ_{th} itself.

Rough Calculation Based on the Steady-State Approximation

Equation 3.69 shows that, of course, at equilibrium, $np = n_i^2$, and there is no net recombination or generation. Out of equilibrium, non-zero source terms U_n and U_p contribute to the continuity equations to bring the system back to an equilibrium point.

Considering the simulation case of **Section 3.4.1** without oxide charge, a step function was applied to a P-type MOS capacitor from an initial state of strong accumulation to a final state of strong inversion. In this case, minority carriers need to be generated in order to reach equilibrium. **Equation 3.69** highlights the fact that most of the generation (negative U_{SRH}) will occur in regions for which $np \ll n_i^2$. Most of the electron generation will therefore take place in the strong depletion regions. By considering $n \ll n_i$ and $p \ll n_i$, and by taking into account that the trap's energy location is at midgap ($E_t \approx E_i$)[32], **Equation 3.69** reduces to the following in the depletion regions:

$$U_{SRH} \approx \frac{-n_i}{\tau_p + \tau_n} \qquad \text{in the strong depletion regions} \quad [\text{cm}^{-3}\text{s}^{-1}] \quad \textbf{(3.70)}$$

Multiplying this rate by the deep depletion width gives us a generation rate expressed per unit area:

$$U_{SRH_{INT}} = U_{SRH} \cdot t_{deep-dep} \qquad \text{in the deep depletion regions} \quad [\text{cm}^{-2}\text{s}^{-1}] \quad \textbf{(3.71)}$$

By analyzing the TCAD results over space, we extract the deep depletion widths $t_{deep-dep}$ for the 1 kΩcm and 50 Ωcm substrates, that are 27 µm and 5.5 µm, respectively[34].

The TCAD results also give us the total generated minority carriers $n_{INT}(t = +\infty)$ that must be generated to balance the new applied voltage. For the 1 kΩcm and 50 Ωcm substrates, we extract $5.3 \cdot 10^{11}$ cm^{-2} and $5.0 \cdot 10^{11}$ cm^{-2}, respectively[35,36].

Knowing the generation rate and the total number of required carriers, we can estimate the thermal response time as:

$$\tau_{th} \approx -\frac{n_{INT}(t = +\infty)}{U_{SRH_{INT}}} \qquad [\text{s}] \tag{3.72}$$

For the 1 kΩcm and 50 Ωcm substrates we obtain analytically thermal time constants τ_{th} of 3.9 and 18.1 ms, respectively.

These simple calculations, based on the steady-state approximation of generation and recombination statistics, agree well with the 1-10 ms response time range obtained from the full TCAD simulations. They explain how lower doped substrates respond faster than higher doped ones due to larger deep depletion regions that act as the dominant sources of minority carriers.

It is important to note that $n_{INT}(t = +\infty)$ depends on the voltage perturbation value, and therefore so does τ_{th}.

The thermal time constant τ_{th} can vary by several orders of magnitude, depending on the density of recombination centers and their energy levels. In particular, surface recombination, that is assisted by traps attributed to imperfect interfaces between different materials, is known to strongly impact the thermal

[34] Note that the equilibrium depletion widths are significantly smaller, by a factor of approximately 3 for both substrates: 7.5 µm and 1.7 µm for the 1 kΩcm and 50 Ωcm substrates, respectively.

[35] The $0.3 \cdot 10^{11}$ cm^{-2} lower charge density for the 50 Ωcm substrate is provided for by the higher concentration of negatively ionized acceptor dopants. $N_{A_{50}} = 3 \cdot 10^{14}$ cm^{-3} and $\int_0^{1\,\mu\text{m}} N_{A_{50}}\, dy = 0.3 \cdot 10^{11}$ cm^{-2}.

[36] Note that $n_{INT}(t = +\infty)$ does not necessarily have to be extracted from the TCAD data, but can be estimated as approximately equal to $N_{free_{INT}}$ in strong inversion, that is equal to $-N_{Applied}(V = +10)$ at thermal equilibrium, that can be calculated from **Equation 3.57**. This is approximate because charges from ionized dopants and free holes are neglected, which is a valid assumption in very strong inversion, such as induced by +10 V applied to a 400 nm oxide. Indeed, we calculated[35] a charge density provided by ionized acceptor dopants for the most highly doped considered substrate as $0.3 \cdot 10^{11}$ cm^{-2}, which is only 6% of $n_{INT}(t = +\infty)$ in the strong-inversion case considered here.

generation/recombination time [124]. However, it is important to point out that in the context of this work, the substrate dynamics of most importance are those occurring before 10 ns, as this thesis focuses on the non-linear modelling of semiconductor substrates subjected to large-amplitude RF signals, with time periods of the order of 1 ns or less.

Note that the steady-state recombination rate give by **Equation 3.69** considers a single trap level at energy E_t. When considering multiple levels, an analogous recombination/generation rate can be developed [61][37].

[37] In particular, the expression of U_{SRH} is given while considering the four tail/Gaussian continuous state distributions associated to polysilicon (see **Section 3.2.2 pg. 78**) in section *"14.2.5 Steady Steady-State Trap Recombination"* (page *728*) in *"Chapter 14 TFT: Thin-Film Transistor Simulator"* of [61].

3.4.4 Dielectric Relaxation Time τ_{sub}

In this section, some physical description is associated with the substrate dielectric relaxation time $\tau_{sub} = 2\pi\rho_{Si}\varepsilon_{Si}$.

From the transient voltage-step simulation results applied to a MOS structure from **Sections 3.4.1 and 3.4.2**, τ_{sub} was observed as the time required for the majority carriers in the initial accumulation layer to be repelled from the interface. Once the applied voltage switches polarity, the entire substrate, from below the BOX to the reference substrate electrode, can be seen as a leaky capacitor. Before the voltage step is applied, at $t = 0^-$, the MOS structure is in a state of accumulation. This situation is depicted in **Figure 3.10 (a)**, and the structure is in equilibrium, with the carrier drift and diffusion currents being of equal amplitude and of opposite directions.

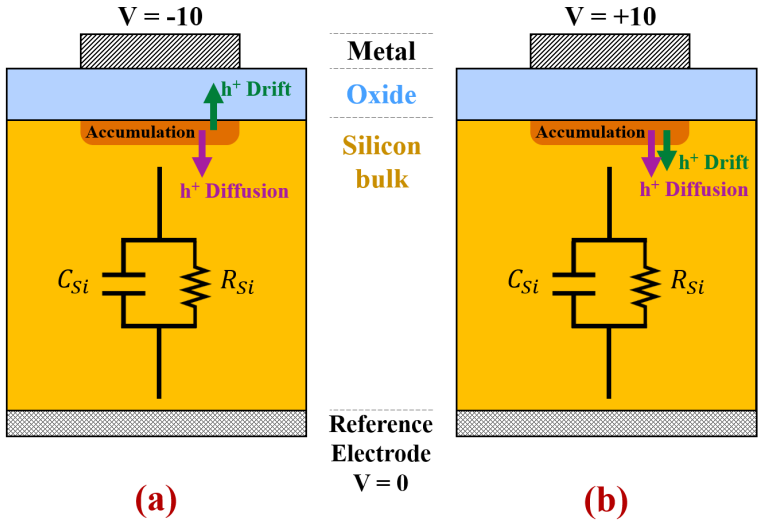


Figure 3.10: P-type MOS structure subjected to a large-amplitude voltage step at time $t = 0$. **(a)** Situation at the initial equilibrium point $t = 0^-$ in strong accumulation at $V = -10$ V. **(b)** Situation at just after the voltage step at $t = 0^+$ and $V = +10$ V: the accumulation layer of holes will discharge through the substrate that acts as a leaky capacitor C_{Si} in parallel with R_{Si}.

After the voltage step, at time $t = 0^+$, a non-equilibrium state is imposed in which drift is no longer compensated by diffusion, and the excess carriers on this silicon capacitor must discharge. This is depicted by **Figure 3.10 (b)**.

The excess holes at the BOX interface must discharge to the reference electrode through the parallel R_{Si} and C_{Si} of the substrate. Regardless of the geometrical factors governing the absolute values of R_{Si} and C_{Si}, the time constant associated with the discharge of C_{Si} through R_{Si} is given by $\tau_{sub} = R_{Si}C_{Si} = 2\pi\rho_{Si}\varepsilon_{Si}$.

We can define $f_{sub} = 1/\tau_{sub}$ as the dielectric relaxation frequency. This frequency carries its name well, as above this frequency, majority carriers cannot follow an applied AC signal, and have restricted movement in substrate regions characterized by ρ_{Si}. As a consequence, the material acts as a lossy[38] dielectric.

Though τ_{sub} defines the response time of excess carriers (majority carriers in our case under study) that are repelled into the substrate, it does not determine the response time of deficient carriers (minority carriers in our case under study). Though in some situations minority carrier responses can be ignored, this is certainly not the case for our considered substrates when an interfacial oxide charge is present, as it induces large reservoirs of minority carriers in the vicinity of our MOS structures. The minority carriers respond with a different time constant than $\tau_{sub} = 2\pi\rho_{Si}\varepsilon_{Si}$ because the drift of these carriers does not involve movements through the substrate characterized by ρ_{Si}. Instead, they drift from the PSC reservoir regions to the left and right of the electrode. This was discussed in **Section 3.4.2**, where **Figure 3.9 (a)** shows indeed that the minority carrier response time does not depend on ρ_{Si}[39]. It does however depend on the dimensions of the MOS structure, i.e. on the size of the electrode, because the *RC* time constant related to this interfacial PSC layer is geometry-dependent[40].

[38] It is important to note that the R_{Si} term in parallel with the C_{Si} term is still a source of energy loss. Indeed, carriers move less in a given AC cycle at higher frequencies, but there are more cycles in a given time span, and the RMS power loss $V^2(t)/(\sqrt{2}R_{Si})$ remains constant, regardless of the frequency of the $V(t)$ signal.

[39] There is a second order dependency because the nominal substrate doping slightly affects the electronic density in the inversion PSC reservoirs.

[40] The electrons must come from the PSC reservoirs adjacent to the MOS electrode. The number of available electrons directly adjacent to the electrode scale with its perimeter, while the number of required electrons to attain equilibrium scale with its area. This means that electrons in the PSC layer will have to flow from further away for larger electrodes, which will lead to a longer delay. Furthermore, depending on the physical dimensions, displacement time beneath the electrode itself may be significant.

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3.4.5 Impact of Fundamental Frequency on Harmonic Distortion

We have overviewed carrier dynamics and response times in a MOS structure subjected to a large-amplitude voltage step. It is clear from those discussions that the frequency of a large-amplitude sine wave will determine the magnitude of free carrier response.

To illustrate this, the same CPW MOS structure (depicted in **Figure 3.12**) is subjected to an RF signal at frequency f with an amplitude of 2.5 V centered around a DC bias point of 0 V. The considered substrate is a 1 kΩcm P-type, without any polysilicon layer, and with an interfacial oxide charge density of $N_{ox} = 10^{11}$ cm^{-2}. The simulated interfacial free carrier density $N_{free_{INT}}(t)$ (defined as before over 1 µm depth according to **Equation 3.63**) is plotted against normalized time t/T in **Figure 3.11**, for several frequencies $f = 1/T$.

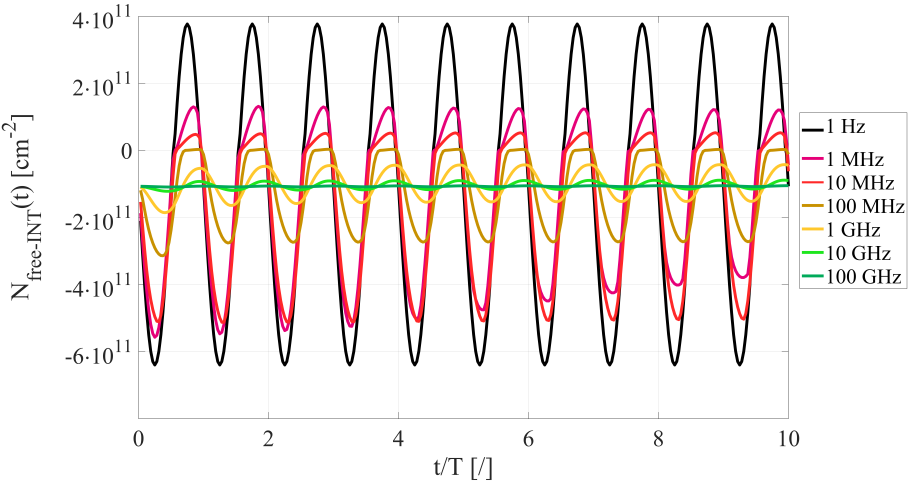


Figure 3.11: Simulated interfacial free carrier density $N_{free_{INT}}(t)$ below a MOS CPW line versus normalized time t/T for a 2.5 V amplitude sinusoidal excitation around 0 V DC bias for several frequencies $f = 1/T$. The substrate is a 1 kΩcm P-type with a 400 nm oxide characterized by $N_{ox} = 10^{11}$ cm^{-2}. No polysilicon trap-rich layer is present.

At the very low frequency of $f = 1$ Hz we can say that the substrate is in equilibrium at each point in time, and so the amplitude of the $N_{free_{INT}}(t)$ response is maximum.

As the frequency is increased, the inertia of the dynamic effects limit the

amplitude response of $N_{free_{INT}}(t)$. This is observable already above a few hundred Hertz, as the final equilibrium time is of the order of 1-10 ms (see **Section 3.4.2**).

From a few kHz to a few hundred MHz, only carriers that were initially present in the MOS structure can rearrange themselves within the substrate in response to the large signal, and their movement is governed by finite response times, as discussed previously. In this frequency range, and with an interfacial charge density N_{ox} of 10^{11} cm^{-2} defined, partial equilibrium can be obtained within a few ns, and the variation in $N_{free_{INT}}(t)$ still remains significant (see **Section 3.4.2**).

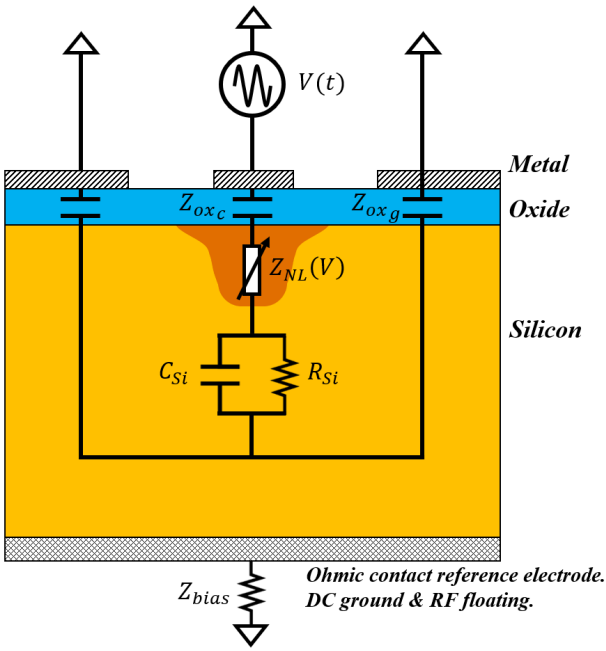


Figure 3.12: Cross-section of the simulated MOS CPW structure. The RF wave is applied between the central line and the two outer lines. The two outer lines are set to the same DC potential as the back-side of the substrate, that is biased through a large resistor to be RF floating. A simplified equivalent circuit model is overlayed on the structure to roughly highlight the linear and non-linear regions of the substrate.

However, as the frequency increases above a few GHz, the carrier response amplitude decreases significantly, as then even the existing carriers cannot follow the RF signal. This is in agreement with the carrier response times of the order of the nanosecond, for both minority and majority carriers (see **Section 3.4.2**).

This is highlighted in **Figure 3.13 (a)**, that plots the amplitude of the net free interfacial charge density $\boldsymbol{A}\{N_{free_{INT}}(t)\}$ as a function of frequency. The effective conductivity $\sigma_{eff} = 1/\rho_{eff}$ of the substrate is given in the same plot on a different axis. Three DC bias conditions are considered. The frequency dependency of ρ_{eff} was described previously in **Section 2.1.2**: due to the conductive nature of a HR substrate suffering from the PSC effect, the propagation mode is the *slow-wave mode* at low frequencies because the E-field is mainly concentrated within the insulator material that dominates the substrate impedance, and the silicon region below the oxide basically acts as an equipotential AC node.

Figure 3.13 (b) plots the simulated second harmonic distortion component $H2$ for a fundamental output power of $H1 = +15$ dBm as a function of fundamental frequency f. It shows that the distortion is maximum around 1 GHz. This can be explained from the plots of **Figure 3.13 (b)** and based on the simplified equivalent circuit of the substrate that is superimposed on the MOS CPW structure of **Figure 3.12**. In that circuit, all impedances are linear except for the impedance $Z_{NL}(V)$, that models the silicon regions at the interface beneath the CPW line[41].

[41] In this simple representation, Z_{NL} represents a volume more or less directly beneath the central conductor of the CPW line. Most of the substrate impedance variation over time will occur in this region, but, in general, impedance variations are not limited to this region. Impedance variations may for example occur in PSC regions adjacent to the central CPW line. The TCAD tool takes these into account, but this simple representation does not depict such effects. The simple view is however helpful in performing the qualitative frequency analysis of this section.

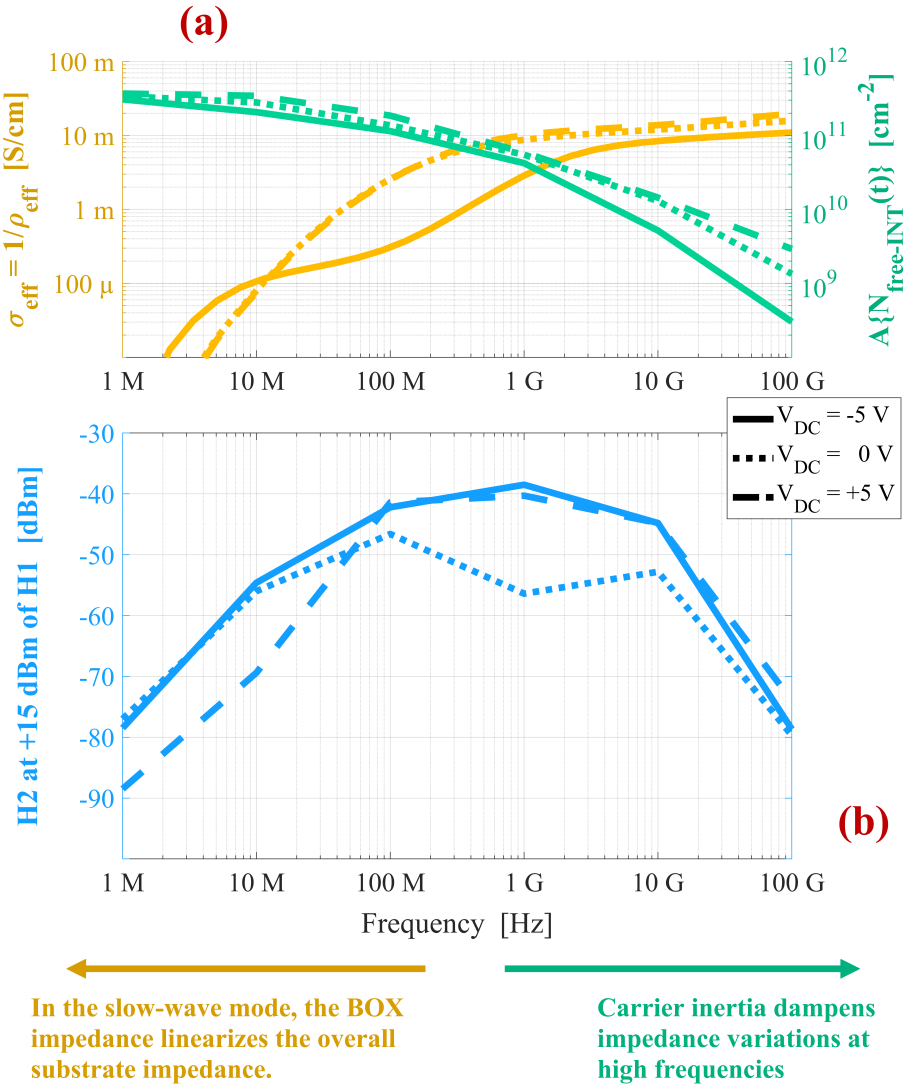


Figure 3.13: TCAD results of a CPW line simulated on a 1 kΩcm P-type HR substrate with 400 nm of oxide and $N_{ox} = 10^{11}$ cm^{-2}, plotted over frequency at three DC bias points. **(a)** Frequency dependency of the effective conductivity $\sigma_{eff} = 1/\rho_{eff}$, and of the amplitude of the net free interfacial charge density $A\{N_{free_{INT}}(t)\}$. **(b)** Frequency dependency of the second harmonic distortion component $H2$, for a fundamental component power $H1$ of +15 dBm.

The frequency dependency of the $H2(f)$ curve can be understood by the facts that:

- At lower frequencies, the (linear) dielectric impedance $Z_{ox_c} + Z_{ox_g}$ dominates the overall substrate impedance and linearizes it.
- At higher frequencies, the substrate region below the CPW signal line becomes more linear due to the finite inertia of the carriers in the semiconductor, i.e. variations in $Z_{NL}(V)$ over time are dampened by carrier inertia. The overall substrate impedance then becomes more linear.

These two effects both tend to reduce harmonic distortion, the first in the low-frequency range, and the second in the high-frequency range. The distortion is then maximum in the intermediate frequency range at around 1 GHz.

This corresponds to a frequency slightly before the end of the slow-wave mode, when the oxide impedance is no longer dominating[42] the total substrate impedance, that is characterized by $\sigma_{eff}(f)$ and $\varepsilon_{eff}(f)$[43], and before the amplitude response of $\boldsymbol{A}\{N_{free_{INT}}(t)\}$, and therefore of $\boldsymbol{A}\{Z_{NL}(t)\}$, reduces any further. It corresponds to a trade-off point between the impacts of these two effects.

We can then conclude by saying that the non-linearity of a HR substrate depends on the frequency responses of both ρ_{eff} and $\boldsymbol{A}\{N_{free_{INT}}(t)\}$. Both of these parameters depend strongly on the fixed oxide charge density at the Si/SiO_2 interface N_{ox}. The oxide impedance, and hence the oxide thickness, also impacts strongly on the $\rho_{eff}(f)$ response.

The bell shape of the $H2(f)$ curve can then be shifted up or down in frequency depending on the slow-wave transition frequency. For the case presented here, a HR with $N_{ox} = 10^{11}$ cm^{-2}, this transition frequency is in the range of 1 GHz. For TR type substrates, it is typically in the range of a few MHz. $H2(f)$ measurements will be presented in **Section 5.8**, for several TR and several HR substrates, with N_{ox} up to $2.1 \cdot 10^{12}$ cm^{-2}.

[42] It is not negligible, but is not dominating either: at 1 GHz, $Z_{ox_c} + Z_{ox_g}$ accounts for roughly 65% of the norm of the overall total substrate impedance.

[43] The effective permittivity of the substrate also changes as a function of frequency, also with higher values at lower frequencies due to the slow-wave mode. $\varepsilon_{eff}(f)$ is not reprinted in this section as its frequency dependency is closely linked to that of $\sigma_{eff}(f)$ and for the same reasons, with similar qualitative effect on $H2(f)$. The reader that is interested in visualizing the $\varepsilon_{eff}(f)$ curve of a HR substrate is invited to revisit **Figure 2.3** (note that a linear frequency scale was used in that plot).

3.4.6 Response Time Analysis With a Trap-Rich Layer

Let us now perform the transient voltage step analysis (step from -10 V to +10 V in a 1 ps ramp time), on a high-resistivity substrate structure that includes a trap-rich polysilicon layer at the Si/SiO_2 interface. The oxide layer thickness is 400 nm with an interfacial fixed charge density of $N_{ox} = 10^{11}$ cm^{-2}. The bulk silicon is P-type and has a nominal resistivity of 1 kΩcm. The polysilicon is 1 µm thick and has the same nominal doping as the bulk, and includes tail-type trap densities that are characterized by the parameter NT. The structure, that depends on NT, is identical to that described in **Section 3.3.2** (**pg. 90**).

Figure 3.14 (a) and (b) plot the evolution of the interfacial free carrier concentrations $p_{INT}(t)$, $n_{INT}(t)$, and $N_{free_{INT}}(t)$. Also plotted in **(c) and (d)** are the interfacial trapped charge (ionized traps) concentrations $N^{+}_{tD_{INT}}(t)$, $N^{-}_{tA_{INT}}(t)$, and $N_{trap_{INT}}(t)$. These are defined as:

$$N^{+}_{tD_{INT}} \triangleq \int_0^{1\,\mu m} N^{+}_{tD}(\bar{r})\, dy \qquad [\text{cm}^{-2}] \qquad \textbf{(3.73)}$$

$$N^{-}_{tA_{INT}} \triangleq \int_0^{1\,\mu m} N^{-}_{tA}(\bar{r})\, dy \qquad [\text{cm}^{-2}] \qquad \textbf{(3.74)}$$

$$N_{trap_{INT}} \triangleq N^{+}_{tD_{INT}} - N^{-}_{tA_{INT}} \qquad [\text{cm}^{-2}] \qquad \textbf{(3.75)}$$

The yellow curve of **Figure 3.14**, for which $NT = 0$, does not include a polysilicon layer at all. This yellow curve is identical to the purple curve of **Figure 3.9**[44]. As previously described, for this case, minority carriers react rapidly as they can drift from the nearby PSC regions adjacent to the pulsed MOS electrode, while the accumulation charge at the interface drifts into the bulk in a time τ_{sub}.

As the trap density NT in the polysilicon layer increases, the PSC reservoirs weaken in density. The free electrons that make up the PSC inversion regions disappear as NT increases beyond 10^{19} cm^{-3}eV^{-1}. This is of course in agreement with the observations made from **Figure 3.6** in **Section 3.3.2** (**pg. 90**), that illustrates that trapped charge $N_{trap_{INT}}$ starts to dominate over free charge $N_{trap_{INT}}$ as NT increases beyond 10^{19} cm^{-3}eV^{-1}, for the same polysilicon parameters[45].

[44] Curve labelled as "$\rho_{Si} = 1$ kΩcm" in **Figure 3.9** (**pg. 104**).

[45] $WTA = WTD = 40$ meV. In the plots of **Figure 3.6** the DC bias point was zero Volts, and so the situation is representative of the electronic configuration in PSC regions adjacent to the electrode considered here.

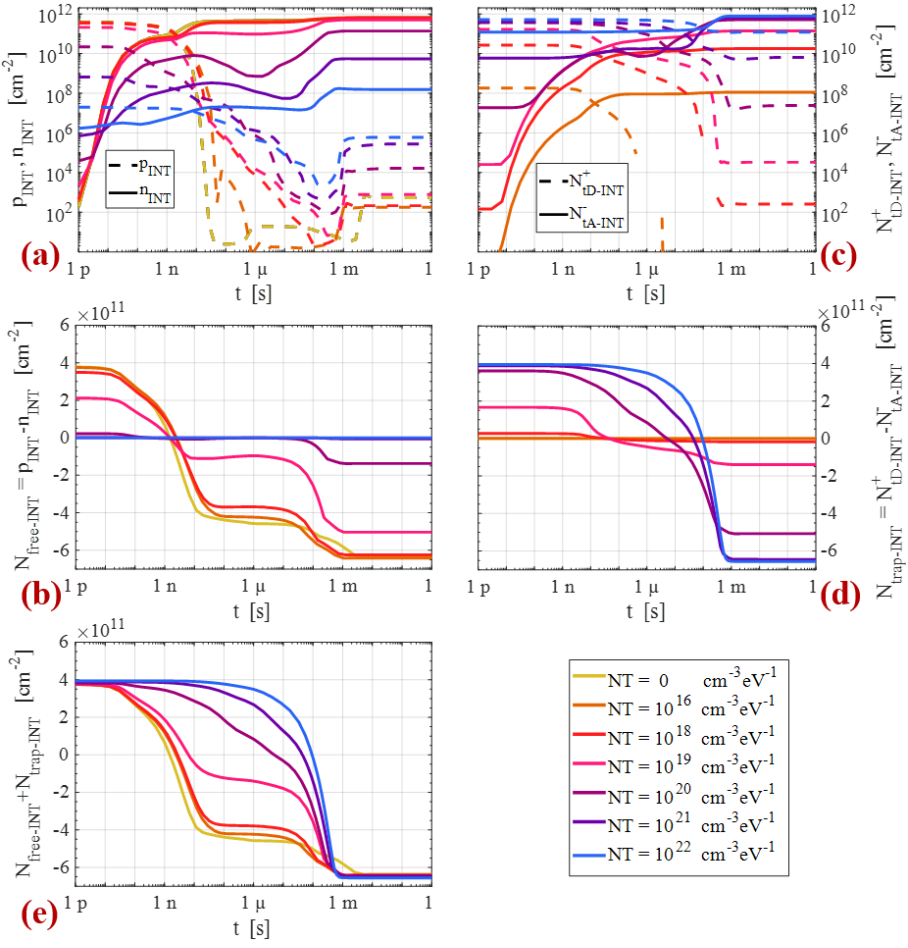


Figure 3.14: Simulations of the evolution over time of interfacial free carrier densities and ionized trap densities in P-type trap-rich substrates in response to a transient voltage pulse from -10 V to +10 V with a 1 ps ramp time. A fixed interfacial oxide charge density of $N_{ox} = 10^{11}$ cm^{-2} is present at the SiO_2 interface. A 1 µm thick polysilicon trapping layer is present below the oxide and is characterized by a density parameter NT (with $WTA = WTD = 40$ meV).

As NT increases further, the free carrier densities p_{INT}, n_{INT} and $N_{free_{INT}}$ become very low, as the Fermi level at the interface moves deep into the band gap and ionized traps provide the charge compensation. Indeed, in the substrates for which $NT > 10^{20}$ cm^{-3}eV^{-1} we observe very low $N_{free_{INT}}$ at both strong

bias conditions at $t = 0$ and at $t = +\infty$. Variations in the trapped charge densities $N^{+}_{tD_{INT}}$ and $N^{-}_{tA_{INT}}$ will provide practically all of the charge compensation. In our present case, after the voltage step $N^{+}_{tD_{INT}}$ must become lower and $N^{-}_{tA_{INT}}$ must become higher, and both of these variations require capturing a free electron from the conduction band or capturing an electron from the valence band, which is equivalent to emitting a free hole. As stated by **Equations 3.15 and 3.20** (**pg. 73**) the reaction time of $N^{+}_{tD_{INT}}$ and $N^{-}_{tA_{INT}}$ will be governed by the electron lifetime parameters τ_n and τ_{tn}. Capturing electrons from the valence band to increase $N^{-}_{tA_{INT}}$ and decrease $N^{+}_{tD_{INT}}$ is a thermal generation process, and requires time constants in the range of a millisecond to thermally fill the deep-level traps.

Figure 3.14 shows that the reaction time of the traps depends heavily on the density of available free carriers that they can interact with, which is in agreement with **Equations 3.20 and 3.21** (**pg. 74**) for τ_{tn} and τ_{tp}. It can be observed from **Figure 3.14 (b)** that trap density variations lag slightly behind the free charge density variations plotted in **(a)**, as free electrons must be brought (by drift current) to the polysilicon interface before the traps can capture them.

Therefore, **Figure 3.14 (e)** shows that the overall charge variation is slower in substrates with high amounts of trapping states, as very few free carriers are present in the low-doped and trap-rich passivated substrates, requiring thermal generation to provide practically all charge variation in the substrate, while the substrates with less traps can provide *partial-equilibrium* within a few nanoseconds by attracting available electrons present at the oxide interface (PSC). Once attracted to the interface, these electrons can be captured by the acceptor and/or donor traps[46].

[46] Please note that the step $N_{Applied}(t)$ is the same on all considered substrates. The response in $N_{comp}(t) \approx N_{free_{INT}}(t) + N_{trap_{INT}}(t)$ differs depending on the electronic and trap configurations in the substrates, however since $N_{Applied}(t = 0)$ and $N_{Applied}(t = +\infty)$ are the same for all substrates, then the initial and final equilibrium values $N_{Comp}(t = 0)$ and $N_{Comp}(t = +\infty)$ are also the same.

RF Analysis

To further highlight the different reaction times of traps and free carriers, results of both small- and large-signal simulations are presented in **Figure 3.15**.

These results pertain to substrates with a high trap density polysilicon layer at the oxide interface characterized by parameter NT that is set to $2 \cdot 10^{22}$ $\text{cm}^{-3}\text{eV}^{-1}$, for various resistivities of the P-type silicon bulk[47].

Figure 3.15 (a) and **(b)** show that the DC charge compensation is provided for almost entirely by the trap-rich layer, and so free carrier densities are independent of V_{DC} in these substrates, which explains why the curves of **Figure 3.15 (c)** and **(d)** are flat. However, free carrier densities are not independent of an RF voltage, which varies too quickly to be compensated for by the ionization/deionization of trap states. As a result, the substrate impedances *do* dependent on a large-amplitude V_{RF}, even though they do not depend on a large-amplitude V_{DC}, because of the slow time constants associated to trapping phenomena compared to the period of the RF signals considered[48].

The DC equilibrium interface Fermi-level is then pinned for every considered DC voltage, and **substrate impedance is independent of the DC signal**. However, the RF non-equilibrium quasi-Fermi levels at the interface are not pinned, and are more heavily modulated by the RF voltage the more available carriers are present in the substrate. The **substrate impedance is dependent on the RF signal**.

The amount of available free carriers determines the amplitude of substrate impedance variation in response to the RF signal[49].

[47] The other material parameters are set to: t_{ox}=400 nm, $N_{ox} = 10^{11}$ cm^{-2}, t_{poly}=1 µm, WTA=45 meV and WTD=30 meV. These parameters are ones that fit well to measured trap-rich data, as will be discussed in **Chapter 5**.

[48] We may add that the equilibrium $C(V)$ and $G(V)$ low-frequency measurements of these samples (not shown) are also flat.

[49] We can note that 900 MHz is well above the dielectric relaxation frequency associated to the 1 kΩcm, 3 kΩcm, 10 kΩcm and 40 kΩcm simulated substrates. The substrate impedance in series with the non-linear surface element is then capacitive and determined by the substrate permittivity, and is therefore identical at 900 MHz for these four substrates. The differences in $H2$ levels can then be associated to differences in the response of the non-linear surface element, which is impacted by the amount of available free carriers present in the substrate. Having said this, we acknowledge that the "surface element" may span several tens of microns away from the MIS device in such low-doped substrates. The point of this note is to draw attention to the fact that the linear G term of these substrates deep in the bulk is shorted out by the linear C bulk term.

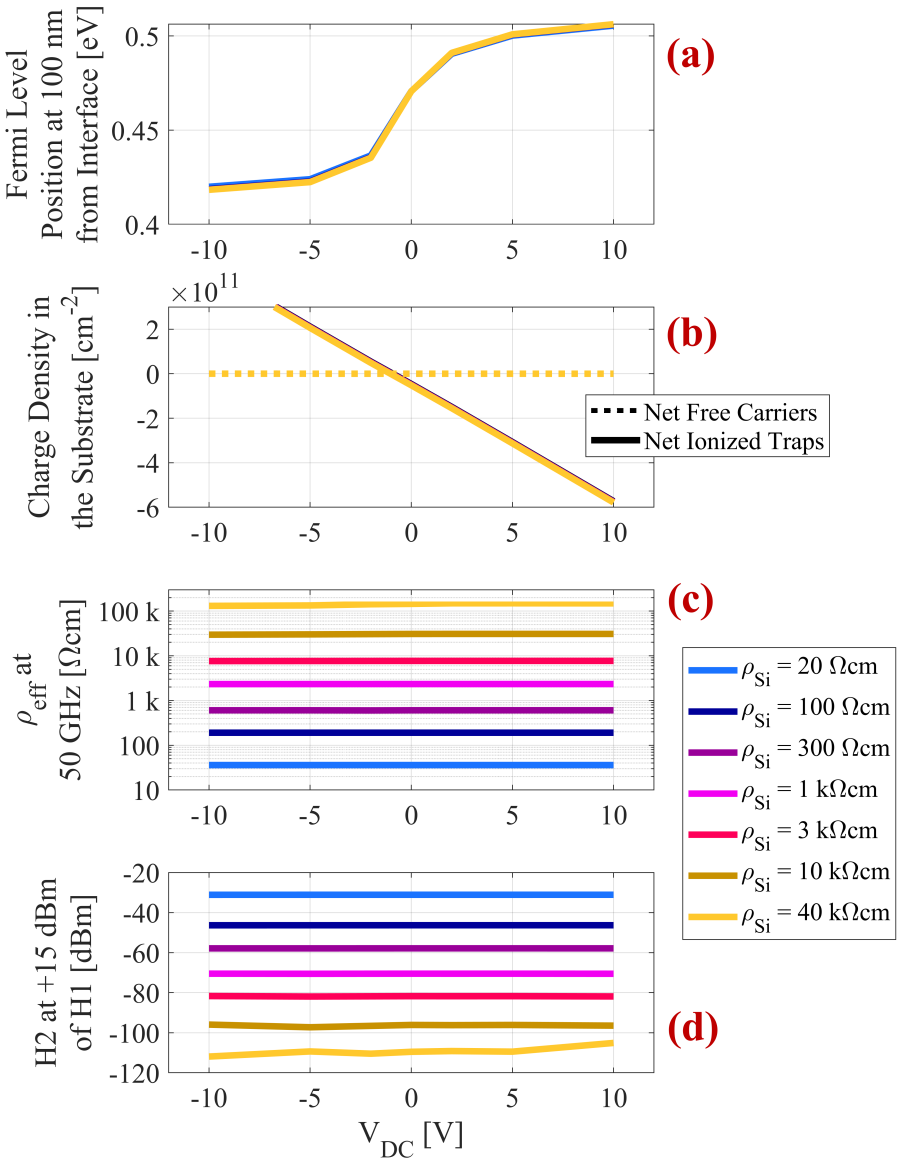


Figure 3.15: Simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC}, for several silicon bulk resistivities ρ_{Si} and with a trap-rich layer at the interface. **(a)** Position of the Fermi level at 100 nm below the oxide layer. **(b)** Interfacial densities of free charge and trapped charge. **(c)** Effective resistivity, extracted above slow-wave mode (> 10 GHz, as discussed in **Section 2.1.2**). **(d)** Second harmonic level for +15 dBm of output fundamental.

3.5 Chapter Summary

In this chapter, the interplay between applied voltage on a MIS structure, fixed interface charge, ionized traps and free carriers was put into equations and overviewed through a charge-balance type analysis.

The first part of the chapter was dedicated to presenting the key semiconductor physical concepts and relations necessary to describe the mechanisms at play in RF substrates including PSC effects and trap effects.

Following from that, these equations are put to use in a TCAD solver in order to simulate pertinent examples that give strong insight into the impact of these effects on RF substrate FoMs. The concept of net substrate compensation charge was introduced, made of either ionized trap centers or of free carriers, the latter of which is responsible for determining substrate impedance, and hence the RF substrate FoMs of effective resistivity and linearity.

First, a static approach was considered in order to illustrate the working principle of a trap-rich type of interface passivation in RF substrates: deep Fermi-level pinning.

Next, ionized trap and free carrier densities were analyzed in response to dynamic excitation signals. Using step functions to pulse a MIS structure from a strong negative applied charge to a strong positive applied charge, carrier dynamics are studied for a range of substrates, from low nominal resistivity (10 Ωcm) to high (10 kΩcm), with and without fixed oxide charge, and with and without a trap-rich layer.

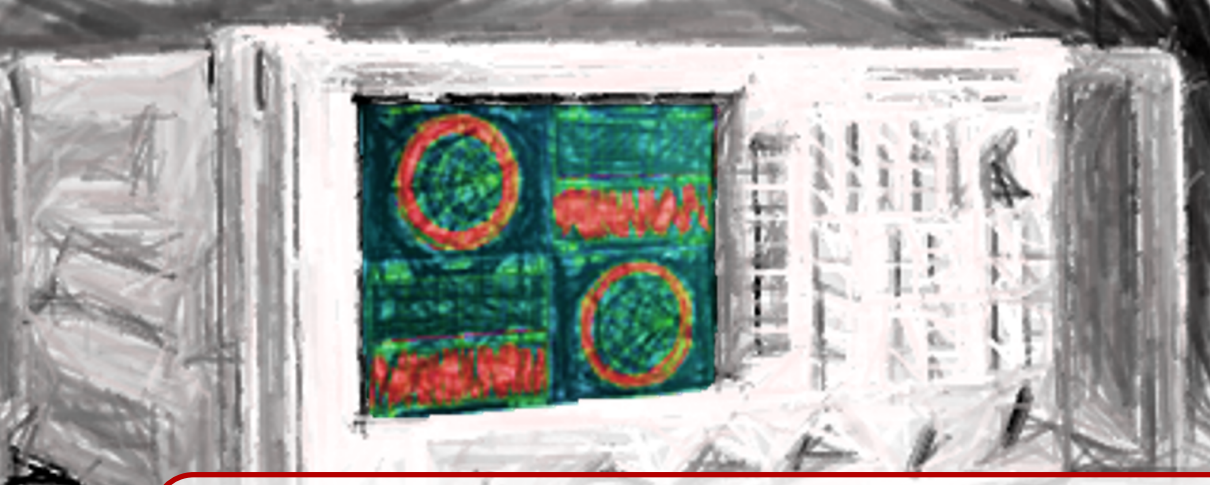
Such analyses highlight the main time constants associated to variations in trap occupation and in the substrate free carrier densities.

In particular, trap-assisted thermal recombination time constants and substrate dielectric relaxation time constants are discussed. The latter can be dominated by the presence of a PSC layer due to fixed oxide charge, as large reservoirs of *available carriers* are present in such a case.

Then, large-amplitude sinusoidal RF signals are considered as excitations. Such conditions enable us to analyze the RF FoM of harmonic distortion for various types of substrates (methodology to be described in **Chapter 4**).

By considering a wide range of fundamental excitation frequencies, these analyses allow us to evaluate the relative impact of the dielectric layer –which linearizes the overall substrate impedance of low frequency (slow-wave mode)– and that of free carrier inertia –that weakens the non-linear substrate amplitude response at higher frequencies– on the HD levels on HR and TR type substrates.

The concept of *available carriers* in the substrate is introduced in this chapter, and is of high relevance when considering high-frequency large-amplitude signals that vary too rapidly for the total amount of free carriers to change significantly in response (through thermal recombination in the cases under consideration). This concept will be of useful when analyzing RF measurement results in **Chapter 5**.



4. Large-Signal Substrate Modelling (Redacted)

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III Advanced Substrate Characterization

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Overview of Part III

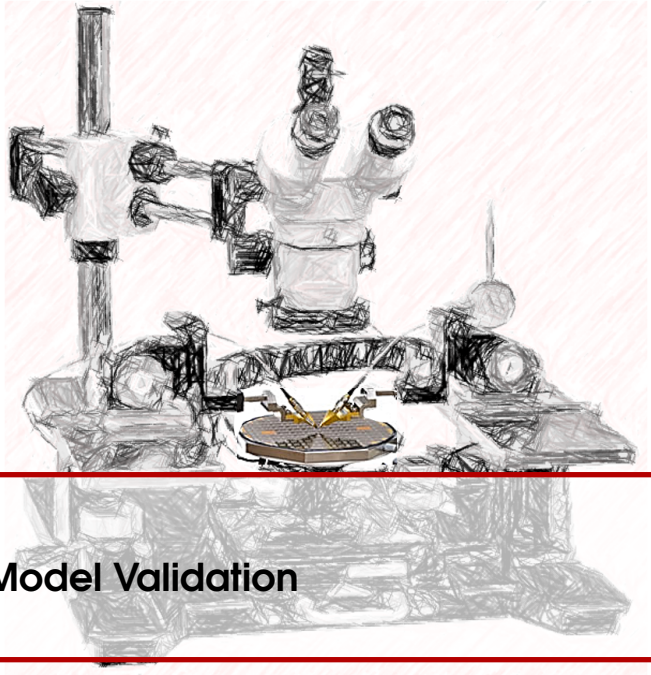
In this part, extensive on-wafer RF characterizations of a multitude of silicon-based substrates are performed.

Chapter 5 presents the correlation results of the developed large-signal model to measurement data of CPW lines on 20 different silicon-based substrates. Good correlation is observed over a wide range of material parameters (traps, doping, interface charge, etc.), excitation parameters (signal amplitude, frequency, etc.), and environment parameters (temperature, dimensions/layout of the structure, etc.).

Beyond that, the data trends can be well explained thanks to the physical understanding gained from **Chapter 3**,

The main results from **Chapter 5** have been published in **[125]**.

Chapter 8 (in appendix) is dedicated to exploring and presenting alternative silicon-based RF substrate solutions, other than the mainstream high-resistivity and trap-rich substrates. Indeed, extensive research exists on other silicon-based solutions, and this chapter then aims to review all relevant solutions. In particular, several novel substrate solutions developed as part of this work are presented and analyzed from measurement data and model results.



5. Model Validation

In this chapter, validation of the large-signal modelling of CPW lines is presented. The modelling approach was developed in **Chapter 4** based on the physical phenomena described in **Chapter 3**.

In all, 20 silicon-based samples with key differences in either the material parameters or the CPW device parameters will be used to validate the model throughout this chapter.

Specifically, the following parameters will be varied towards model validation regarding their impact on the RF FoMs of effective resistivity ρ_{eff} and generated second harmonic power $H2$:

1. As discussed in **Chapter 3**, the **DC bias** point of the CPW line relative to the substrate can cause several tens of dB shift in the generated harmonic levels. In this chapter, all 20 samples (that have dielectric thicknesses ranging from 200 nm to 1 µm) will be validated over a DC bias range from -15 V to +15 V.
2. In **Section 5.2** three high-resistivity samples with different **interfacial charge densities** are compared. The first two comprise SiO_2 as the insulator material, and have fixed interface charge densities of $8 \cdot 10^{11}$ and $2.1 \cdot 10^{12}$ cm^{-2} respectively. The third sample implements Al_2O_3 instead as the insulating material, and Al_2O_3/Si interfaces are characterized by

negative fixed charge, and this sample's interfacial charge density is found to be $-5 \cdot 10^{11}$ cm^{-2}.

3. In Section 5.3 five HR wafer and five TR wafers are considered that have **bulk silicon resistivity** values ρ_{Si} ranging from 20 Ωcm to 10 kΩcm (all 10 samples fabricated at UCLouvain). In the five considered TR samples the polysilicon layer is identical, and all variations in the RF FoMs between samples is attributed to ρ_{Si}. In the five HR samples, the interface fixed oxide charge is also fairly constant.

4. In Section 5.4 the **trap density** parameter is studied. In this section two TR samples (RFeSI^{TM} from Soitec) are presented. The two samples have similar material parameters, one of which has undergone a fairly high thermal-budget anneal step. The main difference between these two samples is then a lower trap density due to a partial recrystallization of the polysilicon layer in the annealed sample which results in a lowering of its defect density.

5. In Section 5.5 **impurity contamination of the polysilicon layer** is considered (oftentimes Boron or Phosphorous). In this section, SRP and SIMS measurements are used to determine both weakly and highly contaminated TR samples (voluntary contamination), and using this information their measurement data is compared to the physical modelling approach that can account for such impurities.

6. As semiconductor properties depend heavily on **temperature**, Section 5.6 is dedicated to confronting the model to measured data from 25°C to 190°C. In particular, intrinsic carrier concentrations and free carrier mobility will vary strongly over this temperature range in the considered HR and TR substrate samples.

7. The **CPW line geometry** is varied in Section 5.7. While Section 5.7.2 focuses on confronting the model to lines of different lengths, in Section 5.7.1 it is the CPW cross-sectional dimensions that are varied, i.e. the signal line width and the spacing to the ground lines (while maintaining close to 50 Ω characteristic impedance).

8. In Section 5.8 different **fundamental frequencies** f_0 are considered. While all other sections treat exclusively a 900 MHz excitation, this section sweeps f_0 over more than two decades, from 50 MHz to 5.4 GHz. Data pertaining to two HR samples and to two TR samples are presented.

9. Finally, **Section 5.9** is dedicated to validating the model for more exotic substrates, that do not fall strictly into one of the above categories. The eSI100^{TM} substrate, gold-doped compensated substrates and PN-junction substrates are modelled in this section.

Comparing Simulations and Measurements

In this chapter, the measured metrics of effective resistivity and second harmonic power will be used to validate the modelling approach, and will be plotted as a function of DC bias[1].

The effective resistivity will be taken at a frequency point above slow-wave mode in a frequency independent region for both the measurement and the simulation data:

$$\rho_{eff} = \rho_{eff}(f > slow\text{-}wave) \qquad [\Omega\text{cm}]$$

The second harmonic power will be taken at the point corresponding to +15 dBm of output power of the fundamental frequency tone:

$$H2 = H2(H1 = 15) \qquad [\text{dBm}]$$

For the most part, ρ_{eff} and $H2$ will be extracted from measurements/simulations of the reference CPW line used for substrate linearity benchmarking, that has a signal-line width W_C of 26 µm and a signal to ground line spacing S of 12 µm, along with a line length L of 2.1 mm. Exceptions arise in **Section 5.7** that is dedicated to validating the model for various CPW line geometries.

Furthermore, the material parameters are tailored to fit spreading resistance profile (SRP) measurements, when available. SRP data is obtained by measuring the DC resistance between two probe tips in contact with the semiconductor material over distance in a physical sample. The sample is cut along a bevel with an acute angle, in order to have sufficient spatial resolution over depth normal to the interface of interest. The measured SRP data is compared to simulated SRP data for several samples. The simulated SRP methodology is described in **Appendix A**, which is based on extracting the resistivity profile along a bevelled

[1] Other harmonics are not considered for the fitting, as $H2$ is dominant in the considered power range (input up to +25 dBm), and $H3$ has been observed through experience to be unsatisfactorily reliable during measurements. One source of $H3$ dependency that we have observed through experience is the probe to pad contact quality, and **[126]** mentions this effect as well.

substrate to emulate the SRP measurement procedure. Then, the measured local resistivity as a function of depth is compared to the simulation results:

$$\rho(y) \qquad [\Omega\text{cm}]$$

The measured $\rho(y)$ profiles contain information about polysilicon contamination by unwanted dopants, and will be used to tune these inputs of the material model.

5.1 Description of the Reference Samples

All 20 samples can be generically represented by the structure of **Figure 5.1**. Aluminum passive devices are patterned atop a dielectric (usually SiO_2) / silicon stack. Furthermore, in some samples, the bottom SiO_2 interface may be passivated with a polysilicon layer.

In this structural model, the polysilicon is defined over a thickness t_{poly}, while the traps are defined over a thickness $t_{trap} \leq t_{poly}$. This modelling approach was chosen because it is common for partial recrystallisation of the polysilicon to take place during some process steps (usually involving significant thermal budgets) due to the contact with the crystalline bulk template material. Then, it is expected for the trap density in the polysilicon to be lower close to the bulk interface, and higher further away from it, closer to the BOX interface. There is then a spatial distribution of the trap densities over the polysilicon thickness. In the presented structure of **Figure 5.1** this distribution is simply modelled as a step function with a uniform (in space) trap density defined over the thickness t_{trap}, and no traps defined beyond that thickness in the polysilicon layer. A more complex distribution could be chosen, but in the context of this work, the step distribution is sufficient to demonstrate the model capabilities[2].

Impurity contamination is also included in the proposed structure, where $N_{A,poly}$ represents the density of shallow (usually acceptor) dopants present in the polysilicon later. For the considered samples of this work, the impurities are usually P-type from Boron contamination, unless explicitly stated otherwise. Because diffusion is higher in the polysilicon trap-rich layer than in the silicon bulk, impurities introduced at the interfaces will tend to stay within the polysilicon layer rather than diffuse out into the bulk. From spreading resistance profile

[2] Also, there is a lack of physical measurements of trap densities over space for the considered samples.

(SRP) measurements such contamination is shown to significantly impact the carrier density and hence local resistivity of trap-rich substrates, especially in the lower portion of the polysilicon layer where lower trap densities are expected. $N_{A,poly}$ is defined over the entire thickness t_{poly} in the proposed structure. The on-wafer measurements confirm that contamination levels have an appreciable impact on the RF figures of merit.

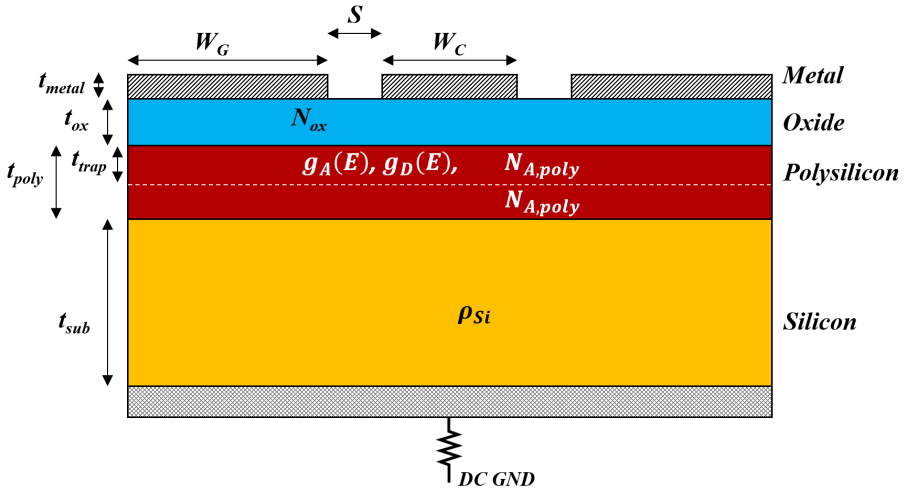


Figure 5.1: Main material parameters and dimensions of a CPW structure on a generic silicon-based substrate sample.

Details of each sample's parameters are listed in **Table 5.1**, with reference to those represented in **Figure 5.1**[3].

Furthermore, the parametric studies described previously are highlighted for each wafer.

Finally, this table also lists the values of the main RF figures of merit ρ_{eff} and $H2$. The highest and lowest measured values obtained over the DC bias range from -15 V to +15 V are given for these two RF FoMs.

The parameters depicted in **Figure 5.1** and listed in **Tables 5.1 and 5.2** serve as the model input parameters for all 19 substrates considered in **Table 5.1**.

[3]Please note that all samples implement SiO_2 as the dielectric material except for sample **HRAl$_2$O$_3$**, that implements Al_2O_3 instead. For this sample, metrics N_{ox} and t_{ox} do not represent SiO_2 parameters, but represent Al_2O_3 parameters.

Name	Study	Comment	t_{ox} [µm]	N_{ox} [cm^{-2}]	t_{poly} [µm]	t_{trap} [µm]	Trap Config.	$N_{A,poly}$ [cm^{-3}]	ρ_{Si} [Ωcm]	ρ_{eff} [Ωcm]	$H2$ [dBm]
HRD1	1,2,7.1,8	HR with SiO_2 dielectric	0.2	$8 \cdot 10^{11}$	/	/	/	/	5 k (P)	17 to 50	-12 to -52
HRD2	1,6,7.2	HR with SiO_2 dielectric	0.2	$1.6 \cdot 10^{12}$	/	/	/	/	5 k (P)	8 to 10	-12 to -45
P01	1,2,8	HR	0.4	$2.1 \cdot 10^{12}$	/	/	/	/	10 k (P)	9 to 11	-50 to -59
HRAl$_2$O$_3$	1,2,7.1	HR with Al_2O_3 dielectric	0.2	$-5 \cdot 10^{11}$	/	/	/	/	5 k (P)	28 to 76	-25 to -57
C38	1,4	Very low bulk ρ_{Si}	1	$9 \cdot 10^{11}$	/	/	/	/	20 (N)	21	-61 to -64
C39	1,4	Low bulk ρ_{Si}	1	$9 \cdot 10^{11}$	/	/	/	/	130 (N)	32 to 36	-55 to -57
C40	1,4	Medium bulk ρ_{Si}	1	$9 \cdot 10^{11}$	/	/	/	/	650 (N)	43 to 50	-53 to -56
C41	1,4	High bulk ρ_{Si}	1	$9 \cdot 10^{11}$	/	/	/	/	5 k (N)	41 to 48	-53 to -56
C42	1,4	Very high bulk ρ_{Si}	1	$9 \cdot 10^{11}$	/	/	/	/	10 k (N)	42 to 48	-52 to -57
C20	1,4	TR with very low ρ_{Si}	0.52	$1 \cdot 10^{11}$	0.47	0.47	*A*	0	20 (N)	41	-27
C21	1,4	TR with low ρ_{Si}	0.52	$1 \cdot 10^{11}$	0.47	0.47	*A*	0	130 (N)	210	-41
C22	1,4	TR with medium ρ_{Si}	0.52	$1 \cdot 10^{11}$	0.47	0.47	*A*	0	650 (N)	1.8 k	-60
C23	1,4	TR with high ρ_{Si}	0.52	$1 \cdot 10^{11}$	0.47	0.47	*A*	0	5 k (N)	30 k	-85
C24	1,4	TR with very high ρ_{Si}	0.52	$1 \cdot 10^{11}$	0.47	0.47	*A*	0	10 k (N)	104 k	-96
B28	1,3,4,5,6,7.2,8	eSI80 sample	0.4	$1 \cdot 10^{11}$	2	1	*A*	$1.4 \cdot 10^{14}$	5 k (P)	9 k	-81
B45	1,3,6	Annealed eSI sample	0.2	$1 \cdot 10^{11}$	2	1	*B*	$1.4 \cdot 10^{14}$	10 k (P)	2.1 k to 3.4 k	-62 to -70
B46	1,5,6	Contaminated eSI sample	0.2	$1 \cdot 10^{11}$	2	1	*A*	$7 \cdot 10^{14}$	14 k (P)	650 to 840	-61 to -69
B67	1,4,5,6,7.2,8	eSI100 sample	0.4	$1 \cdot 10^{11}$	2	1	*A*	$5 \cdot 10^{13}$	40 k (P)	62 k	-101
TRu	1,7.1	Mask with wider CPWs	0.5	$1 \cdot 10^{11}$	0.5	0.5	*C*	0	5 k (P)	4 k to 6 k	-80 to -83
Info	1: DC Bias, 2: Fixed Charge, 3: Trap Density, 4: Bulk Doping, 5: Contamination, 6: Temperature, 7.1: CPW Width, 7.2: CPW Length, 8: Frequency.	Samples are sorted roughly by order of appearance in this chapter.	Ellipsometry meas. RFeSI™ specification.	From MOS capacitance CV meas. Unknown (non-critical).	Meas. RFeSI™ specification.	Used towards SRP fitting.	Trap configurations listed in **Table 5.2**.	From SIMS meas. Estimated from SRP meas. Unknown (set to 0 in sim.).	From SRP meas. From 4-point probe meas. Wafer specification.	ρ_{eff} extracted above slow-wave mode for the reference CPW line (at 25°C). Min./Max. $H2$ measured over the +15/-15 DC bias range.	$H2$ at $H1$=+15 dBm for the reference 2.1 mm CPW (25°C). Min./Max. $H2$ measured over the +15/-15 DC bias range.

Table 5.1: Physical description of the samples used for model validation in this chapter. Colored data in columns pertaining to material parameters were obtained from a corresponding physical measurement.

Config.	NTA [$cm^{-3}eV^{-1}$]	NTD [$cm^{-3}eV^{-1}$]	WTA [meV]	WTD [meV]
A	$2 \cdot 10^{22}$	$2 \cdot 10^{22}$	45	30
B	$8 \cdot 10^{20}$	$1.2 \cdot 10^{21}$	40	25
C	$1 \cdot 10^{22}$	$1 \cdot 10^{22}$	35	35

Table 5.2: Trap distribution parameters associated to the different configurations used to simulate the various trap-rich substrate samples of **Table 5.1**.

Model Input Parameters

In **Table 5.1**, a color-code highlights which material parameters have been extracted from complementary measurements. All values listed were those used for the small- and large-signal simulations.

In particular, the following are generally **well known parameters**:

- Material thicknesses (t_{ox}, t_{poly}, t_{sub}) are well known and controlled through well-established process steps, along with ellipsometry characterization.
- Bulk nominal resistivities (ρ_{Si}) are usually well known from either SRP data, from 4-point contact probe measurements, or from wafer specifications from the sample providers.
- Fixed interface oxide charge densities (N_{ox}) of non-trap-rich passivated samples are extracted from measurements of vertical MOS-capacitors implemented on the wafers from the observed position of the flatband voltage.
- The series R and L elements (only model input parameters not listed in **Table 5.1**, see **Chapter 4** for these inputs to the full model) of each simulated CPW line in this chapter are extracted from small-signal S-parameter of the lines. Alternatively, the R and L terms can be evaluated analytically using **[65]** knowing the physical dimensions of the CPW line and the metal conductivity. Usually, that model agrees very well with the measured S-parameter data.

The following are considered as the **fitting parameters** towards achieving model-hardware correlation in this chapter for the 19 samples of **Table 5.1**:

- The trap configuration, i.e. the acceptor and donor trap density distributions over energy. Eight out of the ten TR samples of **Table 5.1** were fitted using configuration **A** from **Table 5.2**. This distribution was deter-

mined through trial and error type of simulation fitting. More on this is described further on in **Section 5.4.1** (**pg. 183**).

- Parameter t_{trap} served to fit the simulated resistivity profile to the measured SRP data. Close to the poly/bulk interface a degradation in local resistivity is usually observed for the TR samples in this work. In the simulations, the fitting is achieved by lowering the trap density in the lower portion of the polysilicon layer while maintaining the same contamination level. More on this is discussed further on in **Section 5.5** (**pg. 186**).

Some parameters are non-critical and have little impact on the RF FoM results. They are:

- Fixed interface oxide charge densities (N_{ox}) of trap-rich passivated samples. Indeed, due to tight Fermi-level pinning in such substrates (as described in **Chapter 3**) trap-extraction techniques based on electrical stimulus (using MOS-capacitor like structures for example) is impossible. However, since the Fermi-level is tightly pinned, substrate impedance is quite insensitive to N_{ox}, and a precise value is therefore not required to simulate such substrates.
- Trap capture cross-sections. The values used for all polysilicon trap tail-states simulated in this work were given in **Table 3.3** (**pg. 81**). In **Chapter 3** it was shown that trap occupancy changes insignificantly over a time frame of a RF signal's period (sub 1 ns). Therefore, a precise value is not required to simulate such substrates at such frequencies.

Though the modelling of the 19 samples described in **Table 5.1** makes use of the finite number of material parameters shown in **Figure 5.1**, the modelling approach is not limited to these inputs. Rather, any other material stacks can be simulated using the developed TCAD-based approach. One example will be shown at the end of this chapter in **Section 5.9.2**, where the model is used to simulate the small- and large-signal behavior of gold-doped silicon substrates.

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5.2 Fixed Interface Charge

In this section, the impact of fixed interface charge density on the RF FoMs ρ_{eff} and $H2$ is studied through simulations and validation to hardware measurement data.

5.2.1 Parametric Study

Figure 5.2 plots simulation results of a HR substrate ($t_{ox} = 400$ nm, $\rho_{si} = 5$ kΩcm P-type) for various fixed interface charge density levels N_{ox}.

Figure 5.2 (a) shows the flatband voltage becoming more negative as N_{ox} increases, and a similar transition in $\rho_{eff}(V_{DC})$ can be observed in **(b)** around the flatband voltage.

With higher N_{ox} comes a more conductive PSC layer, which lowers the ρ_{eff} values as shown in **(b)**.

The trends of the large-signal model are not so straightforwardly analyzed. In particular, the minimum in the $H2(V_{DC})$ curve does not correlate to a movement in the flatband voltage, but rather remains at 0 V, though the sharpness of the transition to the lowest $H2$ value at 0 V seems to correlate to it.

It is interesting to analyze the simulation result pertaining to the N_{ox} value of 10^{13} cm^{-2}, as it produces a substrate with simultaneously low ρ_{eff}, at around 3 Ωcm, and a low $H2$ metric, at around -80 dBm. These results can be explained by analyzing **Figure 5.2 (a)**, which shows that for this substrate the Fermi level is tightly pinned due to the potential induced by the very high N_{ox} being significantly larger that that of the large-amplitude RF signal. The Fermi level is not pinned deep in the band gap, as is the case for effective trap-rich substrates, but rather is pinned close to the conduction band, making for a substrate with low ρ_{eff} and low $H2$ at the same time.

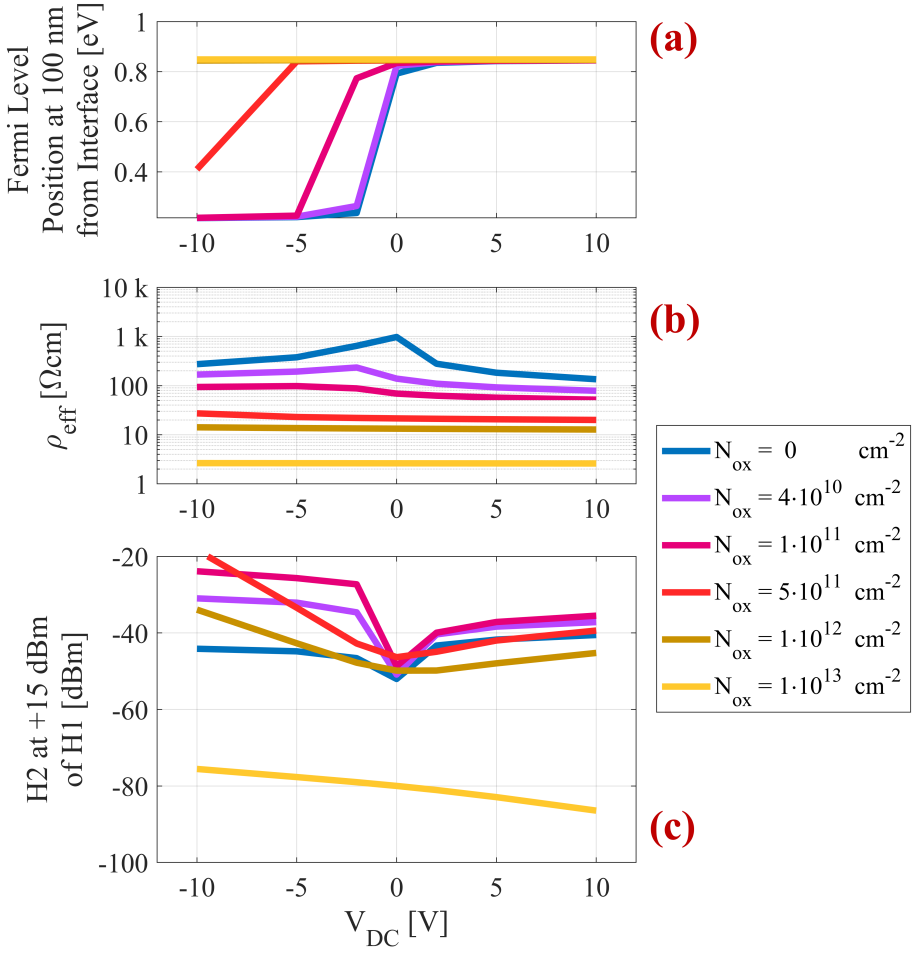


Figure 5.2: Simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC}, on a HR substrate ($\rho_{Si} = 5$ kΩcm, $t_{ox} = 400$ nm) for several fixed interface charge densities N_{ox}. **(a)** Position of the Fermi level at 100 nm below the oxide layer. **(b)** Effective resistivity, extracted above slow-wave mode (> 10 GHz, as discussed in **Section 2.1.2**). **(c)** Second harmonic level for +15 dBm of output fundamental.

5.2.2 Hardware Validation

To validate the model against measurements with various N_{ox} levels, samples **HRD1**, **P01** and **HRAl$_2$O$_3$** are chosen, as they present respectively $8 \cdot 10^{11}$ cm^{-2}, $2.1 \cdot 10^{12}$ cm^{-2} and $-5 \cdot 10^{11}$ cm^{-2}. These values were extracted from low-frequency measurements of vertical MOS capacitors on the same samples (data not shown[4]).

The measurement results along with the small- and large-signal simulation results are shown in **Figure 5.3**. All material parameters used in the simulations are given in **Table 5.1**.

Excellent hardware-model correlation is attained for these three HR samples.

Both the small- and large-signal results ρ_{eff} and $H2$ are strongly bias dependent in HR samples, as can be seen from **Figure 5.3 (b)** and **(c)**.

To help analyze these trends, a simplistic equivalent circuit and resistivity profile are shown in **Figure 5.3 (a)** for the **HRD1** sample at two different bias points, -15 V and +15 V, that correspond to states of strong inversion and strong accumulation in this substrate, respectively. In this substrate, an electron-type PSC is induced at the interface *beneath the ground lines* and *in between the signal and ground lines* of the CPW. The applied DC potential determines the carriers present *below the signal line*.

When -15 V is applied, holes are induced below the signal line, and so there is necessarily the creation of depletion zones between this region and the adjacent electron-PSC regions. Because the PSC path along the interface dominates the effective resistivity value in HR substrates, this negative bias condition yields the highest ρ_{eff}, as this path's resistance is significantly increased by these lateral depletion regions[5].

When +15 V is applied, the entire surface path at the interface is made up of electrons between the signal line and ground lines of the CPW, and ρ_{eff} is at a minimum.

[4] From the measured $C(V)$ and $G(V)$ data the substrate flatband voltage is observed. Then, the interfacial charge density can be calculated using **Equation 3.50**. Though the C(V) and G(V) data is not shown here, the flatband voltage of the **HRD1** and the **HRAl$_2$O$_3$** samples can be observed from the $\rho_{eff}(V)$ curves of **Figure 5.3 (a)** as approximately -8 V and +2 V, respectively. The flatband voltage of the **P01** sample was extracted as approximately -39 V.

[5] Actually, to be more precise, the highest ρ_{eff} value is obtained when the DC bias induces a state of depletion beneath the entire signal electrode. This can be observed in **Figure 5.2 (b)** and **Figure 5.3 (b)**, that show that ρ_{eff} is actually slightly higher near flatband voltage (close to depletion voltage in low-doped semiconductors) than at large negative bias.

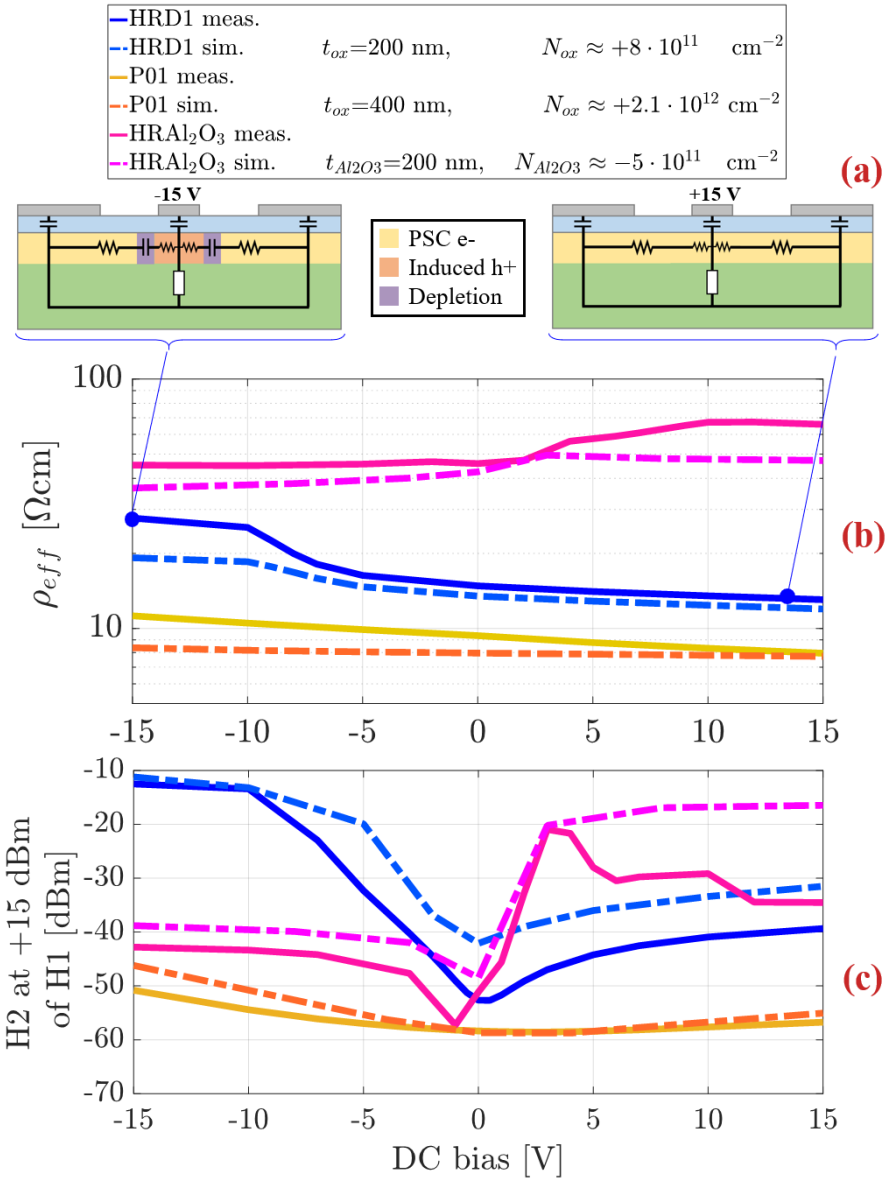


Figure 5.3: Model correlation to measured CPWs on HR substrates with various levels of fixed interface charge density. **(a)** Resistivity cross-section profile and simplistic equivalent circuit of the **HRD1** sample at ±15 V applied DC bias. **(b)** Effective resistivity, extracted above slow-wave mode (> 10 GHz, see **Section 2.1.2**). **(c)** Second harmonic level for +15 dBm of output fundamental.

Please note that the general shape of the $\rho_{eff}(V_{DC})$ curve, higher at strong negative bias and lower at strong positive bias, does not depend on the type of the HR bulk, but rather on the *sign of the interface charge*[6].

Al_2O_3/Si interfaces present *negative* fixed charge **[59, 127–130]**. Then, for sample **HRAl_2O_3**, the trend of the $\rho_{eff}(V_{DC})$ and $H2(V_{DC})$ are flipped compared to those of **HRD1**. For **HRAl_2O_3**, a hole-type PSC is present in between the signal line and the ground lines, and a positive bias is therefore required to induce the lateral depletion regions that increase ρ_{eff}.

The $\rho_{eff}(V_{DC})$ of the **P01** sample increases when the applied DC bias is lower than -40 V[7], required to induce holes, and hence lateral depletion regions, along the interface.

The HD data of the **HRD1** and **HRAl_2O_3** samples show that the substrate is less linear when the lateral depletion regions exist. Analysis of the carrier dynamics from the TCAD simulations revealed that under large-signal excitation, the lateral depletion regions are strongly modulated, being flooded with both types of carriers from either side during one half-cycle of the large-amplitude RF signal, and being over depleted on the other half-cycle, making for larger swings in the instantaneous substrate impedance under this type of bias condition.

[Redacted Confidential Content]

[6] For this reason, the type of the silicon bulk is not specified in **Figure 5.3 (a)**, and therefore any depletion regions to the bulk are not depicted, in an attempt to keep this explanation general.

[7] Measurements down to -40 V of applied bias were performed and confirm this, though that data is not shown here.

[Redacted Confidential Content]

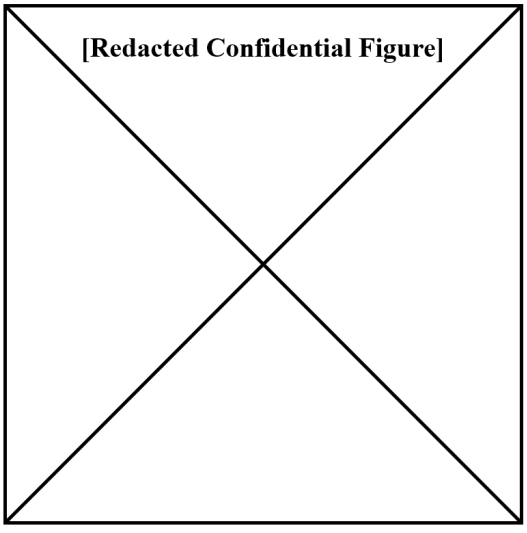


Figure 5.4: Redacted Confidential Figure.

5.3 Nominal Doping

In this section, the impact of substrate nominal doping level, and hence nominal resistivity ρ_{Si} of the bulk silicon is studied on the RF FoMs ρ_{eff} and $H2$. First, substrates without a polysilicon layer are considered, and then, similar substrates with a trap-rich layer are studied.

5.3.1 Hardware Validation without a Trap-Rich Layer

To validate the model against measurements of substrates with different nominal doping values, samples **C38** to **C42** are employed. These five samples — that were fabricated in the context of C. Roda Neve's thesis work **[117]** — are N-type with nominal resistivities ranging from 20 Ωcm to 10 kΩcm. For most of these wafers, the exact substrate nominal resistivity value was obtained from four-point probe measurements of the samples **[117]**. These values, along with all other material parameters of these substrates, are recapped in **Table 5.1**.

Figure 5.5 plots the small- and large-signal simulation and measurement results. Because the oxide thickness is quite large (t_{ox} =1 µm) and the fixed charge density is quite high ($N_{ox} \approx 9 \cdot 10^{11}$ cm^{-2}), the RF FoMs are not strongly dependent on the DC bias, and the model correlates well to the measured data in this regard.

Sample **C38** presents the lowest ρ_{eff} and the lowest $H2$ level, and these FoMs are impacted by the low bulk nominal resistivity of $\rho_{Si} = 20$ Ωcm.

However, since the N_{ox} of these samples is quite high, the PSC is therefore very strong, and seems to completely dominate the total substrate impedance and its variations to an RF large-signal for higher resistivity bulks. For this reason, samples **C40**, **C41** and **C42** have very similar RF FoMs, and this is well confirmed by the model simulations[8].

Overall, excellent correlation trends are achieved between the model and the measurements for the five samples presented[9].

[8] Though almost no differences are observed here between the 650 Ωcm (**C40**), 5 kΩcm (**C41**) and 10 kΩcm (**C42**) samples, we shall see in the next section that this is no longer the case when considering the same base resistivities while including a TR layer. This note serves to stress that there truly is a factor of 20 between the nominal dopings of these three samples, which will be confirmed in the next section (also confirmed by 4-point probe measurements, see **Table 5.1**).

[9] In terms of absolute values, ρ_{eff} deviates by a factor of approximately 1.5, and $H2$ by around 5 dB. Better correlation might be achievable by lowering slightly the interface mobility (in the PSC layer), and/or by slightly adapting the N_{ox} value, which could be slightly different for each sample (CV measurements — not shown — informed us that these five samples had similar N_{ox} values, but with a little non-uniformity over the wafers).

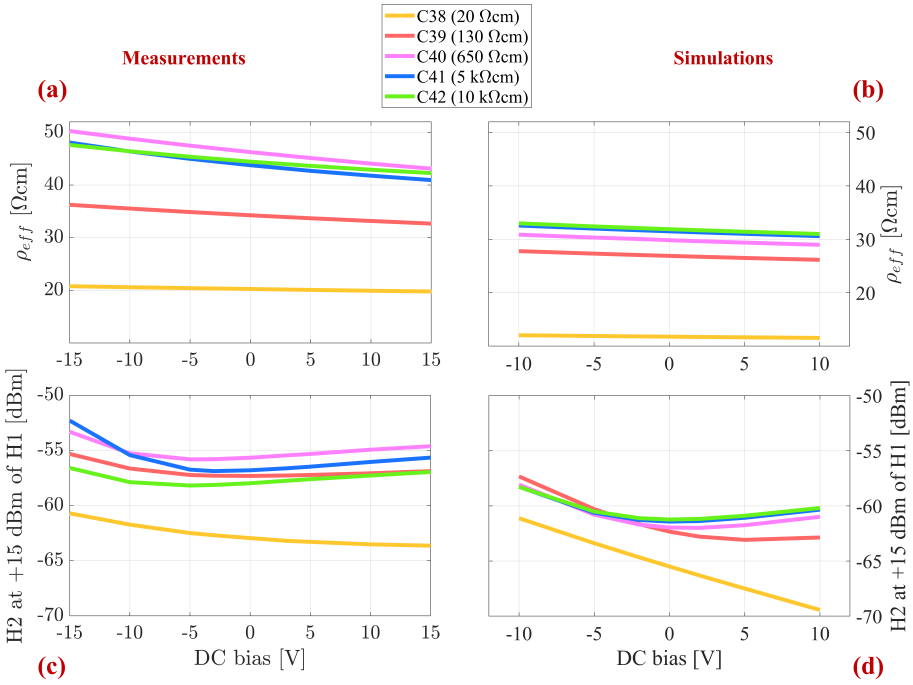


Figure 5.5: CPW line RF FoMs as a function of applied DC voltage V_{DC}, for samples of various silicon substrate resistivity, ranging from 20 Ωcm to 10 kΩcm (no trap-rich layer). **(a)** and **(b)**: measured and simulated effective resistivity, extracted above slow-wave mode. **(c)** and **(d)**: measured and simulated second harmonic level for +15 dBm of output fundamental at 900 MHz.

5.3.2 Hardware Validation with a Trap-Rich Layer

To validate the model against measurements of substrates with different nominal doping values, samples **C20** to **C24** are employed. These five samples — that were fabricated in the context of C. Roda Neve's thesis work **[117]** — are N-type with nominal resistivities ranging from 20 Ωcm to 10 kΩcm. For most of these wafers, the exact substrate nominal resistivity value was obtained from four-point probe measurements of the samples **[117]**. These values, along with all other material parameters of these substrates, are recapped in **Table 5.1**.

Figure 5.6 plots the small- and large-signal simulation and measurement results.

As described in **Section 3.4.6** (**pg. 123**), the trap-rich layer provides charge compensation for the DC voltage, and so free carrier densities are independent of V_{DC} in these substrates, which explains why the curves of **Figure 5.6 (a)** and **(b)** are flat. However, free carrier densities are not independent of an RF voltage, which varies too quickly to be compensated for by the ionization/deionization of trap states[10]. As a result, free carrier in the substrate are spatially modulated by the RF signal, and therefore substrate impedance does dependent on a large-amplitude V_{RF}, even though it does not depend on a large-amplitude V_{DC}[11].

These physical phenomena were observed in the TCAD simulations.

[Redacted Confidential Content]

[10] A parametric study on ρ_{Si} in trap-rich substrates was presented in **Section 3.4.6** (**pg. 123**) where it was explained that DC Fermi level pinning does not necessarily imply RF Fermi level pinning, and linearity is a strong function of the *existing free carriers* in a substrate, meaning that lower doped substrates are more linear.

[11] We may add that the C(V) and G(V) obtained from low-frequency measurements of vertical MOS capacitors on these same samples (not shown) are also flat.

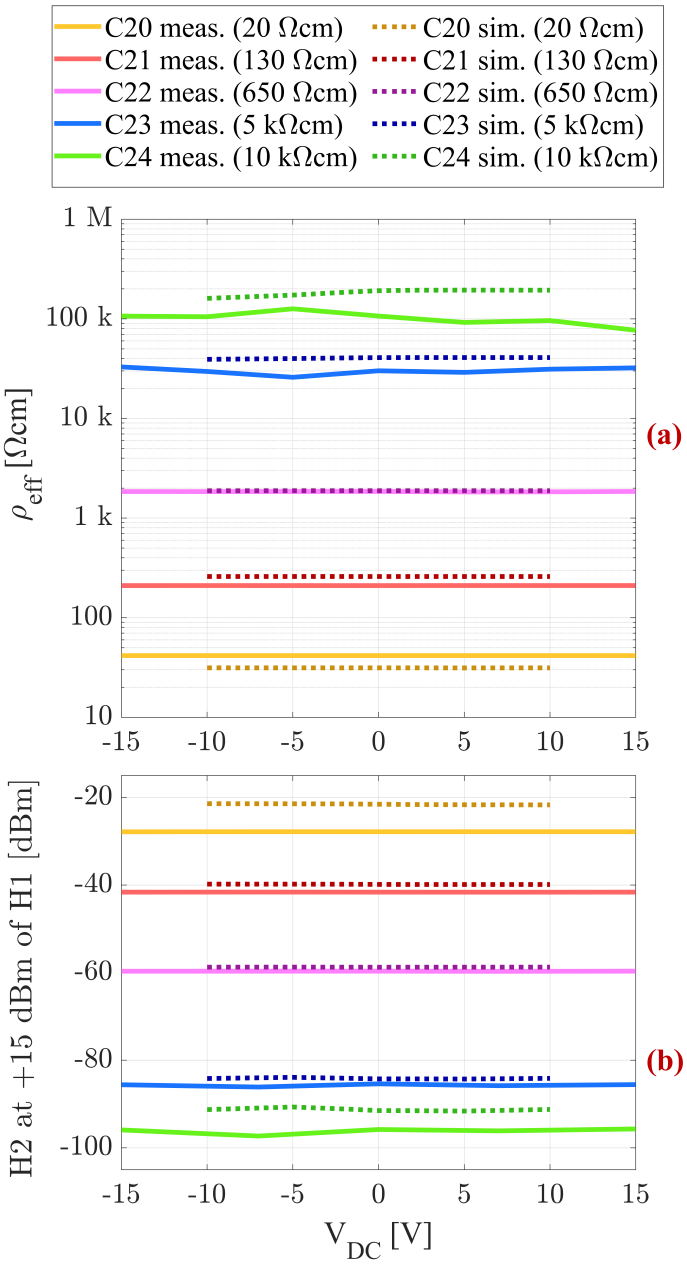


Figure 5.6: Model correlation to measured CPWs on TR substrates with various nominal bulk resistivities ρ_{Si} (N-type). **(a)** Effective resistivity, extracted above slow-wave mode. **(b)** Second harmonic level for +15 dBm of output fundamental.

Overall, **Figure 5.6** shows that good hardware-model correlation is achieved for the five trap-rich samples considered with different bulk resistivities

[Redacted Confidential Content]

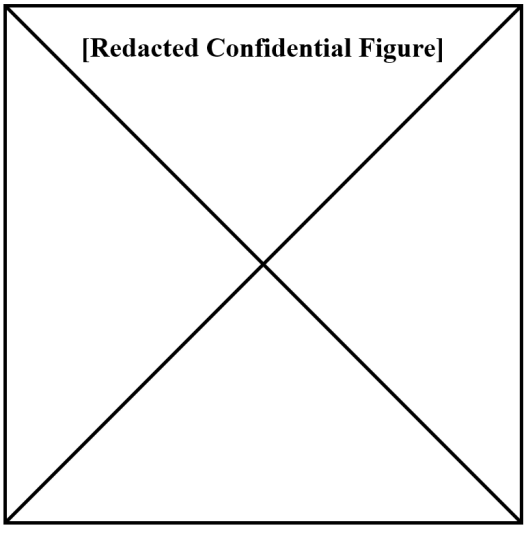


Figure 5.7: Redacted Confidential Figure.

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5.4 Trap Density

In this section, the impact of trap density in the polysilicon layer of trap-rich type substrates on the RF FoMs ρ_{eff} and $H2$ is studied through simulations and validated against measurement data.

Trap-rich samples are compared that have processes with or without a high thermal budget anneal step, expected to reduce trap-densities in the polysilicon layer **[117, 131]**.

Figure 5.8 compares images obtained from tunneling electron microscopy (TEM) of a batch of trap-rich samples having undergone various high-temperature anneal steps, up to 1100°C for 2 hours. In **(a)** the polysilicon layer can be observed without any thermal anneal having taken place. **(b)**, **(c)** and **(d)** show the progressive recrystallization of the polysilicon as the anneal temperature is increased. It should be noted that the recrystallization dynamics are heavily dependent on the fabrication process. These samples are not optimized in this regard as they are university fabricated samples, as opposed to RFeSI^{TM} commercial wafers which are engineered to maintain high RF performance even after a high thermal-budget CMOS FEOL process.

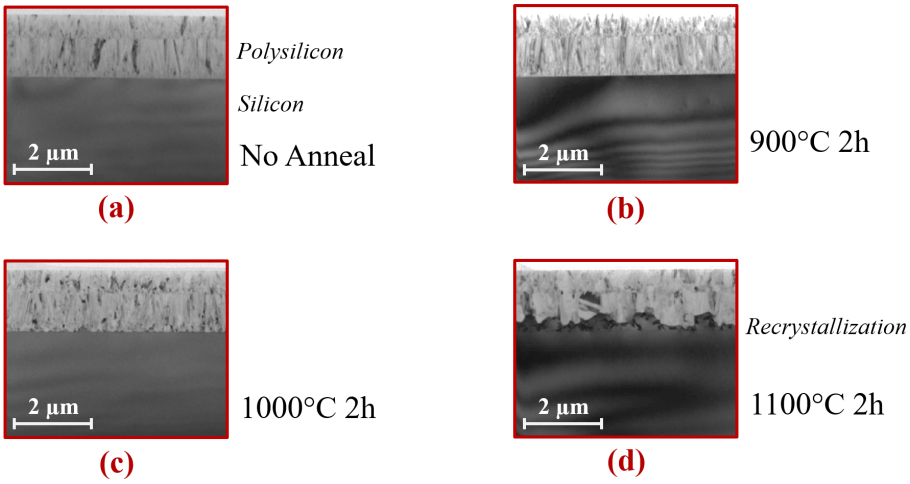


Figure 5.8: TEM images of a trap-rich sample with various thermal anneal steps.

5.4.1 About the Trap Density Distributions Used in this Work

So far, all presented samples were simulated using trap distribution parameters given by configuration **A** in **Table 5.2**. This configuration was tailored through trial and error type simulations to fit for multiple samples simultaneously: **B28**, **B67** and **B46**, that are expected to have the same polysilicon parameters due to their similar process. These trap-rich samples were processed at Soitec, though it is important to note that these samples were not taken from the commercial production line, but are part of an R&D line. Although the distributions of configuration **A** obtained in this manner provide good fitting of the model to the measurements of these three samples, when taking other material differences into account as well (mainly contamination levels and oxide thickness), we cannot affirm that configuration **A** represents the true trap distribution of these sample. It merely happens to be a distribution that fits the model to the data for small- and large-signal RF measurements of CPW lines[12].

The five samples **C20** to **C24** were fabricated in the Winfab cleanrooms at UCLouvain. Though the polysilicon thickness is different for these samples than for the three RFeSI^{TM} samples used to determine the trap parameters of configuration **A**, that configuration also provides good modelling results for samples **C20** to **C24**. Therefore, in this work, there are a total of eight TR samples whose modelling fit well to the measured data by using configuration **A**.

Sample **B45** is from a similar process as the three aforementioned RFeSI^{TM} wafers, with the addition of a strong thermal anneal step that is expected to have partially recrystallized its polysilicon and lowered the trap density **[117, 131]**. By simulation trial and error, the distribution parameters of configuration **B** from **Table 5.2** were determined to provide fairly good fitting of the model to the measurement data of **B45**.

Finally, **TRu**'s measured electrical behavior is fitted using configuration **C** from **Table 5.2**. It was also fabricated in the UCLouvain Winfab facilities, and configuration **C** corresponds to quite a high trap density, similar to configuration **A**[13].

[12] Furthermore, the trap distribution modelling used is simplistic in many ways. For example, all acceptor/donor traps are considered to be of the same *species*, i.e. they are defined as having the same carrier capture cross-sections independent of their energy location in the band gap (see **Section 3.2.2**). Physical characterization of the trap parameters of trap-rich samples is necessary in order to fuel the model in a more accurate way.

[13] To be clear, configuration **A** did not provide sufficiently accurate modelling of sample **TRu**. From that, it was required to determine configuration **C** for this sample.

5.4.2 Parametric Study

Simulations of RF substrates with varying levels of trap densities were presented in **Section 3.3.2**, and are not reprinted here. The interested reader is invited to revisit **Figure 3.7** (**pg. 97**), where deep Fermi level pinning was highlighted for increasing trap density. With more traps came a more deeply pinned Fermi level, meaning less free carriers to be modulated by the RF signal[14].

5.4.3 Hardware Validation

Based on the above discussion, samples **B28** and **B45** are selected in order to validate the model against measurements of substrates with different trap densities.

Due to a lower trap density, the RF performance of **B45** is expected to be degraded compared to that of **B28**. **Figure 5.9** shows that this is indeed the case, as the **B45** sample presents more than 5 times lower ρ_{eff} and more than 10 dB higher $H2$ as compared to **B28**, even though its bulk resistivity is roughly 3 times higher[15], as shown in the SRP data of **Figure 5.9 (a)** (see **Appendix A**). The SRP plots also confirm that similar contamination levels are present in these two samples (details about the contamination modelling and its impact on the RF FoMs are given in the next section).

The strong differences in the RF performances are then attributed to a lower trap density at the BOX interface in the trap-rich polysilicon layer. The trap distributions used for the simulations of both substrates are given by configurations **A** (for **B28**) and **B** (for **B45**) of **Table 5.2**. These trap densities are plotted in **Figure 5.9 (a)**, where weaker distributions in both acceptor and donor states are observable for the annealed sample. Using these distributions, fairly good model to hardware correlation is achieved[16].

[14] Non-linearities in the GHz range depend on the amount of free carriers in the substrate at the equilibrium DC point, as at such frequencies only *existing* substrate carriers can be modulated, as the signal is too fast for any significant thermal generation processes (see **Section 3.4 pg. 98**).

[15] Indeed, we saw in **Section 5.3** that a 3x increase in ρ_{Si} should provide an *increase* in ρ_{eff} by approximately 3x, and a *decrease* in $H2$ of around 10 dB.

[16] As discussed above, although these distributions provide good fitting for both measured RF FoMs, it should not be presumed that these distributions are therefore validated as material parameters of these samples. Indeed, there may be other trap distributions that provide model fitting of similar quality.

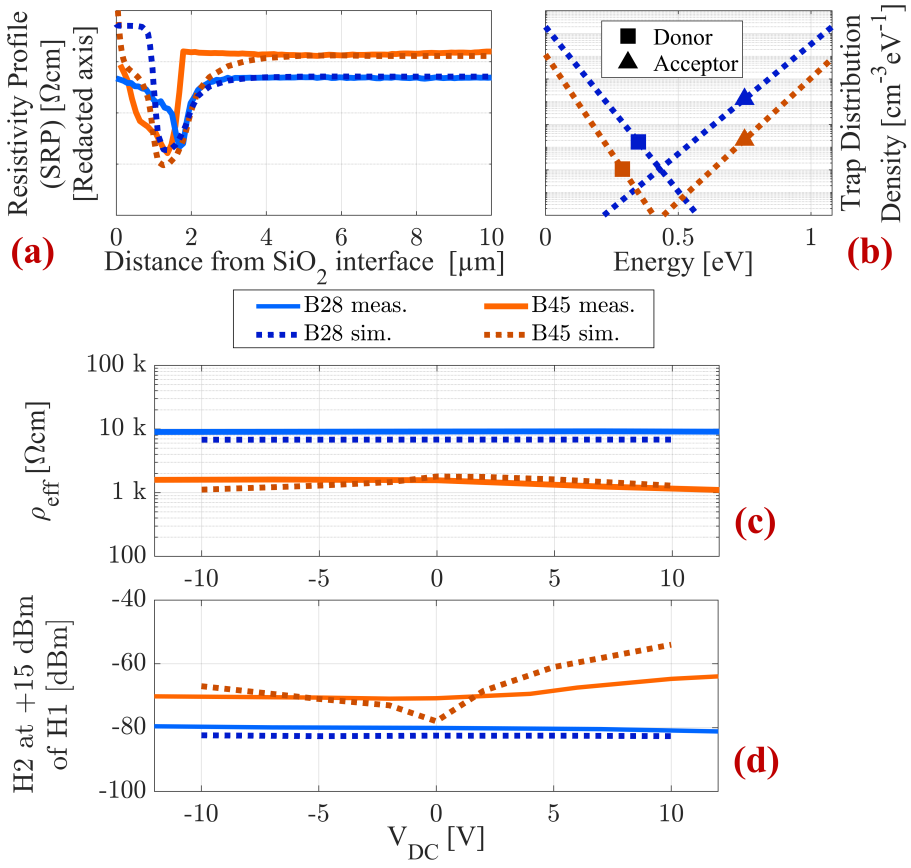


Figure 5.9: Measured and simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC}, for several trap-rich substrates with various trap density distributions. **(a)** Vertical resistivity profile from BOX interface: measured and simulated SRP (see **Appendix A**). SRP measurements courtesy of Soitec. **(b)** Trap energy distributions. **(c)** Effective resistivity, extracted above slow-wave mode. **(d)** Second harmonic level for +15 dBm of output fundamental.

5.5 Polysilicon Contamination

In this section, the impact of polysilicon contamination level in trap-rich type substrates is studied on the RF FoMs ρ_{eff} and $H2$.

Polysilicon is made up of grains of single crystal silicon that are randomly oriented relative to each other. Within the single crystal grains, the diffusion characteristics are similar to those of bulk crystalline silicon. In the grain boundaries however, diffusion can proceed at up to 100 times the rate of diffusion within the crystal grains [132]. The effective diffusion in polysilicon over lengths equivalent to multiple grain sizes is then dominated by the grain boundary effects. These grain sizes range from 0.1 to 20 µm and depend on the deposition conditions, thickness, underlying material film, and the subsequent thermal anneal steps [132].

Because polysilicon used in trap-rich substrates is undoped, its electrical properties may be non-negligibly impacted by impurity contamination. And, because the diffusion is higher in the polysilicon trap-rich layer than in the silicon bulk, impurities introduced at the interfaces will tend to stay within the polysilicon layer rather than diffuse out into the bulk.

5.5.1 Parametric Study

Figure 5.10 plots simulation results of a TR substrate ($t_{ox} = 400$ nm, $\rho_{si} = 5$ kΩcm P-type) for various polysilicon (P-type) contamination levels $N_{A,poly}$ defined over the entire polysilicon thickness t_{poly}. In these simulations, t_{poly} is set to 2 µm, while traps are defined using configuration **A** of Table 5.2 over a depth of $t_{trap} = 1$ µm (so as to take into account lower trap density at the polysilicon/silicon interface, as described in Section 5.1).

Figure 5.10 (a) shows how the contamination affect the resistivity profile in the semiconductors, while (b) and (c) plot the RF FoMs as a function of DC bias. Both RF FoMs are bias independent, as DC biases over a large range are compensated for by only a small shift in the equilibrium Fermi level by ionized traps. This was also the case in Section 5.3.2 where TR substrates of various nominal silicon doping levels were considered. The results presented here are similar in trends, as with higher contamination levels comes a larger amount of free carriers in the substrate that can be modulated by an RF voltage, and for this reason the harmonic distortion levels in Figure 5.10 (c) are a strong function of $N_{A,poly}$.

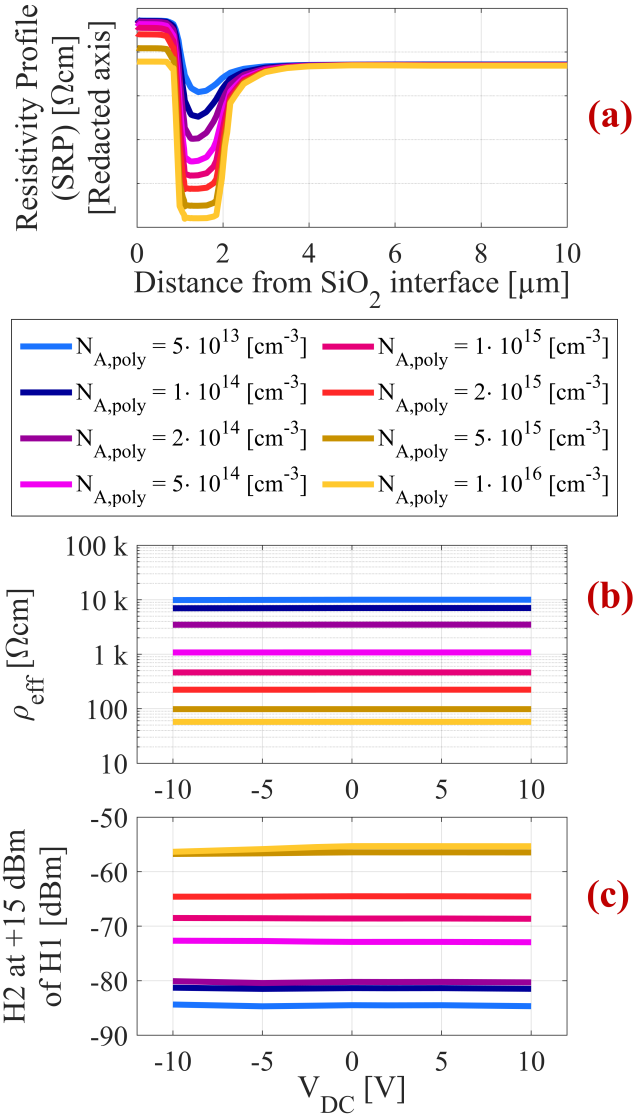


Figure 5.10: Simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC}, for several trap-rich substrates with various polysilicon (P-type) contamination levels. **(a)** Vertical resistivity profile from BOX interface (simulated SRP see **Appendix A**). **(b)** Effective resistivity, extracted above slow-wave mode. **(c)** Second harmonic level for +15 dBm of output fundamental.

5.5.2 Hardware Validation

To validate the model against measurements with various contamination levels $N_{A,poly}$, samples **B28** and **B46** are chosen.

The measurement results along with the small- and large-signal simulations are shown in **Figure 5.11**. For both samples t_{poly} is 2 µm and t_{trap} is set to 1 µm. All material parameters used in the simulations are given in **Table 5.1**. That table lists the contamination level in the **B46** sample as $7 \cdot 10^{14}$ cm^{-3}. SIMS measurements on that wafer (not shown) report Boron contamination in the range of $8 \cdot 10^{14}$ to $4 \cdot 10^{15}$ cm^{-3} in the polysilicon trap-rich layer. To fit the SRP data, $7 \cdot 10^{14}$ cm^{-3} was determined in the presented simulations. The discrepancy between SIMS data and SRP data is likely due to inaccuracies in the mobility model of polysilicon, i.e. the mobility in the polysilicon layer could be modified such that a contamination value of $4 \cdot 10^{15}$ cm^{-3} provides a resistivity profile to fit the SRP. In this work, adapting the polysilicon mobility models was not considered and the TCAD Atlas default models were used, though we note here that for a more accurate description effort should be made in this regard[17,18].

For these two samples, good fitting is achieved in terms of SRP, and both RF FoMs $\rho_{eff}(V)$ and $H2(V)$. The impact of contamination of the order of $1 \cdot 10^{15}$ cm^{-3} is a tenfold reduction in $\rho_{eff}(V)$ and a 10 dB decrease in linearity, which the model predicts well for the given set of material parameters considered.

[17] **B46** is the only sample for which SIMS data is available, as the contamination in all other samples was in the noise floor of the SIMS measurements. Therefore, all contamination levels listed in **Table 5.1** obtained from SRP also depend on the mobility models used in polysilicon, and are likely slightly wrong valued.

[18] Because the mobility need only be adapted by a factor of 2 to reconcile SRP and SIMS data (both of which are available only for a single sample), the impact on the results of the simulations should not be very large. In particular in this work overall physical trends are sought, rather than close fitting to within a few dB.

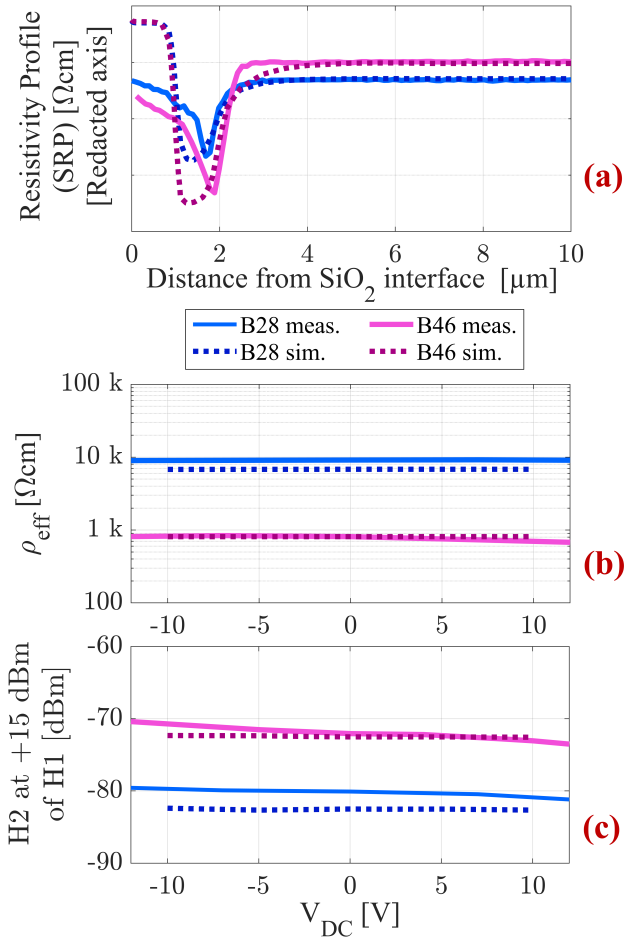


Figure 5.11: Measured and simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC}, for several trap-rich substrates with various polysilicon contamination levels (P-type). **(a)** Vertical resistivity profile from BOX interface: measured and simulated SRP (see **Appendix A**). SRP measurements courtesy of Soitec. **(b)** Effective resistivity, extracted above slow-wave mode. **(c)** Second harmonic level for +15 dBm of output fundamental.

5.6 Temperature

In this section, the RF substrate performance is evaluated over temperature and compared to the model, from 25 °C to 190 °C.

In semiconductors in general, temperature plays a strong effect, notably through mobility degradation due to increased phonon scattering at higher temperatures, and also through the strong dependence of the intrinsic carrier density n_i with temperature. This latter term has an especially large impact in low-doped semiconductors as it will determine the resistivity of such materials over a significant part of the temperature range considered in this work.

For these reasons, temperature is an excellent parameter to vary towards validating the physical modelling.

Furthermore, RF substrate modelling up to such temperatures is relevant, as some applications call for a wide range of operating temperatures, such as automotive applications, which are required to operate down to -40 °C and up to 125 °C.

5.6.1 Hardware Validation: High-Resistivity Substrate

To validate the model over temperature for a typical HR substrate, sample **HRD2** was measured and simulated from 25 °C to 190 °C under both small- and large-signal excitations. During the on-wafer measurements, the temperature of the samples was controlled by a Temptronics thermal 8-in chuck tool.

The results are plotted in **Figure 5.12**, that show a weak dependency of the RF FoMs on temperature. This is explained by the fact that the PSC interface region dominates the substrate impedance, meaning that increasing carrier concentration in the bulk has negligible effect on the overall impedance through the substrate.

The effective resistivity is approximately doubled from 25 °C to 190 °C, in both the measurements and the simulations, and this is attributed to a decrease in free carrier mobility. In the PSC regions this mobility degradation is dampened by carrier-carrier scattering due to large carrier densities in these regions. Taking carrier-carrier scattering into account, the observed twofold increase in ρ_{eff} is in good agreement with a twofold decrease in carrier mobility from 25 °C to 190 °C given by Arora's models and measurements **[133]**, as well as by Silvaco

ATLAS mobility models [61][19].

With a twofold increase in ρ_{eff} from 25 °C to 190 °C comes a 3-4 dB decrease in $H2$ and the same general $H2(V_{DC})$ shape[20].

Overall, the model correlates well to the small-signal and HD measurements of a typical HR sample over the considered temperature range.

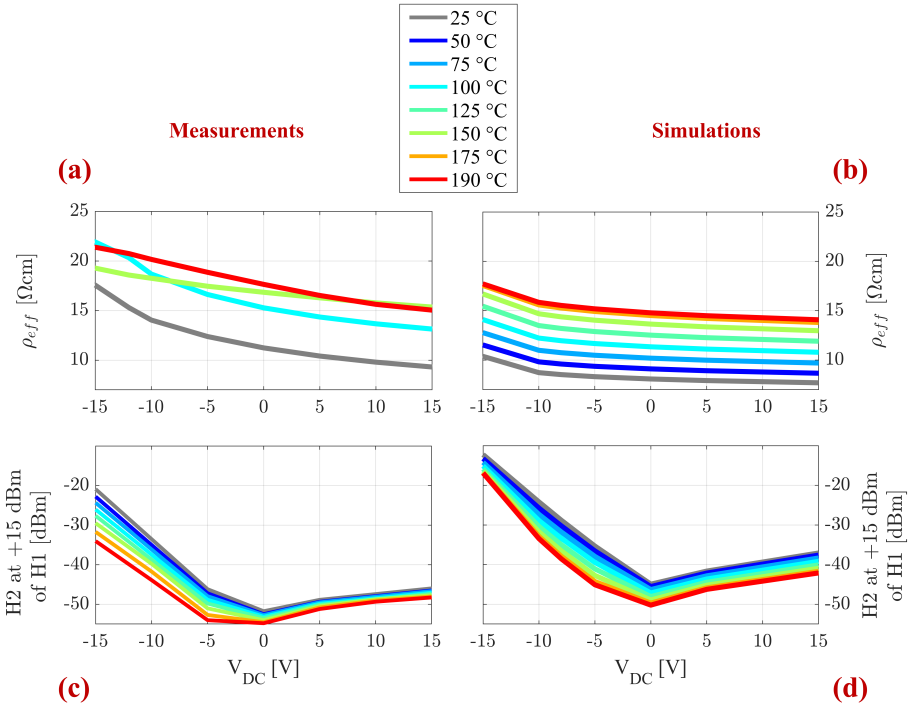


Figure 5.12: CPW line RF FoMs as a function of applied DC voltage V_{DC}, for sample **HRD2** at various temperatures. **(a)** and **(b)**: measured and simulated effective resistivity, extracted above slow-wave mode. **(c)** and **(d)**: measured and simulated second harmonic level for +15 dBm of output fundamental at 900 MHz.

[19]The electron mobility values in low-carrier density silicon regions at 25 °C to 190 °C are approximately equal to 1400 and 500 $cm^2V^{-1}s^{-1}$, respectively. In a silicon region in which the electron density is $5 \cdot 10^{17}$ cm^{-3}, carrier-carrier scattering further limits mobility values, that are approximately equal to 450 and 220 $cm^2V^{-1}s^{-1}$ at 25 °C and 190 °C, respectively [133].

[20]The measurements in fact show a larger variation at strong negative bias of approximately 10 dB from 25 °C to 190 °C. This discrepancy with the model at this bias point is unexplained.

5.6.2 Hardware Validation: Trap-Rich Substrate

To validate the model over temperature for typical TR substrates, samples **B28**, **B46** and **B67** were measured and simulated in both small- and large-signal conditions from 25 °C to 190 °C.

Figure 5.13 plots the $\rho_{eff}(V_{DC})$ and $H2(V_{DC})$ curves of sample **B28** at several temperature points. Sample **B28** is seen to be highly temperature dependent, especially above 100 °C, which is approximately the temperature at which the intrinsic carrier concentration becomes higher than the sample's nominal doping level (ρ_{Si} = 5 kΩcm). Then, the substrate's impedance rapidly degrades with increasing temperature, and ρ_{eff} falls to around 190 Ωcm at 190 °C. As ρ_{eff} degrades, the non-linear substrate impedance has a stronger impact on the 50 Ω CPW line, and, with more free carriers in the substrate, substrate impedance modulations at RF frequencies become larger in amplitude. For these reasons, $H2$ of the eSI80^{TM} sample **B28** drops from -80 dBm at 25 °C to -50 dBm at 190 °C[21]. Excellent model to hardware correlation is achieved for this sample over temperature.

Figure 5.14 plots the RF FoMs as a function of temperature at 0 V DC bias for all samples measured up to 190 °C: sample **HRD2** from the previous section and three RFeSI^{TM} samples.

The RF FoMs of **B28** and **B46**[22] do not strongly dependent on temperature below 75-100 °C, due to the nominal doping level (and/or contamination level) remaining higher than the thermally generated intrinsic carrier density. **B67** on the other hand shows temperature dependence over the entire measurement range, due to its extremely low nominal doping level ($\rho_{Si} \approx 40$ kΩcm) and low contamination.

At 190 °C, the intrinsic carrier concentration in the bulk silicon dominates the effective resistivity and non-linear substrate response. For these reasons, the three RFeSI^{TM} samples present almost identical RF FoM values, with ρ_{eff} and $H2$ at approximately 190 Ωcm and -50 dBm, respectively.

[21] Because the value of the bulk carrier density (and hence bulk resistivity) below the polysilicon trap-rich layer explains well the trends shown here over temperature, the interested reader is invited to revisit **Figure 5.6** (**pg. 179**) and compare the RF FoM trends, as in that figure, TR-type samples with various bulk nominal resistivities were compared (at 25 °C). The trends in both RF FoMs are quite similar, and for the same reasons.

[22] Sample **B46** is the annealed RFeSI^{TM} substrate that presents lower trap density distributions than the other RFeSI^{TM} samples considered in this work, and was discussed previously in **Section 5.4.3**.

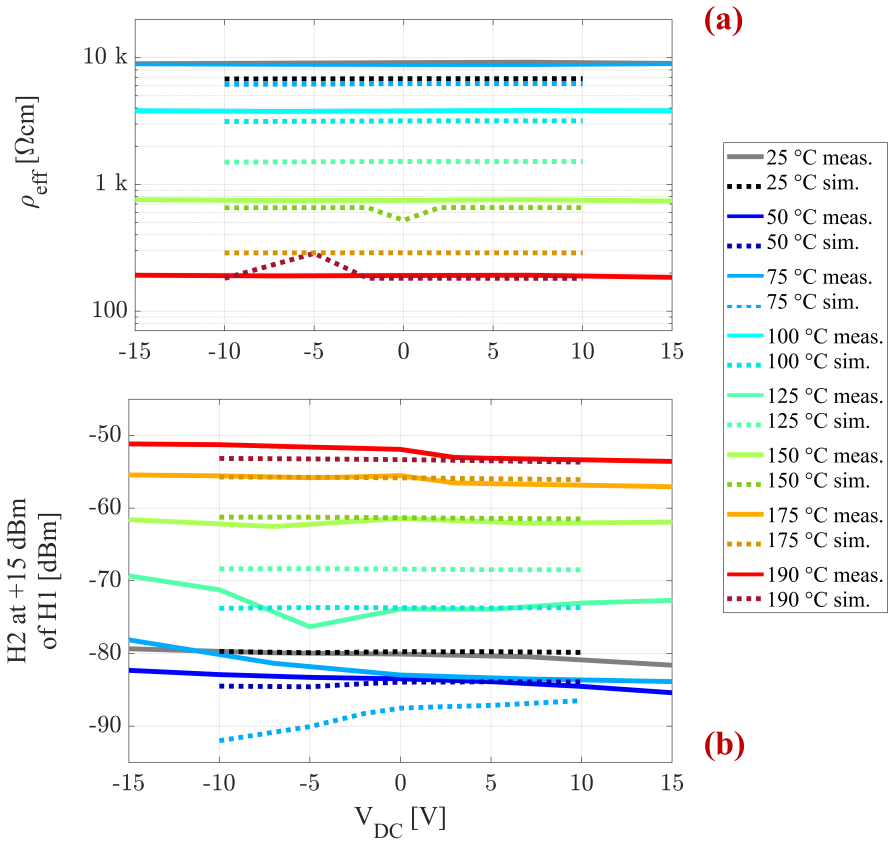


Figure 5.13: CPW line RF FoMs as a function of applied DC voltage V_{DC}, for sample **B28** at various temperatures. **(a)** Measured and simulated effective resistivity, extracted above slow-wave mode. **(b)** Measured and simulated second harmonic level for +15 dBm of output fundamental at 900 MHz.

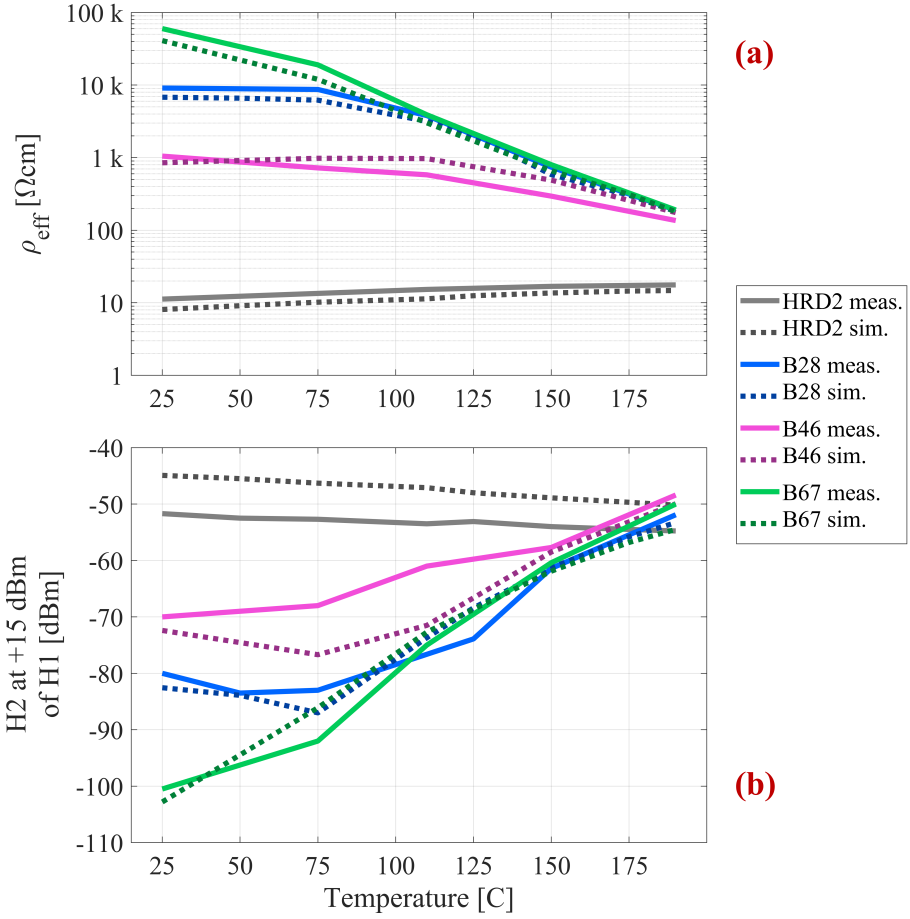


Figure 5.14: CPW line RF FoMs as a function of temperature at $V_{DC} = 0$ V. **(a)** Measured and simulated effective resistivity, extracted above slow-wave mode. **(b)** Measured and simulated second harmonic level for +15 dBm of output fundamental at 900 MHz.

Figure 5.14 shows good model to hardware correlation over temperature for the considered HR and TR samples. The model captures well the overall trends of both the small-signal and large-signal FoMs.

5.7 CPW Line Geometry

In this section, the impact of CPW line geometry on the RF FoMs ρ_{eff} and $H2$ is studied through simulations and validated against measurement data.

The section will be divided into two parts. In the first part (**Section 5.7.1**), different CPW line cross-sectional dimensions are considered. The central conductor width W_C and spacing to ground lines S are varied, while maintaining a characteristic impedance close to 50 Ω. The W_C/S pairs considered here for ρ_{eff} and $H2$ model to hardware correlation are 11/8, 26/12, 45/25 and 95/50, where all numbers are given in microns. The reader is invited to revisit **Figure 2.6** of **Section 2.1.3** (**pg. 42**) where $\rho_{eff}(S)$ was plotted for several HR and TR samples, and the trends where explained based on the vertical resistivity profile $\rho(y)$ in the substrate beneath the CPW lines of various dimensions.

In the second part (**Section 5.7.2**), several CPW line lengths are considered, from 1.0 mm to 8.0 mm for the reference W_C/S cross-sectional dimensions of 26/12.

5.7.1 Width and Spacing

To validate the model over cross-sectional CPW dimensions (W_C/S) samples **HRD1**, **HRAl$_2$O$_3$** and **TRu** are measured and simulated in both small- and large-signal conditions using several CPW lines.

Four CPWs of different cross-sectional sizes will be considered, each named as a unique *set* of dimensions as:

- Set B: $W_C/S = 11/8$ [µm]/[µm],
- Set C: $W_C/S = 26/12$ [µm]/[µm],
- Set D: $W_C/S = 45/25$ [µm]/[µm],
- Set E: $W_C/S = 95/50$ [µm]/[µm].

HR Validation Over W_C and S

Figure 5.15 plots the measured and simulated $\rho_{eff}(VDC)$ and $H2(VDC)$ curves of sample **HRD1**, while **Figure 5.15** plots the curves pertaining to sample **HRAl$_2$O$_3$**.

As discussed in **Section 2.1.3** (see **pg. 42**), the presence of a conductive PSC layer at the dielectric/silicon interface has the effect of increasing the value of ρ_{eff} for increasing W_C and S dimensions due to increased overall substrate impedance. These trends are well observed in **Figures 5.15 and 5.16** for both considered HR samples. In terms of $H2$, the overall trends are a reduction of $H2$

as W_C and S increase, and can be interpreted as being correlated to an increase in ρ_{eff}. In all cases the model fits well to the measured data in terms of trends and also of absolute values of the RF FoMs for the considered cross-sectional CPW dimensions.

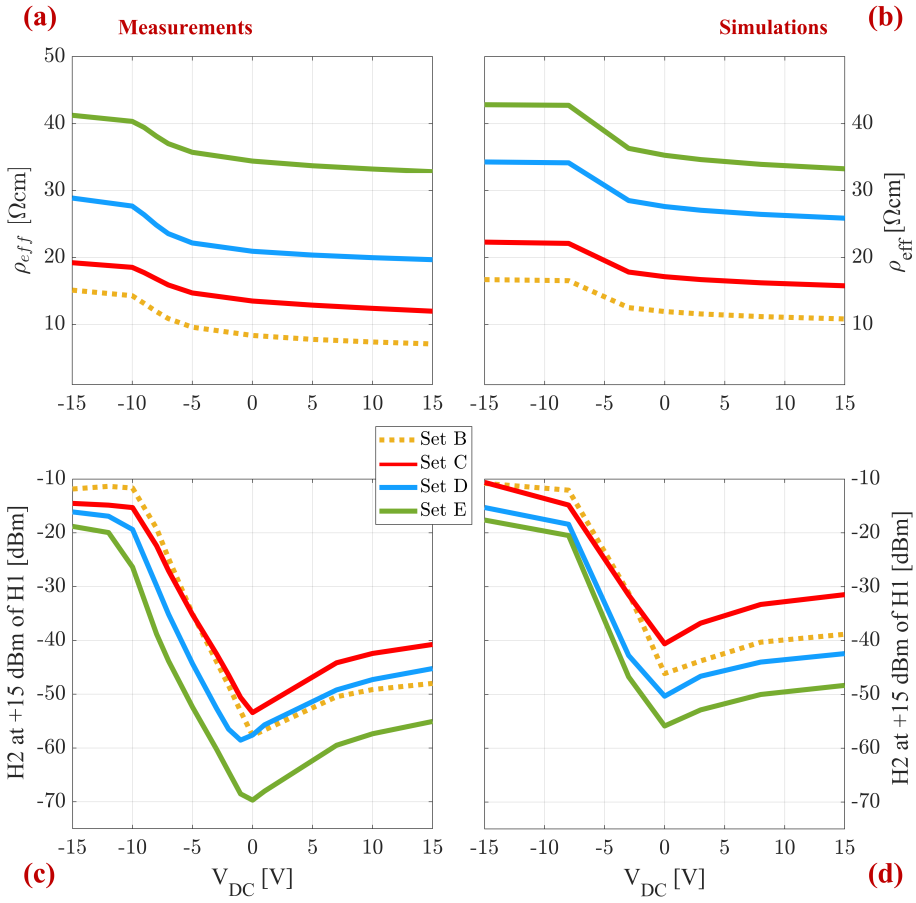


Figure 5.15: RF FoMs as a function of applied DC voltage V_{DC}, for sample **HRD1**, obtained from four 50 Ω CPW lines of different cross-sectional geometry W_C and S. **(a)** and **(b)**: measured and simulated effective resistivity, extracted above slow-wave mode. **(c)** and **(d)**: measured and simulated second harmonic level for +15 dBm of output fundamental at 900 MHz.

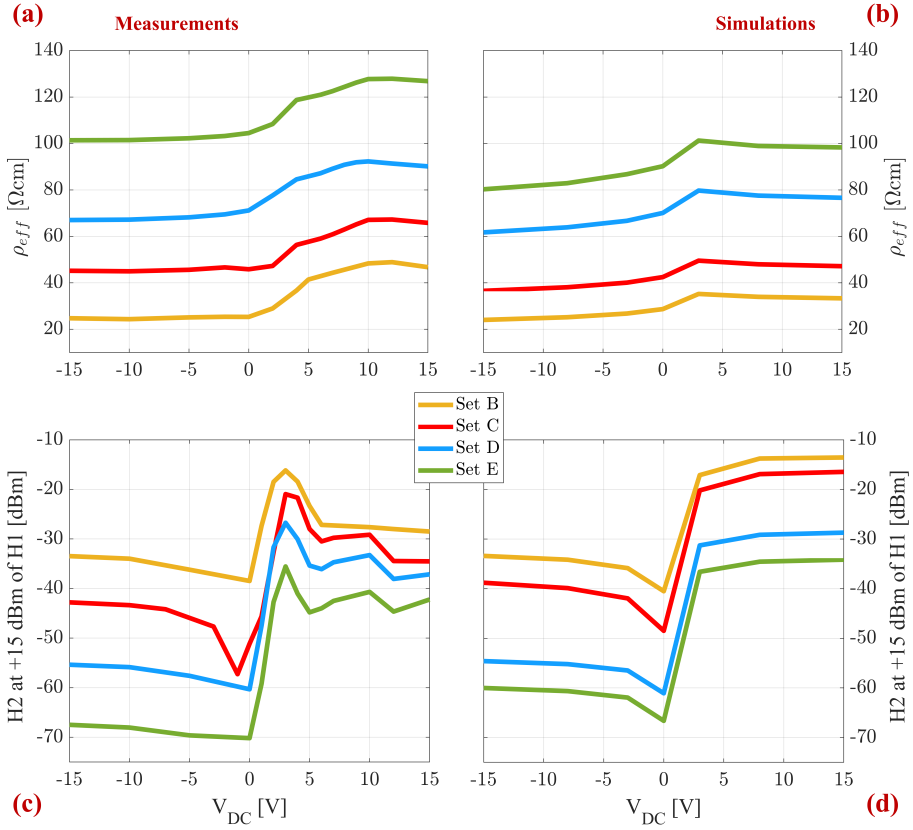


Figure 5.16: RF FoMs as a function of applied DC voltage V_{DC}, for sample **HRAl$_2$O$_3$**, obtained from four 50 Ω CPW lines of different cross-sectional geometry W_C and S. **(a)** and **(b)**: measured and simulated effective resistivity, extracted above slow-wave mode. **(c)** and **(d)**: measured and simulated second harmonic level for +15 dBm of output fundamental at 900 MHz.

TR Validation Over W_C and S

Figure 5.17 plots the measured and simulated $\rho_{eff}(VDC)$ and $H2(VDC)$ curves of sample **TRu**.

The same global trends are present for the RF FoMs of sample **TRu** as were for the HR substrates: lower ρ_{eff} and higher $H2$ for smaller W_C and S dimensions. Based on the discussion of **Section 2.1.3** (see **pg. 42**) this would suggest that for this **TRu** sample the local resistivity in the semiconductor is

lower at the dielectric interface than deeper in the bulk. This was indeed verified in the simulated substrate by analyzing the TCAD carrier-concentration profiles.

Overall, thanks to the fitting of **TRu**'s trap parameters, given as configuration **C** in **Table 5.2**, good agreement between the model and the measured data is achieved over the considered CPW cross-sectional dimensions. Both the fourfold increase in ρ_{eff} and the 20 dB decrease in $H2$ are well captured by the model as W_C/S increase from $11/8$ [µm]/[µm] to $95/50$ [µm]/[µm].

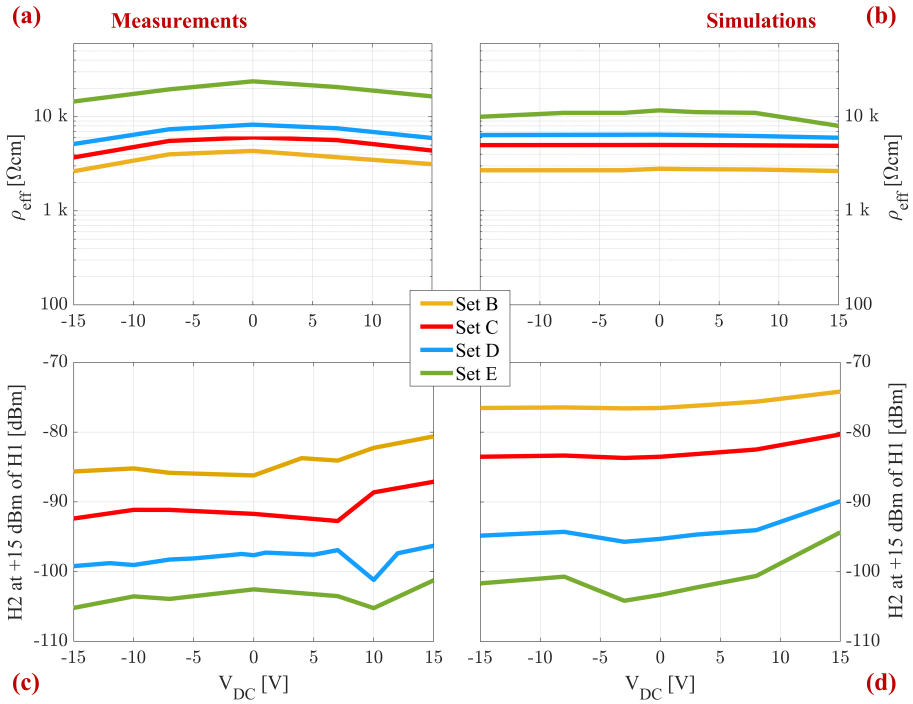


Figure 5.17: RF FoMs as a function of applied DC voltage V_{DC}, for sample **TRu**, obtained from four 50 Ω CPW lines of different cross-sectional geometry W_C and S. **(a)** and **(b)**: measured and simulated effective resistivity, extracted above slow-wave mode. **(c)** and **(d)**: measured and simulated second harmonic level for +15 dBm of output fundamental at 900 MHz.

5.7.2 Line Length

To validate the model over CPW line length L samples **HRD2**, **B28** and **B67** are measured and simulated in both small- and large-signal conditions using several lines from set C ($W_C/S = 26/12$ µm/µm)[23].

For each considered sample the second harmonic is measured on up to 5 CPW lines with lengths ranging from 1240 µm to 8000 µm. The measured and simulated $H2$, taken at 0 V DC bias, are plotted in **Figure 5.18** for the three samples[24].

The $H2(L)$ results of the large-signal modelling are superimposed upon the same graph, which illustrates the model's ability to accurately capture the $H2$ trends over CPW line length for both HR and TR samples.

For **HRD2** the simulated $H2(L)$ curve is replotted with an offset of -9.0 dB to highlight that the simulated trend correlates well to the measured trend. For the **HRD2** sample the material parameters were chosen to fit best the $H2(V_{DC}, T)$ data presented in **Figure 5.12** for the 2.1 mm-long CPW line of set C. Though fairly good *overall fitting* was achieved in both temperature and bias voltage, the $V_{DC} = 0$ point at $T = 25°C$ presented an approximately 9 dB difference between the model and the measured data.

For **B28** the simulated $H2(L)$ curve is replotted with an offset of +2.7 dB to highlight that the simulated trend correlates well to the measured trend[25].

[23] Note that different samples from the previous section are used because different RF masks were used to pattern either CPWs of many lengths (L), or CPWs of many cross-sections (W_C/S), i.e. no mask was drawn in which there are simultaneously CPW lines of many different lengths as well as CPW lines of many different widths.

[24] The ρ_{eff} parameter is not plotted as it is independent of line length for a given set, as the cross-sectional dimensions determine the *lineic* G and C parameters of the line. The $\rho_{eff}(V_{DC})$ model to hardware correlations have already been performed for these three samples, and are not reprinted in this section.

[25] The fitting of the **B28** sample's material parameters was performed dependently on the material parameter fitting of samples **B45**, **B46** and **B67**, during which model to hardware discrepancies in $H2$ of up to a few dB was tolerated for all four samples, see **Figures 5.9 and 5.11** (as well as **Figure 5.22** further on).

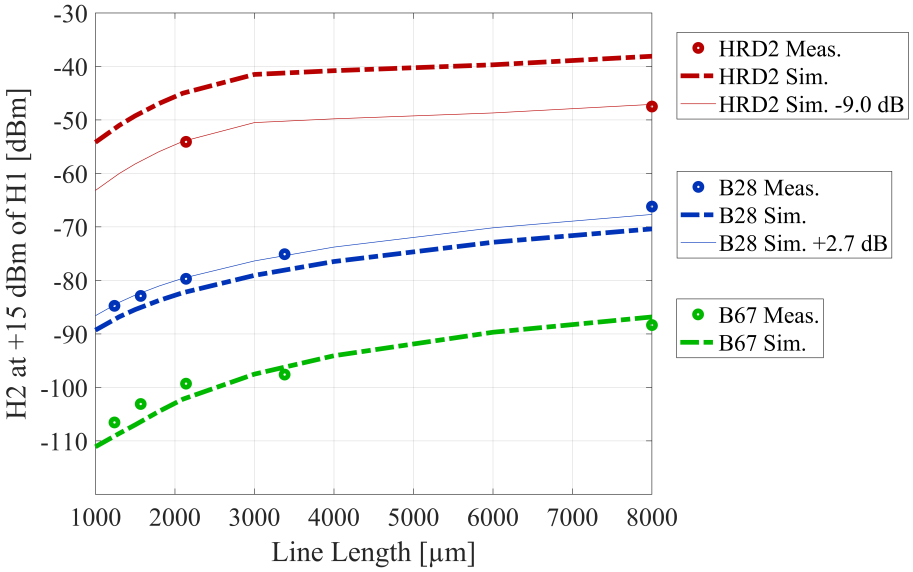


Figure 5.18: Second harmonic power level $H2$ at +15 dBm of $H1$ (at 900 MHz at 0 V DC bias) at the output of CPW lines of various lengths on three samples. All lines are described by $W_C = 26$ µm and $S = 12$ µm.

5.8 Fundamental Frequency

To validate the model over a range of fundamental frequencies, samples **HRD1**, **P01**, **B28** and **B67** are measured under large-signal conditions up to +25 dBm input power using the following fundamental excitation frequencies that span over two decades: 50 MHz, 250 MHz, 900 MHz, 2.5 GHz and 5.4 GHz.

The HD measurements at each one of these five frequencies requires a dedicated set-up with filters and a power amplifier tailored to each fundamental and its harmonic frequencies (see HD measurement set-up in **Appendix B**).

The impact of fundamental frequency was already discussed in **Chapter 3 Section 3.4.5** (see **Figure 3.13 pg. 117**), where it was shown that dielectric on semiconductor substrates are more linear:

- At high frequency due to substrate being less modulated by large-amplitude signals due to the finite inertia of carriers.
- At low frequency due to the (linear) series dielectric impedance dominating the overall substrate impedance (slow-wave mode in a CPW).

The take-away conclusion from **Section 3.4.5** was that substrate-induced harmonic distortion levels in such substrates depend on frequency and are maximum just after the transition from the slow-wave mode f_{SW}, as below it the (linear) dielectric impedance dominates while above it substrate variations weaken due to finite carrier inertia.

5.8.1 Hardware Validation

Figure 5.19 plots the measured and simulated $H2(V_{DC})$ curves at the five considered fundamental frequencies for sample **HRD1**, at an output fundamental power of $H1 = +15$ dBm. The 50 MHz curve is 10 to 25 dB lower than the 5.4 GHz curve over the whole DC range, and the model correlates well in trends to the measured data. In particular, the 250 MHz to 5.4 GHz data are quite close in magnitude, which is due to the fact that the transition frequency out of the slow-wave mode is around $f_{SW} \approx 3$ GHz in this sample ($H2(f_0)$ is flattest around the f_{SW}, see **Figure 3.13 pg. 117**).

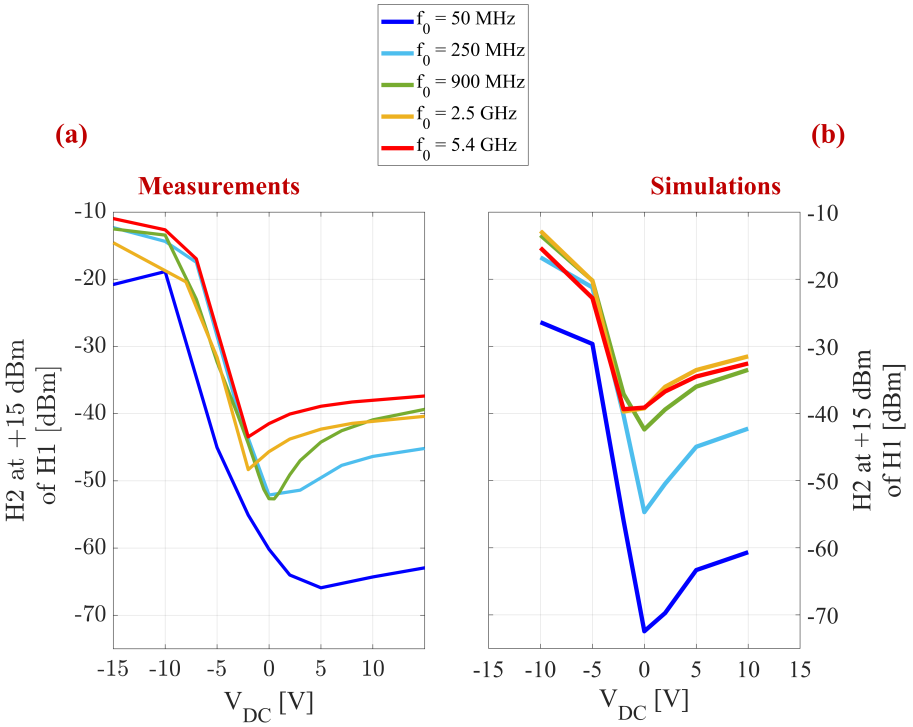


Figure 5.19: CPW line harmonic distortion as a function of applied DC voltage V_{DC}, for sample **HRD1** at various fundamental frequencies f_0. The second harmonic power level is extracted at +15 dBm of fundamental output power $H1$. **(a)** On-wafer measurements. **(b)** Large-signal simulations.

Figure 5.20 plots the measured and simulated $H2(V_{DC})$ curves at the five considered fundamental frequencies for sample **B28**. This TR sample's slow-wave transition frequency is around $f_{SW} \approx 5$ MHz, and so over the measured fundamental frequency range the harmonic levels of **B28** monotonically decrease for increasing f_0. Excellent model to hardware correlation is achieved for this sample, whose material properties were calibrated in the TCAD environment such that the 900 MHz simulations fit to the on-wafer measurements. The 30 dB reduction in $H2$ from 50 MHz to 5.4 GHz is well captured by the model.

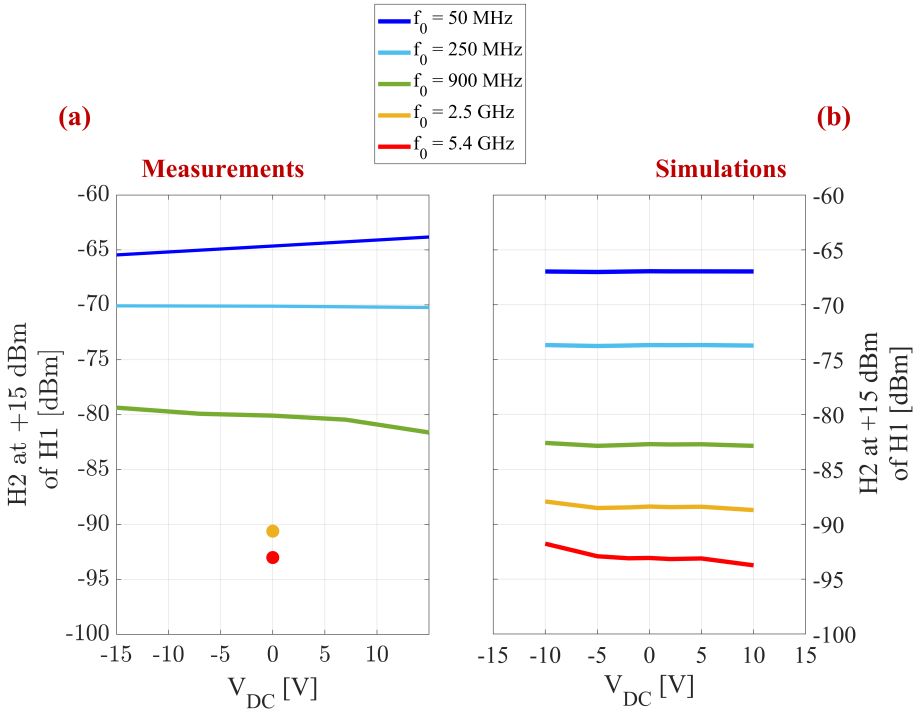


Figure 5.20: CPW line harmonic distortion as a function of applied DC voltage V_{DC}, for sample **B28** at various fundamental frequencies f_0. The second harmonic power level is extracted at +15 dBm of fundamental output power $H1$. **(a)** On-wafer measurements (not performed over a DC voltage sweep at 2.5 GHz or at 5.4 GHz). **(b)** Large-signal simulations.

Figure 5.21 plots the $H2$ level extracted at a given DC bias point as a function of fundamental excitation frequency f_0 for the four considered samples.

The results pertaining to sample **HRD1** are plotted in **Figure 5.21 (a)** at three DC bias points. The model's trends correlate well to the measured data, and simulations at frequencies above the highest measurement fundamental reveal the downward trend in harmonics due to finite carrier inertia starting from approximately 5 GHz.

Figure 5.21 (b) plots the data pertaining to sample **P01**, which is also a HR sample but with a very high interfacial charge density of $N_{ox} \approx 2.1 \cdot 10^{12}$ cm^{-2}. This high N_{ox} results in a significantly lower substrate effective resistivity as for sample **HRD1** and for a significantly higher slow-wave mode transition

frequency, which is in the range of $f_{SW} \approx 15$ GHz for sample **P01**. Then, $H2(f_0)$ is monotonically increasing for this HR substrate, as depicted in **Figure 5.21 (b)**, due to the reduction in the series dielectric impedance (with increasing frequency) that is responsible for linearizing the overall substrate impedance below f_{SW}. The model's trends correlate well to the measured data in this respect. Over the measured frequency range, the power of the second harmonic $H2$ is seen to vary by 40 dB. Very good model to hardware correlation is achieved for this sample at 900 MHz and above, and the trend at low frequency is also in agreement with the data, even if a 10 dB difference is observed below a few hundred MHz.

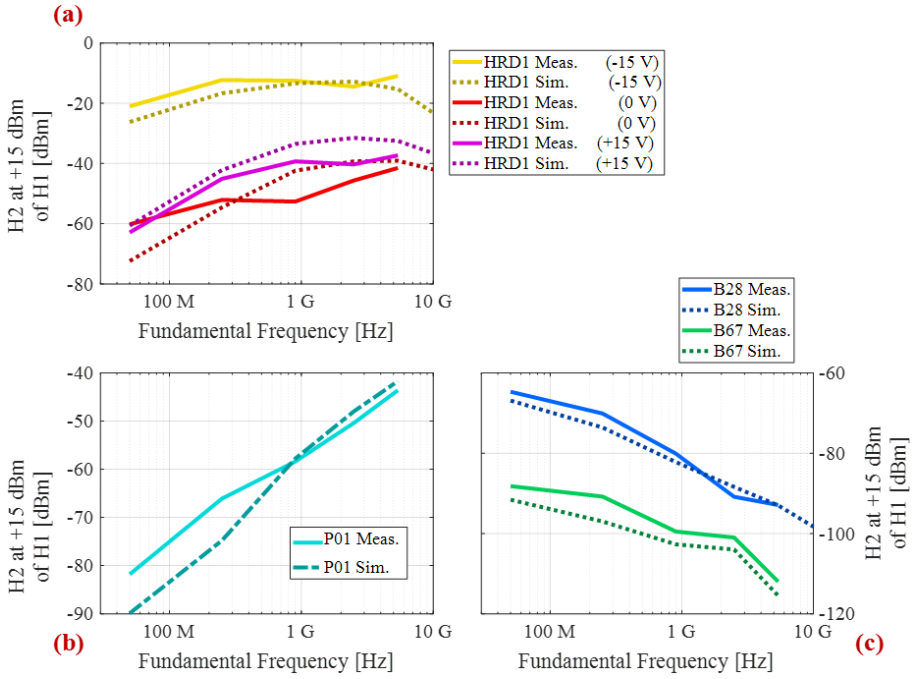


Figure 5.21: CPW line harmonic distortion as a function of fundamental frequency. The second harmonic power level is extracted at +15 dBm of fundamental output power $H1$, measured and simulated on various substrates. **(a)** For sample **HRD1** at three DC bias points. **(b)** For sample **P01** at 0 V DC bias. **(c)** For samples **B28** and **B67** at 0 V DC bias.

Figure 5.21 (c) plots the data pertaining to the samples **B28** and **B67**. In these RFeSI^{TM} substrates f_{SW} is in the range of a few MHz, and therefore the harmonic levels monotonically decrease for increasing f_0 over the measured frequency range because of an increasingly small response in the carrier distributions in the semiconductor volume due to finite carrier response times.

Overall, the four RF substrates are well represented by the large-signal model, and provide high confidence in terms of the physical understanding of the carrier behavior as well as in terms of the relative impact and interplay of the dielectric and substrate impedances on the substrate-induced harmonic distortion.

5.9 Other

5.9.1 Ultra-High Linearity at -100 dBm (RFeSI100^{TM})

Though sample **B67** has already been presented multiple times throughout this chapter, we discuss here in a little more detail how to obtain such high eSI100^{TM} performance by comparing it to the reference **B28** (eSI180^{TM}) substrate which has a similar polysilicon trap-rich fabrication process.

The main difference between these two samples if that **B28** has a nominal resistivity of $\rho_{Si} = 5$ kΩcm and a contamination level of $N_{A,poly} \approx 1.4 \cdot 10^{14}$ cm^{-3}, while **B67** has $\rho_{Si} = 40$ kΩcm and $N_{A,poly} \approx 5.0 \cdot 10^{13}$ cm^{-3}. This is highlighted by the SRP data from **Figure 5.22 (a)**.

Thanks to these two low impurity levels, very few free carriers are present in the **B67** substrate. As we have seen in **Section 3** the magnitude of the substrate-induced harmonic distortion at RF frequencies is dependent on the number of *available* free carriers present in the substrate capable of being modulated by the large-amplitude signal. **Figure 5.22** shows that **B67** then boasts more than 4 times higher ρ_{eff} and approximately 20 dB lower $H2$ distortion level as compared to the eSI80^{TM} substrate **B28**.

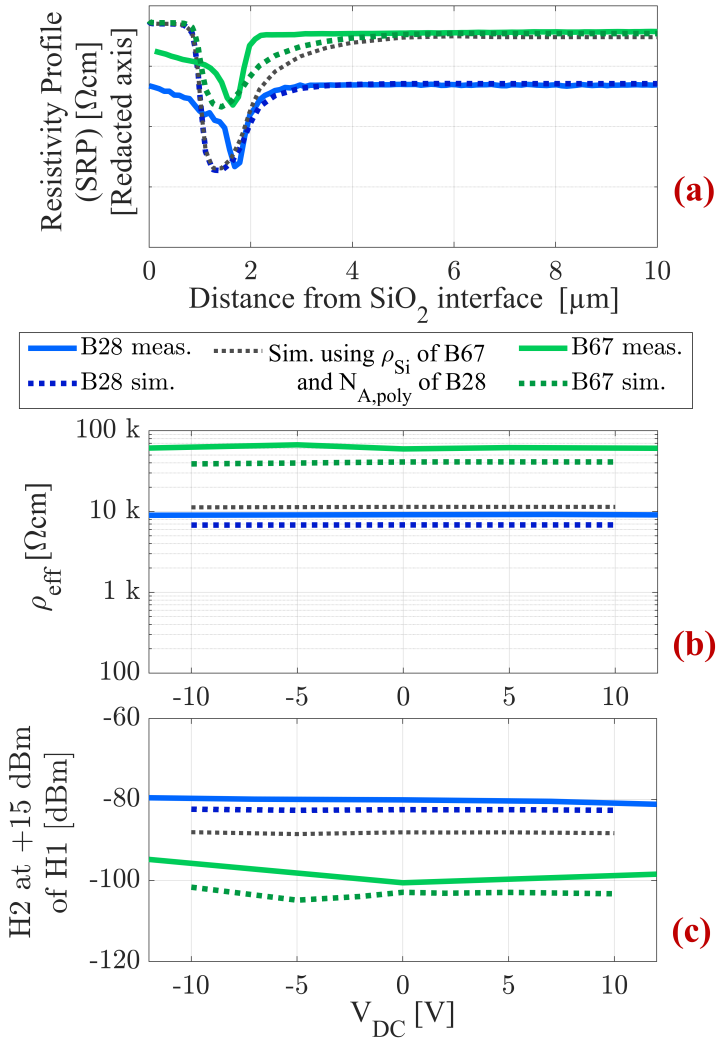


Figure 5.22: Measured and simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC}, for eSI80^{TM} and eSI100^{TM} samples. **(a)** Vertical resistivity profile from BOX interface: measured and simulated SRP (see **Appendix A**). SRP measurements courtesy of Soitec. **(b)** Effective resistivity, extracted above slow-wave mode. **(c)** Second harmonic level for +15 dBm of output fundamental.

5.9.2 Au Compensated Silicon

To provide bulk substrate passivation, doping silicon with gold (Au) atoms has been considered in [134–142] in order to implement high-resistivity substrates, notably for RF applications. It is commonly accepted that gold atoms in substitutional sites in crystalline silicon introduce two main deep-level trap states: a donor level at approximately $E_V + 0.34$ eV and an acceptor level at approximately $E_C - 0.54$ eV [136, 141, 143–146].

UCLouvain, in collaboration with the University of Southampton, has worked to characterize and model Au-compensated substrate samples [147, 148], and the main results are reviewed in this section.

Fabricated Au-Si Samples

Au-compensated silicon samples were fabricated at the University of Southampton, and metal deposition and patterning of the RF structures was performed in UCLouvain's cleanroom facilities.

The process starts from a standard N-type (phosphorous-doped) silicon wafer with a nominal resistivity of 56 Ωcm, which corresponds to a phosphorous donor density of $N_{Ph-D} = 9 \cdot 10^{13}$ cm^{-3}.

Gold atoms were then implanted at the backside of the wafer with a dose of $4 \cdot 10^{13}$ cm^{-2} at an energy of 100 keV.

The sample is subsequently annealed at 950°C in order to diffuse the Au atoms throughout the substrate in order to passivate the entire bulk volume.

An optimized combination of slow-cooling followed by a quenching step is applied to bring the samples back to room temperature, in order to maintain as many Au atoms in active substitutional sites (which contribute deep-level trap centers) rather than in interstitial sites (which do not) of the crystal lattice.

In depth details of all of these processing steps given in [141].

Then, 200 nm of SiO_2 is deposited atop the samples, followed by 1 µm of aluminum in which the RF devices are patterned.

The substrates used were 625 µm thick, and so if the Au atoms were to distribute evenly over this thickness, the volumetric density would be $N_{Au} = 4 \cdot 10^{13}/0.0625 = 6.4 \cdot 10^{14}$ cm^{-3}. It was shown in [135] from Secondary Ion Mass Spectrometry (SIMS) profiling along with SRP profiling that though more Au atoms end up at the front and back interfaces of the wafer, there remains more than $N_{Ph-D} = 9 \cdot 10^{13}$ cm^{-3} gold atoms deep within all parts of the bulk material, enabling sufficient doping compensation and conferring local resistivities higher than 5 kΩcm in every region of the sample.

Working Principle

The working principle can be explained in an analogous manner to that of trap-rich substrates, that was detailed in **Chapter 3 Section 3.3 pg. 87** based on a charge compensation analysis. To avoid low-resistivity, charge-balance must avoid including large free carrier terms n and p, whose presence degrade RF FoMs. In the silicon bulk, any ionized thermal dopants (Phosphorous, Boron, etc.) should then be compensated for by ionized trap states such that the Fermi level E_F is deep in the band gap.

Figure 8.14 illustrates the charge balance at an arbitrary point in the Au-compensated and phosphorous-doped silicon material. Donor states are depicted in purple, while acceptors are shown in blue. A phosphorous level is plotted at energy $E_{Ph-D} = E_C - 0.045$ eV, and gold donor and acceptor levels are plotted at energies $E_{Au-D} = E_V + 0.34$ eV and $E_{Au-A} = E_C - 0.54$ eV, respectively.

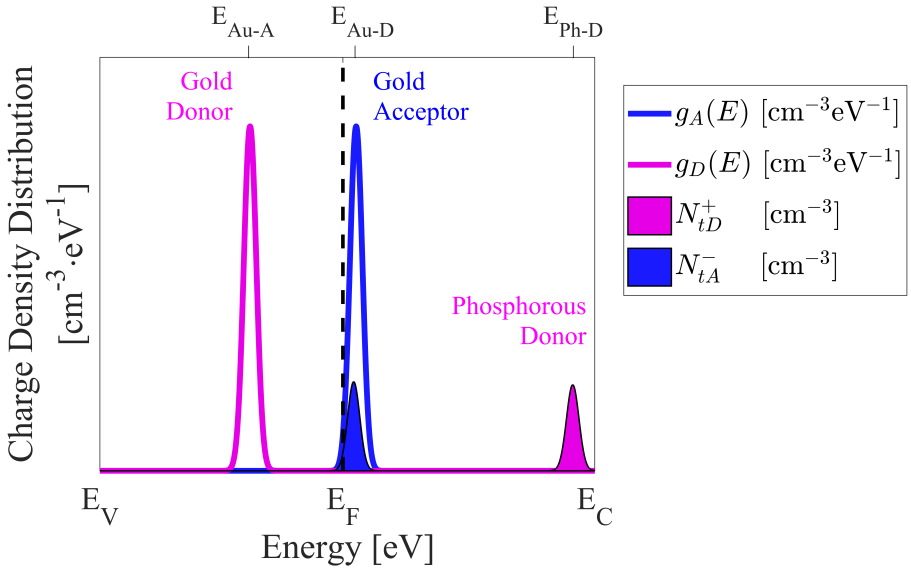


Figure 5.23: Representation of the Fermi level location and trap occupancy in Au-compensated silicon with background N-type phosphorous doping.

These states are depicted as thin distributions labelled as $g_A(E)$ and $g_D(E)$[26], and the integral of the product of each trap distribution by the occupation function over energy yields the total density of ionized gold/phosphorous atoms in the material, expressed in cm^{-3}, according to:

$$N_{tA}^{-} = \int_{E_V}^{E_C} g_A(E) \cdot F(E - E_F)\, dE \qquad [\mathrm{cm}^{-3}] \qquad (5.1)$$

$$N_{tD}^{+} = \int_{E_V}^{E_C} g_D(E) \cdot \big(1 - F(E - E_F)\big)\, dE \qquad [\mathrm{cm}^{-3}] \qquad (5.2)$$

$$g_A(E) = N_{Au} \cdot \delta(E - E_{Au-A}) \qquad [\mathrm{cm}^{-3}\mathrm{eV}^{-1}] \qquad (5.3)$$

$$g_D(E) = N_{Au} \cdot \delta(E - E_{Au-D}) \qquad [\mathrm{cm}^{-3}\mathrm{eV}^{-1}] \qquad (5.4)$$

$$F(\Delta E) = \big(1 + \exp\{\Delta E / kT\}\big)^{-1} \qquad [\,/\,] \qquad (5.5)$$

Where $\delta(x)$ is the Dirac delta distribution function.

In the example curves of **Figure 8.14** the gold states are in a density 5 times higher than the phosphorous state, which is a similar ratio to that in the fabricated samples, as described above with $N_{Au} = 6.4 \cdot 10^{14}$ cm^{-3} and $N_{Ph} = 9 \cdot 10^{13}$ cm^{-3}.

Assuming that free carriers contribute in negligible quantity to the charge balance (true if E_F is deep in the band gap), E_F can be solved for graphically from **Figure 8.14** as the position which yields the same total purple area N_{tD}^{+} and total blue area N_{tA}^{-} [27]. The first term corresponds solely to the ionized thermal phosphorous donors, as the gold donor levels are not ionized. The second term corresponds to the proportion of ionized acceptor gold states for the given E_F value. This Fermi level is very deep, close to mid gap in fact, conferring to the material very low free carrier densities and hence very high resistivity.

In general, when N-type compensation is required (i.e. when considering a sample with thermal donors close to E_C), the Fermi level in Au-Si samples will lodge close to $E_{Au-A} = E_C - 0.54$ eV. If $E_F = E_C - 0.54$ eV, the bulk resistivity will be of 45 kΩcm (slightly N-type).

[26] The representations of $g_A(E)$ and $g_D(E)$ with finite widths in **Figure 8.14** serve to facilitate the reader's understanding. In the TCAD simulator, these distributions are considered as Dirac delta functions, as described by **Equations D.3 and D.4**. In that case, **Equations D.1 and D.2** reduce to $N_{tD}^{+} = N_{Au} \cdot F(E_{Au-A} - E_F)$ and $N_{tD}^{+} = N_{Au} \cdot (1 - F(E_{Au-D} - E_F)$.

[27] Put into mathematical form, if the bulk is N-type with a thermal donor density of N_{D-th}, then the Fermi level will be at a position such that the following relationship is satisfied: $N_{Au-A} \cdot F(E_{Au-A} - E_F) = N_{D-th} \cdot \big(1 - F(E_{D-th} - E_F)\big) \approx N_{D-th}$.

And when P-type compensation is required (i.e. when considering a sample with thermal acceptors close to E_V), the inclusion of Au impurities will see the Femi-level lodge close to $E_V + 0.34$ eV. If $E_{Au-D} = E_F = E_V + 0.34$ eV, the bulk resistivity is around 700 Ωcm (P-type).

From this, we easily understand that the highest performance Au-compensated substrates should start life out as N-type.

The net ionized trap density depends on the Fermi level and hence on the applied E-field, which will contribute to the total charge to be compensated in the substrate, by either free carriers or trapped charge. The total ionized trap density is limited to a finite value due to a finite density of introduced Au. For the samples under consideration, this maximum charge compensation through ionized Au centers is limited to $N_{Au} = 6.4 \cdot 10^{14}$ cm^{-3} (assuming a uniform distribution of the implanted Au and that all Au atoms are in an active substitutional site). Though this value is sufficient to balance the background doping level while ensuring a highly resistive state, it is not high enough to pin the Fermi level close to E_{Au-A} (for an N-type compensated sample) for applied voltages of a few volts over an SiO_2 thickness of 200 nm[28]. Before looking at the RF results, we can then already state that we expect some substrate impedance modulation by the applied electrical signals (DC and RF).

[28] While this is the case in usual trap-rich substrates employing polysilicon, in which the total trap density is orders of magnitudes higher than the $6.4 \cdot 10^{14}$ cm^{-3} considered here for the Au-Si sample. See typical trap distribution parameters used in **Chapters 3 and 5**.

RF Performance Results

Both small- and large-signal measurement and simulation results pertaining to CPW lines fabricated on the Au-Si samples are plotted in **Figure 8.15**, where the interface Fermi level is plotted in **(a)**, and the effective resistivity and $H2$ level are plotted in **(b)** and **(c)**.

The simulated Au-Si substrate includes an interfacial oxide charge density of $N_{ox} = 10^{11}$ cm^{-2}.

The effective resistivity is always above 10 kΩcm for every applied DC bias. This is because the Fermi level is deep in the band gap at all interface regions other than directly beneath the CPW's central signal line. **Figure 8.15 (a)** shows that for zero applied DC field, the interface Fermi level is at $E_{F0_{AuSi}}$, which corresponds to a point close to $E_{Au-A} = E_C - 0.54$ eV, as expected. Hence, there is no PSC, as the gold density is sufficient to provide the surface passivation for the considered N_{ox} of 10^{11} cm^{-2} (while there is a PSC in the non-Au-compensated silicon sample, as it is shown that $E_{F0_{Si}}$ is close to E_C). At 0 Volts of DC bias, the entire interface, including directly below the CPW's central line, is in a state close to mid gap, i.e. highly resistive. The simulated ρ_{eff} at 0 V is then around 100 kΩcm, which is close to the maximum achievable value at 25°C of around 400 kΩcm[29]. The measurement point at 0 V is in the noise detection floor, because the extracted substrate G parameter is extremely low and close to zero. In practice, it is a challenge to extract ρ_{eff} values larger than 20 kΩcm, and is practically impossible to extract a ρ_{eff} above 100 kΩcm[30]. That data point is then set to 100 kΩcm as a default in this plot, and serves as a fairly rough indicator of the true $\rho_{eff}(V = 0)$ of the sample.

At other DC bias points, ρ_{eff} lowers appreciably due to the presence of inversion or accumulation regions below the signal electrode (see $E_F(V)$ curves in **Figure 8.15 (a)**), though remains high, above 10 kΩcm, (these values are in the measurement detection range) as these regions come in series with the near-intrinsic resistivity regions between the CPW's signal and ground lines. This measured $\rho_{eff}(V)$ behavior is in agreement with the simulated data.

[29] The maximization of $\rho_{Si} = (q\mu_n n + q\mu_p p)^{-1}$ at 25°C for optimal Fermi-level position yields $\rho_{Si-MAX}(T = 25) \approx 250$ kΩcm, considering usual carrier mobilities of silicon, i.e. not considering any additional scattering due to the Au implants (additional scattering due to Au centers is not included in the considered TCAD simulations either). Due to the 200 nm layer of SiO_2 (infinite resistivity), the maximum ρ_{eff} of the considered CPW line is then slightly increased, to $\rho_{eff-MAX}(T = 25) \approx 400$ kΩcm for such a MOS stack of material.

[30] At least using the CPW dimensions and measurement equipment considered in this work.

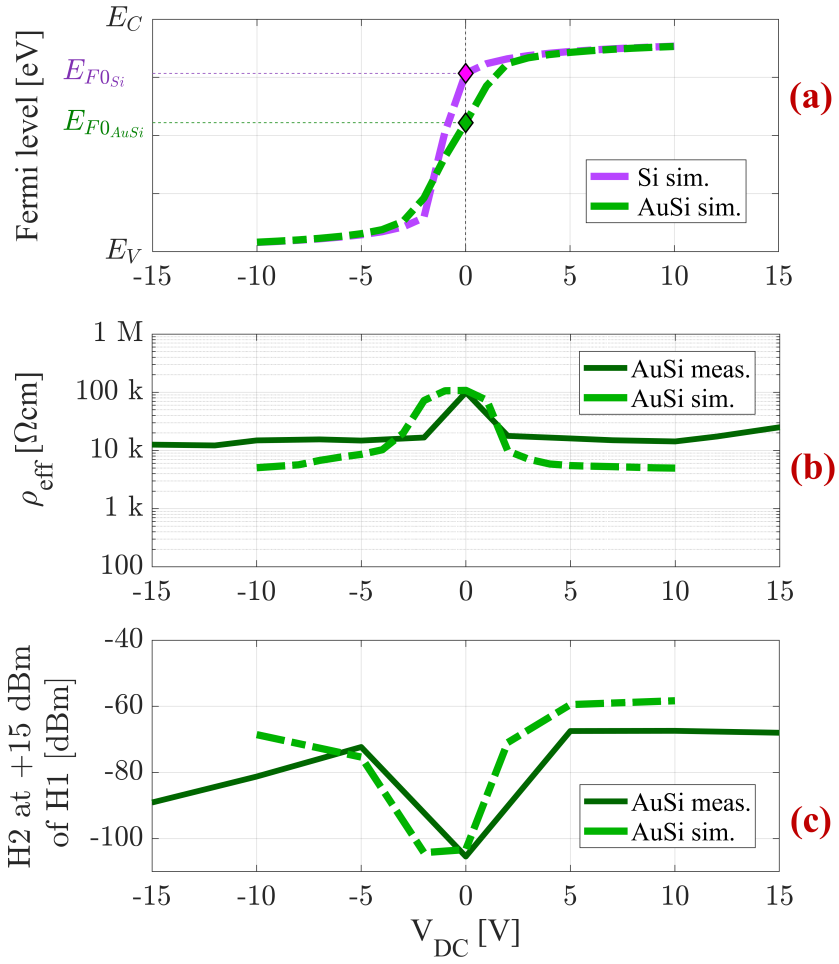


Figure 5.24: Simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC} implemented on an Au-compensated silicon substrate. **(a)** Position of the equilibrium Fermi level at 100 nm below the oxide layer. **(b)** Effective resistivity, extracted above slow-wave mode. **(c)** Second harmonic level for +15 dBm of output fundamental.

In terms of harmonic distortion levels, the large-signal model also correlates well to the hardware data. As extensively discussed in **Chapters 3 and 5**, the $H2$ level is strongly dependent on the number of *available free carriers* in the substrate that the RF signal can modulate. At a bias of 0 Volts extremely few

carriers are present in the semiconductor due to deep Fermi level positions at every location. The substrate is then very linear, with a $H2$ level below -100 dBm, which is of similar quality to the best in-class RFeSI^{TM} trap-rich substrate from Soitec, see **Section 5.9.1 pg. 206**.

However, when the DC bias induces inversion or accumulation layers below the central CPW electrode, the large-amplitude RF signal can then more strongly modulate the overall substrate impedance, as these *available free carriers* are alternately pushed away from and then pulled towards the silicon region below the signal line. The $H2$ remains quite low in absolute value, with the measured data remaining below -65 dBm over the considered bias range. This physical interpretation was verified by analyzing the free carrier distributions in the transient simulation results. The linearity variations of more than 30 dB in the $H2(V)$ curve are well captured by the large-signal simulations, further validating the robustness of the modelling approach.

From a theoretical standpoint, we note that by substantially increasing the Au impurity concentration, Fermi level pinning over several Volts of DC bias should be achievable. Then, though the bulk resistivity may slightly decrease as the Fermi level could move further away from mid gap **[135]**, the $\rho_{eff}(V)$ and $H2(V)$ should improve[31] and become flat over an extended bias range.

5.9.3 PN-Doped High-Resistivity Substrate

Silicon-based RF substrate solutions that implement alternations of shallow P and N type implants at the Si/SiO_2 interface of a high-resistivity bulk are also considered in this work, and will be discussed in detail in **Chapter 8 Section 8.2** (**pg. 265**). These implants serve to passivate the interface and significantly increase its impedance by interrupting the PSC layer with highly-resistive depletion PN junctions.

The large-signal approach was employed to simulate such substrates and though the results will be presented in **Section 8.2**, we note here that the model to hardware correlation is good, and that these samples also lend validity to the modelling approach.

[31] Improvements should certainly be observed in the $H2$ levels at bias points other than 0 V. Depending on the exact location of $E_F(V=0)$, the $\rho_{eff}(V=0)$ may slightly increase or slightly decrease when increasing the active Au concentration.

5.10 Chapter Summary

In this chapter, large-signal on-wafer RF measurements of CPW lines were performed on 20 different wafers under various conditions in order to validate the large-signal model developed in this thesis.

The model was shown to correlate well to the CPW measurements of these samples over the following parameters:

- **Material parameters**:
  - ***Interfacial fixed charge densities*** (positive and negative) up to $2.1 \cdot 10^{12}$ cm^{-2},
  - Presence or not of a ***polysilicon passivation layer***, with various ***trap densities*** considered,
  - Bulk silicon ***nominal resistivity***, from 20 Ωcm to 10 kΩcm,
  - ***Impurity contamination in the polysilicon*** layer, from very low up to $7 \cdot 10^{14}$ cm^{-3}.
- **CPW parameters**:
  - CPW line ***width/spacing***, from 11/8 µm/µm to 95/50 µm/µm,
  - CPW line ***length***, from 1.2 mm to 8.0 mm.
- **Measurement conditions**:
  - ***Temperature***, from 25°C to 190°C,
  - ***Fundamental frequency***, from 50 MHz to 5.4 GHz.

In general, over all of these parameters, the model captures well the substrate-induced signal distortion, and is a rigorous modelling approach along a CPW transmission line including physical non-equilibrium phenomena such as carrier dynamics and carrier spatial redistribution, that can be captured as a response to any time varying voltage signal on the line using the developed methodology.

Though HD discrepancies between the model and the measurements can be as high as 10 dB, they are usually below 5 dB, and overall, the results from this chapter lend high confidence to the physical modelling approach, as all trends are well evaluated.

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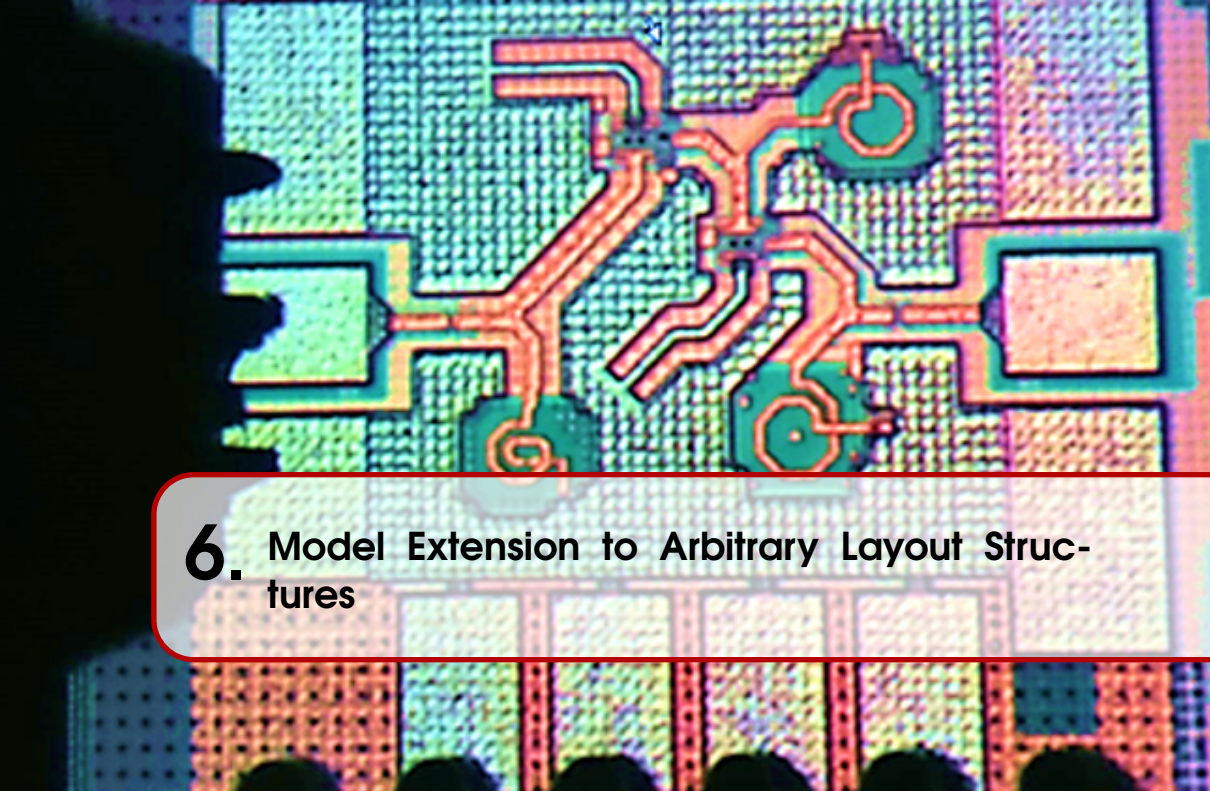
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Overview of Part IV

Chapter 6 offers a perspective methodology to extend the non-linear substrate modelling to any arbitrary layouts, beyond uniform CPW lines, by coupling TCAD responses with full-wave EM simulation results.

With this methodology, an integration path for the large-signal substrate model into a flow of IC design tools becomes foreseeable. The proof-of-concept of the proposed approach is demonstrated by comparing its results to on-wafer HD measurements of passive two port devices that are significantly different from CPWs: a two-port crosstalk device and an inductive meander line.

Finally, **Chapter 7** is dedicated to reviewing the global conclusions of this thesis, and to offer perspective future endeavors in line with the presented work.



6. Model Extension to Arbitrary Layout Structures

In **Chapter 4** a large-signal modelling approach was described for CPW lines that combined closed-form analytical expressions of the series R and L terms with the shunt non-linear substrate terms $G(V)$ and $C(V)$ obtained from TCAD-based simulations. This approach was based on the telegraph equations for transmission-lines and allows for the use of TCAD computations in 2D, as CPW lines are uniform in the direction of propagation.

In order to extend the non-linear modelling to arbitrary layouts, a combination with an EM tool is proposed.

In this chapter, non-linear *surface impedance* elements are obtained from TCAD simulations and combined with EM simulation tools that will take into account all *linear* substrate and BEOL interactions in the physical layout.

The methodology is first applied to CPW lines to verify the validity of the approach, and is then used to simulate more complex passive RF layouts, such as two-port crosstalk structures and meander inductors.

Finally, model to hardware correlation is discussed for several HR and TR samples.

6.1 Methodology

6.1.1 EM Simulation Partitioning

To simulate arbitrary layouts, we propose combining two EM simulations with non-linear admittances $Y_{surf}(V)$ that serve to model the dielectric/silicon interface. This methodology is depicted in **Figure 6.1**, where an S-parameter matrix S_{BEOL} with $2N$ ports is combined with N surface non-linear admittances and with an N-port S-parameter matrix S_{Sub}.

S_{BEOL} and S_{SUB} are obtained from two distinct EM simulations, each using a different material stack.

S_{BEOL} accounts for all coupling interactions in the BEOL layers, as well as the coupling to the dielectric/silicon interface. Coupling through materials below the dielectric/silicon interface are not accounted for in S_{BEOL}.

S_{SUB} contains information about the coupling between each part of dielectric/silicon interface with all other parts of the dielectric/silicon interface through the silicon bulk material. Coupling through materials above the dielectric/silicon interface are not accounted for in S_{SUB}.

Figure 6.2 depicts the $2N$ port definitions and the **material stack A** implemented for the calculation of S_{BEOL}. The case of a CPW line is depicted, though the methodology remains generally applicable to any layout. Ports 1 to N are defined in the metallic layer named "BEOL-layer", while ports $N+1$ to $2N$ are defined below the dielectric stack using layer "SUB-layer". Silicon is not defined beneath these dielectrics, but is replaced by the material "VOID". This material has low permittivity (and zero conductivity) so as to limit any port interactions through this material[1].

Figure 6.3 depicts the N port definitions and the **material stack B** implemented for the calculation of S_{SUB}. All N ports are defined at the silicon interface, and aim to capture the (linear) coupling between all ports through the silicon region.

Then, S_{BEOL} and S_{SUB} are connected up together through non-linear surface admittances $Y_{surf}(V)$, as depicted in **Figure 6.1**, where it is also shown that two global GSG ports are defined to excite the passive (CPW) structure.

[1] In the EM simulator used in this work, ADS Momentum from Keysight, the minimum allowed relative permittivity is 1, and this is what was used for material "VOID" in this work ($\varepsilon_{r,VOID} = 1$). There will then be some capacitive coupling proportional to this permittivity through this material. This coupling will be compensated for later on, when combining with EM simulation of the silicon substrate (to produce S_{SUB}), where we shall not use silicon's permittivity $\varepsilon_{r,Si} = 11.7$ but shall instead use a reduced value.

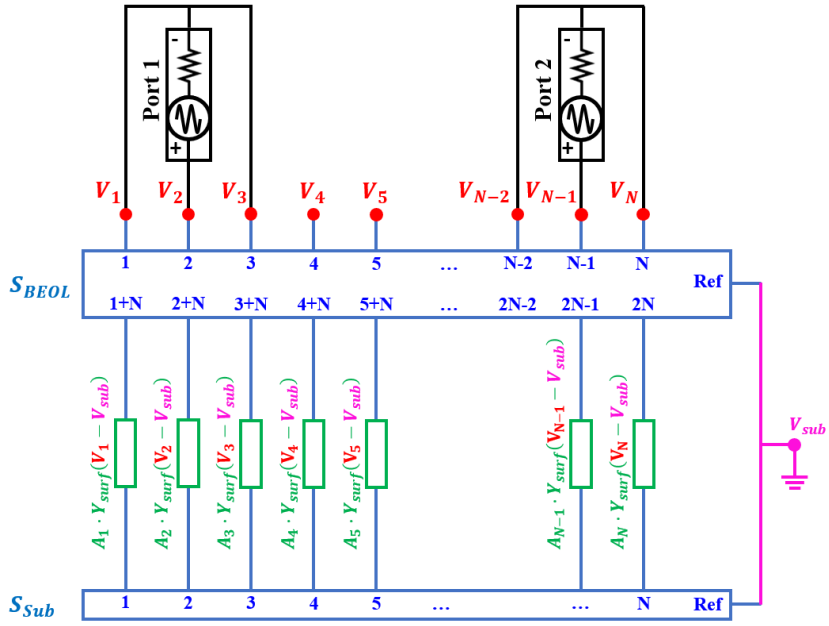


Figure 6.1: Large-signal simulation methodology combining a $2N$-port EM simulation file S_{BEOL} with an N-port EM simulation file S_{SUB} and N non-linear dipole admittances $Y_{surf}(V)$.

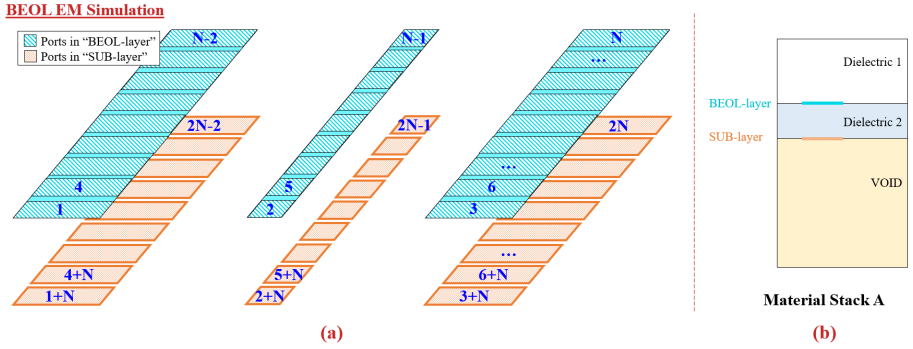


Figure 6.2: *BEOL EM Simulation.* **(a)** Layout representation and $2N$ port definitions. **(b)** Material stack used for the BEOL EM layout simulation.

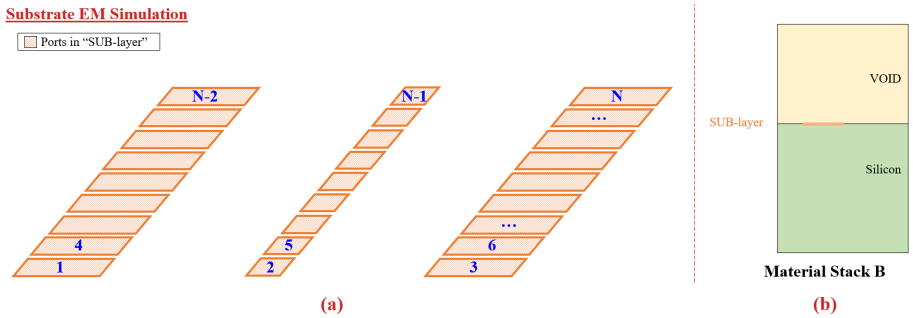


Figure 6.3: *Substrate EM Simulation.* **(a)** Layout representation and N port definitions. **(a)** Material stack used for the Substrate EM layout simulation.

The ports are sized smaller than $\lambda/40$ for accurate spatial resolution, where λ is the shortest electrical wavelength of the considered signals propagating in the passive device. Considering a harmonic simulation at a fundamental frequency of $f_0 = 900$ MHz, and considering simulating up to the third harmonic component we calculate the maximal port size as 1.1 mm (using an effective relative permittivity of 6.5). In the cases presented in this chapter, the largest dimension of the considered ports will be 100 µm, satisfying the above criteria.

Figure 6.4 depicts the port definitions in the layout of the 2.1 mm-long reference CPW line[2]. A total of $2N = 168$ ports are used in the *EM BEOL Simulation* and a total of $N = 84$ ports are used in the *EM Substrate Simulation*. This type of top-view representation will be used from here on to illustrate the port partitioning and sizing used for the two EM simulations of each considered passive device of this chapter.

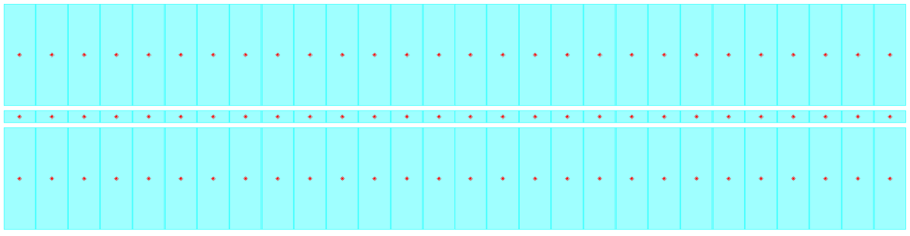


Figure 6.4: Two-port CPW line layout and representation of the EM ports ($N = 84$).

[2]Signal conductor width W_C of 26 µm and gap spacing to ground lines of S of 12 µm.

6.1.2 Partitioning Verification in Small-Signal

Before considering including any non-linear elements, let us first verify that the partitioning approach is valid under small-signal (linear) simulation analysis.

To do so, the 2-port passive layout of **Figure 6.5** is considered. This crosstalk structure is identical to that presented in **Chapter 2** in **Section 2.3** **Figure 2.10** (see **pg. 49**).

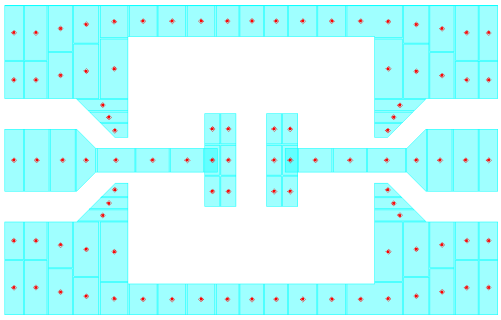


Figure 6.5: Two-port crosstalk layout and representation of the EM ports ($N = 96$).

This structure's S-parameters are simulated using two approaches. The passive device is implemented using 1 µm thick aluminum atop 400 nm of SiO_2 with a uniform silicon bulk beneath it with $\rho_{Si} = 5.5$ kΩcm and $\varepsilon_{r,Si} = 11.7$.

The reference simulation approach using the EM tool ADS Momentum is identical to that used throughout **Chapter 2**, where six pins are defined to implement two coplanar GSG port inputs to the passive device defined atop the aforementioned material stack. The S_{21} parameter of this reference simulation is plotted over frequency as the blue curve in **Figure 6.6**.

The second simulation approach is based on two EM simulations. The first *BEOL EM simulation* implements $2N$ ports ($N = 96$) and serves to include all BEOL interactions and coupling to the plane beneath the dielectric layer, as discussed above and based on **Figure 6.2**. The second *substrate EM simulation* implements N ports and serves to include all substrate interactions, as discussed above and based on **Figure 6.3**. The two S-parameter files are then connected without the inclusion of any non-linear surface impedance elements, and two GSG global ports are defined as depicted in **Figure 6.1**. The simulated S_{21} parameter is then plotted in red in **Figure 6.6**, and fits well to the reference simulation over the wideband simulated frequency range.

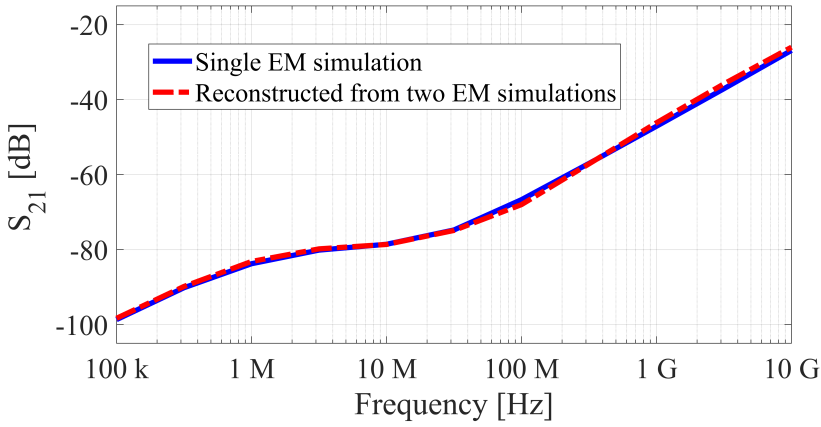


Figure 6.6: Simulated S_{21} of the two-port crosstalk structure of **Figure 6.5** using two approaches. The first approach is classical and implements a single EM simulation and six pins to excite the two GSG ports of the structure. The second approach combines two separate EM simulations employing respectively N ports and $2N$ ports, that are then reconnected together to model the entire layout and materials.

In the *substrate EM simulation*, the silicon material must have its relative permittivity reduced such that the overall coupling including the various "VOID" material (with non-zero permittivity) layers remains accurate. In the *BEOL EM simulation*, some "substrate" (bottom material "VOID") coupling is included due to the relative permittivity of the "VOID" material $\varepsilon_{r,VOID}$. This coupling should not be accounted for twice, and justifies a first reduction of $\varepsilon_{r,Si}$ in the *substrate EM simulation*. Furthermore, coupling proportional to $\varepsilon_{r,VOID}$ also occurs in the "VOID" material of the *substrate EM simulation*, and this justifies a second reduction in $\varepsilon_{r,Si}$. Overall, $\varepsilon_{r,Si}$ is replaced by $\varepsilon_{r,Si} - 2 \cdot \varepsilon_{r,VOID}$ in this simulation approach (to compensate for the inevitable coupling through the "VOID" material present in the two considered material stacks). Whereas in the reference simulation involving a single EM result, $\varepsilon_{r,Si}$ was used (in the single material stack). Overall, identical capacitive coupling is achieved using this method, as can be seen from the good agreement between the two methods at high frequency in **Figure 6.6**. In the results presented here, in practice $\varepsilon_{r,VOID}$ was set to 1, and so $\varepsilon_{r,Si}$ was set to 9.7 in the second simulation approach (and to 11.7 in the reference EM simulation).

This verifies the partitioning approach under small-signal excitation, and is valid for any arbitrary layout. Small-signal CPW line simulations were also run and the results (not shown[3]) also validate that this partitioning approach is accurate for such passive devices.

We note that this partitioning cannot account for mutual inductive coupling between the BEOL structures and the substrate. Eddy currents are then neglected through this approach, which is a reasonable assumption for modelling substrates with effective resistivities above 1 Ωcm[4].

[3]Because the frequency dependency of the S-parameters of low-loss matched lines is not as interesting as the presented wideband S-parameters of the 2-port crosstalk structure, that illustrate nicely the accurate modelling of the dielectric capacitance as well as the semiconductor bulk's resistive and capacitive nature over a wide band.

[4]Compact models of RF passives on silicon substrates found in the literature only include a mutual inductance element with the substrate on high conductivity silicon, such as on epitaxial silicon substrates (in the 10 mΩcm range), and are neglected in the passive models on higher resistivity materials **[73–79]**.

6.1.3 Obtaining the Non-Linear Surface Admittance

In this section, the non-linear surface elements $Y_{surf}(V)$ are discussed.

They are obtained from the TCAD simulated $G_{neq}(V)$ and $C_{neq}(V)$ responses discussed in **Chapter 4**.

Specifically, the surface non-linear element is obtained from an analogy of the overall TCAD simulated $G_{neq}(V)$ and $C_{neq}(V)$ with the equivalent circuit model of **Figure 6.7**. Then, Z_{surf} is calculated as follows[5]:

$$Z_{surf} = Z_{sub} - Z_{Si-Hein} \quad [\Omega m] \quad (6.1)$$

$$Y_{Si-Hein} = G_{Si-Hein} + j\omega C_{Si-Hein} = \left(1/\rho_{Si} + j\omega\varepsilon_{Air}\right)F_{bot} \quad [S/m] \quad (6.2)$$

$$Z_{sub} = Z_{bot} - Z_{ox} \quad [\Omega m] \quad (6.3)$$

$$Z_{ox} = 1/(j\omega C_{ox_C}) + 1/(2 \cdot j\omega C_{ox_G}) \quad [\Omega m] \quad (6.4)$$

$$C_{ox_c} = \varepsilon_{ox} W_C / t_{ox} \quad [F/m] \quad (6.5)$$

$$C_{ox_g} = \varepsilon_{ox} 2(W_C + S)/t_{ox} \quad [F/m] \quad (6.6)$$

$$Y_{bot} = Y_{neq} - Y_{Air-Hein} \quad [S/m] \quad (6.7)$$

$$Y_{Air-Hein} = j\omega C_{Air-Hein} = j\omega\varepsilon_{Air} F_{top} \quad [S/m] \quad (6.8)$$

$$Y_{neq} = G_{neq} + j\omega C_{neq} \quad [S/m] \quad (6.9)$$

where Heinrich's closed-form expressions **[65]** of CPW *RLGC* parameters are used to calculate $Y_{Si-Hein}$ and $Y_{Air-Hein}$ from the geometrical factors F_{top} and F_{bot} that are determined analytically from the CPW dimensions (as previously discussed in **Section 2.1.2 pg. 32**).

Then, non-linear conductance and capacitance terms are determined at the surface as:

$$G_{surf}(V) = \Re\{Y_{surf}\} \quad [S/m] \quad (6.10)$$

$$C_{surf}(V) = \Im\{Y_{surf}\}/\omega \quad [F/m] \quad (6.11)$$

It is important to note that because $G_{neq}(V_{BEOL} - V_{Sub})$ and $C_{neq}(V_{BEOL} - V_{Sub})$ depend on the large-signal defined as the difference between the BEOL voltage V_{BEOL} and the substrate voltage V_{Sub}, so too do $G_{surf}(V)$ and $C_{surf}(V)$. It is to be understood that the current flowing through the surface admittance is:

$$\begin{aligned} I_{surf}(t) = \quad & G_{surf}\left(V_{BEOL}(t) - V_{Sub}(t)\right) \cdot V_{surf}(t) \\ & + C_{surf}\left(V_{BEOL}(t) - V_{Sub}(t)\right) \cdot \frac{\partial V_{surf}(t)}{\partial t} \end{aligned} \quad (6.12)$$

[5] The equation for C_{ox_g} is an approximation.

where V_{surf} is the voltage drop across the surface admittance Y_{surf}, and the overall large signal $V_{BEOL} - V_{Sub}$ controls the values of the surface elements (as depicted in **Figure 6.1**). Zero voltage difference is defined between the substrate and the CPW ground lines, so that all impedance variations are associated to the region beneath the central electrode.

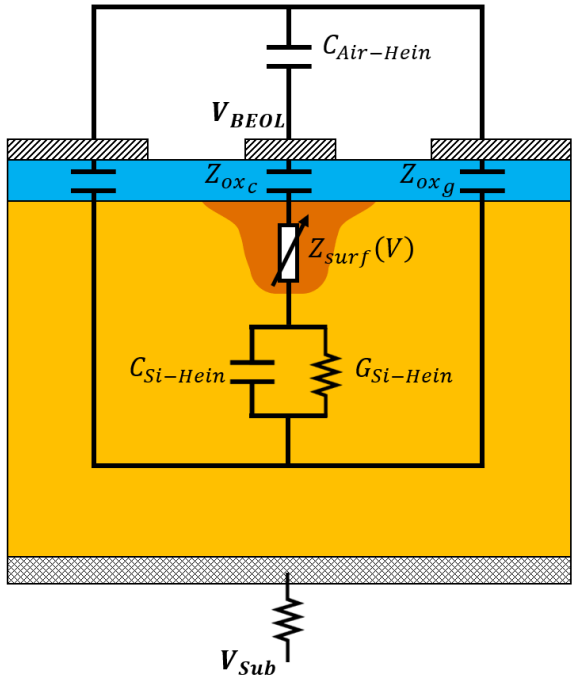


Figure 6.7: Cross-section of the simulated MOS CPW structure used to obtain the G_{neq} and C_{neq} elements between the central line and the two outer lines. The two outer lines are set to the same DC potential as the back-side of the substrate (the back-side is RF floating). An equivalent circuit model is overlayed on the structure to highlight the extraction of the Z_{surf} element.

Terms G_{surf} and C_{surf} are given per unit length, and their voltage-dependencies are associated with free carrier variations beneath the signal electrode of width W_C. We can then calculate normalized surface admittance elements per unit area as:

$$G_{surf\text{-}norm}(V) = G_{surf\text{-}norm}(V)/W_C \quad [\mathrm{S/m^2}] \quad \textbf{(6.13)}$$

$$C_{surf\text{-}norm}(V) = C_{surf\text{-}norm}(V)/W_C \quad [\mathrm{F/m^2}] \quad \textbf{(6.14)}$$

The following basis functions are used towards analytical fitting of the non-linear responses of these surface elements:

$$\widetilde{G}_{surf\text{-}norm}(V) = G_0 + G_1 \cdot V + G_2 \cdot V^2 + G_3 \cdot V^3 + G_4 \cdot V^4 + G_d \cdot \frac{\partial V}{\partial t} \quad \textbf{(6.15)}$$

$$\widetilde{C}_{surf\text{-}norm}(V) = C_0 + C_1 \cdot V + C_2 \cdot V^2 + C_3 \cdot V^3 + C_4 \cdot V^4 + C_d \cdot \frac{\partial V}{\partial t} \quad \textbf{(6.16)}$$

Such analytical expressions will then be included in a *harmonic-balance* type simulator **[149]** and combined with two EM simulations to model the overall non-linear behavior of a passive layout on different types of silicon-based substrates.

This extraction procedure assumes that all impedance variation occurs directly below the metal BEOL element (as the $Y_{surf\text{-}norm}$ parameters are normalized to the metal BEOL element's area). This hypothesis is of limited validity, notably for HR-type substrates that are affected by PSC effects[6]. For the case of TR type substrates, this assumption is expected to hold better, and motivates the investigation proposed in this chapter.

[6] And especially when they are biased to strong voltages of the opposite sign of the interfacial fixed charge, as in that case highly voltage-sensitive lateral depletion regions exist that are strongly modulated by large-amplitude RF signals.

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6.1.4 Implementation in ADS Harmonic Balance

To reconstruct the overall simulation from S-parameter files and analytical non-linear modelling of surface elements, ADS's schematic environment is used [150], in which the harmonic-balance is implemented as the simulation type [149].

Figure 6.8 depicts a typical non-linear simulation using this approach, combining a $2N$-port BEOL EM-simulated S-parameter file, an N-port substrate EM-simulated S-parameter file, and N non-linear admittance elements $Y_{surf}(V)$.

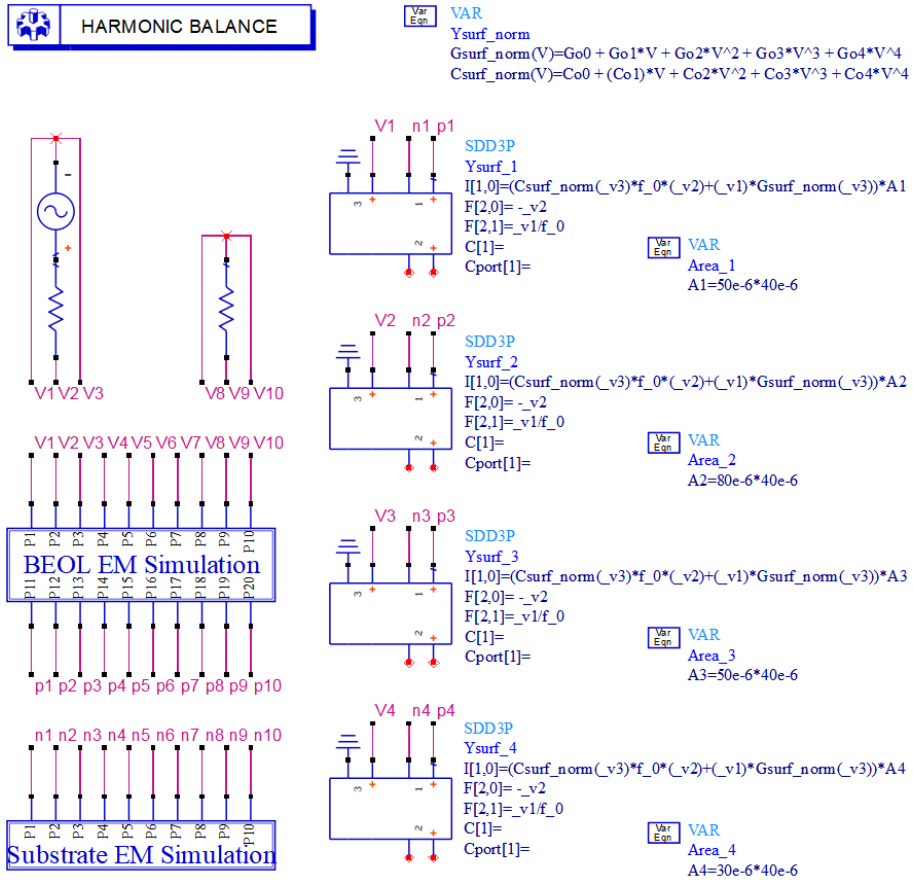


Figure 6.8: Large-signal simulation approach using ADS harmonic balance combining two EM S-parameter files (*BEOL EM Simulation* and *Substrate EM Simulation*) and N non-linear surface admittance elements $Y_{surf}(V)$.

The non-linear surface admittances are defined using *Symbolically Defined Devices* (SDD) from the ADS library which allow the creation of user-defined non-linear components **[151]**.

A three port SDD device (SDD3P) is defined for each non-linear surface element. At each port k the voltage and current are written as v_k and i_k, respectively.

For each SDD3P surface element, with reference to the formulae shown in **Figure 6.8**, inputs $F[2,0]$ and $F[2,0]$ define together an implicit equation at port 2:

$$F[2,0] + \frac{\partial F[2,1]}{\partial t} = 0 \tag{6.17}$$

where we have defined (see **Figure 6.8**):

$$F[2,0] = -v_2 \tag{6.18}$$

$$F[2,1] = v_1 / f_0 \tag{6.19}$$

such that the overall equation defined can be written as:

$$v_2 = \frac{1}{f_0} \cdot \frac{\partial v_1}{\partial t} \tag{6.20}$$

Port 2 of all SDD3P devices is left floating, and v_2 serves only as an intermediate variable in which to calculate and store the derivative of v_1, the voltage drop over the considered surface element[7]. Multiplication by f_0, the main frequency component of v_1 is recommended for increased stability of the numerical computations **[151]**.

Then, an explicit equation serves to compute the current at port 1 of the SDD3P devices, which is the current flowing between the two EM S-parameter-defined devices through the non-linear substrate surface impedances. It writes for each SDD3P element as:

$$I[1,0] = \left(\widetilde{C}_{surf\text{-}norm}(v_3) \cdot f_0 \cdot v_2 + \widetilde{G}_{surf\text{-}norm}(v_3) \cdot v_1\right) \cdot A_N \tag{6.21}$$

where the surface admittance values are controlled by the third port voltage v_3, which samples the large-signal amplitude present between the metal passive device and the substrate $V_{BEOL_N\text{-}Sub} = (V_{BEOL_N} - V_{Sub})$ above the non-linear

[7] Previously referred to as v_{surf} in the above text.

surface element N under consideration. Substituting I_{surf_N} for $I[1,0]$ and $\partial v_1/\partial t$ for $f_0 \cdot v_2$, and $V_{BEOL_N\text{-}Sub}$ for v_3, and v_{surf_N} for v_1, we can rewrite the surface current for each SDD3P device as:

$$I_{surf_N} = \left(\widetilde{C}_{surf\text{-}norm}(V_{BEOL_N\text{-}Sub}) \cdot \frac{\partial v_{surf_N}}{\partial t} + \widetilde{G}_{surf\text{-}norm}(V_{BEOL_N\text{-}Sub}) \cdot v_{surf_N}\right) \cdot A_N \tag{6.22}$$

While $\widetilde{G}_{surf\text{-}norm}$ and $\widetilde{C}_{surf\text{-}norm}$ are expressed in [S/m^2] and [F/m^2] respectively, I_{surf_N} is expressed in Amps [A], as denormalization occurs for each surface admittance SDD3P device through multiplication by area A_N, expressed in [m^2], which is the area of the substrate port of the EM simulations under consideration, connected through the SDD3P element.

Equation 6.22 is analogous to **Equation 6.12**, demonstrating that this implementation produces the desired modelling.

In the simple example presented in **Figure 6.8** N is equal to 10, and surface admittances 1 to 4 are shown (and admittances 5 to 10 are not). Each surface element is scaled by the substrate port area A_N.

Nodes 1 to 3 are used to define the excitation GSG port, where a large-signal fundamental tone will be inputted, and nodes $N-2$ to N are used to define the second GSG port, where the output signal spectrum will be analyzed (see **Figure 6.1** for similar uses of these nodes).

In practice, when simulating passive layouts at RF frequencies, N will be in the range of 100 in the cases presented in the next sections of this chapter, and the reference port impedances will be set to 50 Ω, as is the case during the large-signal on-wafer hardware measurements.

The attentive reader will have realized that the non-linear impedances as described above based on the SDD3P devices do not include dependencies on $\partial V_{BEOL}/\partial t$. In practice, these can be modelled using an SDD4P device by calculating and storing $\partial V_{BEOL}/\partial t$ in the fourth port voltage v_4 by using the following SDD equations:

$$
\begin{aligned}
I[1,0] &= \Big(\big(\widetilde{C}(v_3) + \widetilde{C}_d \cdot f_0 \cdot v_4\big) \cdot f_0 \cdot v_2 + \big(\widetilde{G}(v_3) + \widetilde{G}_d \cdot f_0 \cdot v_4\big) \cdot v_1 \Big) \cdot A_N \\
F[2,0] &= -v_2 \\
F[2,1] &= v_1/f_0 \\
F[4,0] &= -v_4 \\
F[4,1] &= v_3/f_0
\end{aligned}
$$

However, when using such a definition in the harmonic balance simulator convergence problems arise and no solution is obtained. Therefore, for these reasons parameters G_d and C_d will be set to zero throughout the rest of this chapter, and all least-squares fitting on $G_{neq}(V)$ and $C_{neq}(V)$ data to obtain $\widetilde{G}_{neq}(V)$ and $\widetilde{C}_{neq}(V)$ expressions will be performed without including $\partial V/\partial t$ in the list of basis functions.

6.2 Model-Hardware Correlation Results

This section is dedicated to running the $EM + Y_{surf}(V)$ model for different RF passive layouts on several reference RF substrates, and comparing the results to measured data (at 900 MHz and up to +25 dBm).

To that end, we shall first consider the modelling of several 2-port layouts on two eSI wafers (samples **B28** and **B67**), starting with a model calibration of $Y_{surf}(V)$ using CPW lines, and then using the same $Y_{surf}(V)$ function to further model more complex layouts, notably a 2-port crosstalk structure and a meander inductor.

6.2.1 CPW Lines and Model Calibration

900 MHz harmonic distortion simulations and measurements of the reference 2.1 mm-long CPW line on sample **B28** are plotted in **Figure 6.9**. The power of the output spectral components $H1$, $H2$ and $H3$ are plotted against the power of the 900 MHz pure tone input of power P_{in}.

The simulation results of the $RLG_{neq}(V)C_{neq}(V)$ CPW model presented in **Chapter 4** show good agreement to the measured data in terms of $H2$, and this good correlation for sample **B28** was previously presented in **Chapter 5** based on material input parameters and physical modelling. The third harmonic is overestimated however using the TCAD non-linear input data, as $H3$ information was not used during the simulation fitting in **Chapter 5**.

By transforming the lineic $G_{neq}(V)$ and $C_{neq}(V)$ data into $\widetilde{G}_{surf\text{-}norm}(V)$ and $\widetilde{C}_{surf\text{-}norm}(V)$ expressed per unit area (see **Section 6.1.3**), the $EM + Y_{surf}(V)$ simulation is run, based on the EM layout of **Figure 6.4** in which the characteristic port discretization number is $N = 84$.

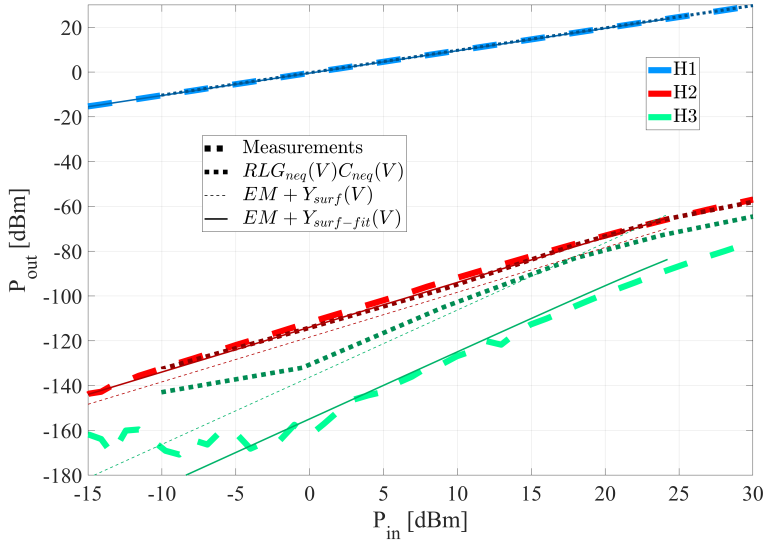


Figure 6.9: Measured and simulated power of the output components of the reference CPW line on sample **B28** for a 900 MHz input signal of power P_{in}. Low noise floor (-170 dBm) measurements courtesy of Incize **[152]**.

Good agreement between this model and the $RLG_{neq}(V)C_{neq}(V)$ model validates the approach for the considered **B28** sample. The agreement between

these two models in terms of output $H1$ is within 0.05 dB difference, while the $H2$ and $H3$ components are within 3 to 4 dB of difference between the two models.

The analytical fitting parameters employed in the expression of $\widetilde{G}_{surf\text{-}norm}(V)$ and $\widetilde{C}_{surf\text{-}norm}(V)$ are given in **Table 6.1**[8]. These were obtained from the 2D-TAD simulation results [9] $G_{neq[4,900\text{M},0]}(V)$ and $C_{neq[4,900\text{M},0]}(V)$ by applying the method described in **Section 6.1.3**.

The material parameters of the 2D TCAD simulations were tuned such that the $RLG_{neq}(V)C_{neq}(V)$ model fed with its results would fit to the measured data (in terms of $H1$ and $H2$). Since there is a non-negligible discrepancy of 3 to 4 dB between the $RLG_{neq}(V)C_{neq}(V)$ model and $EM+Y_{surf}(V)$ model using the same TCAD non-equilibrium admittance data, the $Y_{surf}(V)$ function is slightly tuned and replaced by $Y_{surf\text{-}fit}(V)$ such that the $EM+Y_{surf\text{-}fit}(V)$ model fits to the measured data (including $H3$). The tuned fitting parameters are also given in **Table 6.1** for the analytical modelling of the $Y_{surf\text{-}fit}(V)$ functions.

	G_0 C_0	G_1 C_1	G_2 C_2	G_3 C_3	G_4 C_4	G_d C_d
$\widetilde{G}^{\text{B28}}_{surf}$	-3.4e4	-465	-659	-5.9	0.23	0
$\widetilde{C}^{\text{B28}}_{surf}$	5.0e-5	1.1e-7	-3.1e-8	-6.0e-10	9.7e-12	0
$\widetilde{G}^{\text{B28}}_{surf\text{-}fit}$	-3.1e4	-577	-59	-5.9	0.23	0
$\widetilde{C}^{\text{B28}}_{surf\text{-}fit}$	4.2e-5	1.3e-7	-2.8e-9	-6.0e-10	9.7e-12	0
$\widetilde{G}^{\text{B67}}_{surf}$	-6.5e4	-50	-78	-6.9e-2	2.2e-2	0
$\widetilde{C}^{\text{B67}}_{surf}$	4.0e-5	9.9e-10	-6.8e-9	3.7e-11	2.0e-12	0
$\widetilde{G}^{\text{B67}}_{surf\text{-}fit}$	-5.4e4	-62	-4.1	-6.9e-2	2.2e-2	0
$\widetilde{C}^{\text{B67}}_{surf\text{-}fit}$	3.5e-5	1.2e-9	-3.7e-10	3.7e-11	2.0e-12	0

Table 6.1: Fitting parameters according to **Equations 6.15** and **6.16** for the analytical modelling of the non-linear surface admittances.

The same CPW line was also simulated based on the large-signal TCAD data pertaining to sample **B67**. All modelling approaches are compared to measurements in **Figure 6.10**, where is it shown once again that the $EM+Y_{surf}(V)$ model correlates to within 4 dB in terms of $H2$ to the $RLG_{neq}(V)C_{neq}(V)$ model

[8] G_d and C_d set to zero due to harmonic balance convergence issues ($\partial V/\partial t$ not included in the list of basis functions during least squares fitting).

[9] These notations were introduced in **Chapter 4**.

and to the measured data, and the analytical description parameters of $Y_{surf}(V)$ are also given in **Table 6.1** for this sample.

Using instead the $Y_{surf\text{-}fit}(V)$ description yields excellent fitting in terms of $H1$, $H2$ and $H3$ between the $EM+Y_{surf\text{-}fit}(V)$ model and the RF measurements.

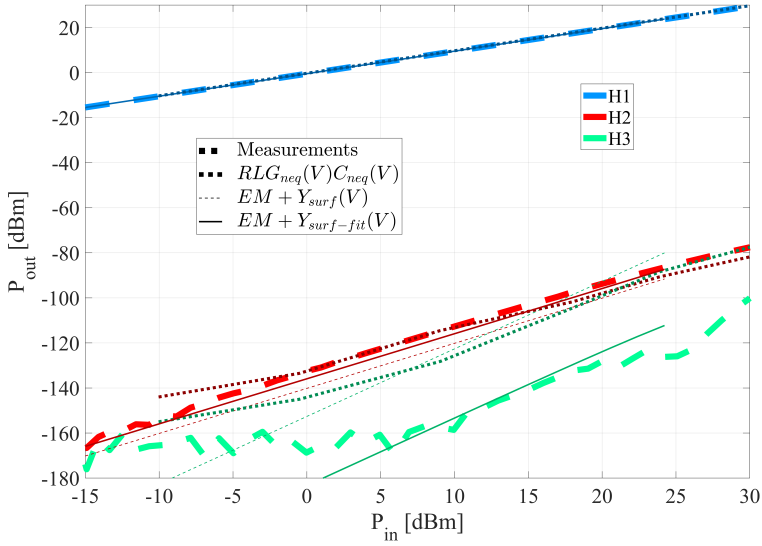


Figure 6.10: Measured and simulated power of the output components of the reference CPW line on sample **B67** for a 900 MHz input signal of power P_{in}. Low noise floor (-170 dBm) measurements courtesy of Incize **[152]**.

For both the **B28** and **B67** samples the main modifications between the $Y_{surf}(V)$ parameters and the $Y_{surf\text{-}fit}(V)$ parameters are slight increases in the G_1 and C_1 terms (in order to raise $H2$ by a few dB) and a severe decrease in the G_2 and C_2 terms (in order to decrease $H3$ by a few tens of dB).

Notice how the G_1 and C_1 terms are approximately one order of magnitude lower for the **B67** eSI100^{TM} substrate than for the **B28** eSI80^{TM} substrate, since it presents 20 dB lower harmonic components.

The large-signal simulations of the CPW line on both the **B28** and the **B67** samples make use of the same *BEOL EM simulation*. Separate substrate EM simulations are run for both samples however, using $\rho_{Si} = 5$ kΩcm for **B28** and $\rho_{Si} = 40$ kΩcm for **B67**.

Now that the $Y_{surf\text{-}fit}(V)$ functions have been calibrated to fit well to the canonical CPW line structures, we shall use these same functions in the $EM+$

$Y_{surf\text{-}fit}(V)$ methodology to simulate other two-port layouts under 900 MHz large-signal excitation and compare the results to measured data.

6.2.2 Crosstalk Structure

The first non-canonical 2-port structure under consideration is the crosstalk device whose layout was presented previously in **Figure 6.5** (**pg. 225**) of **Section 6.1.2**.

The model to hardware correlation using the $EM + Y_{surf\text{-}fit}(V)$ approach for samples **B28** and **B67** are plotted in **Figure 6.11**, using the same non-linear $Y_{surf\text{-}fit}(V)$ that were used in the CPW line simulations.

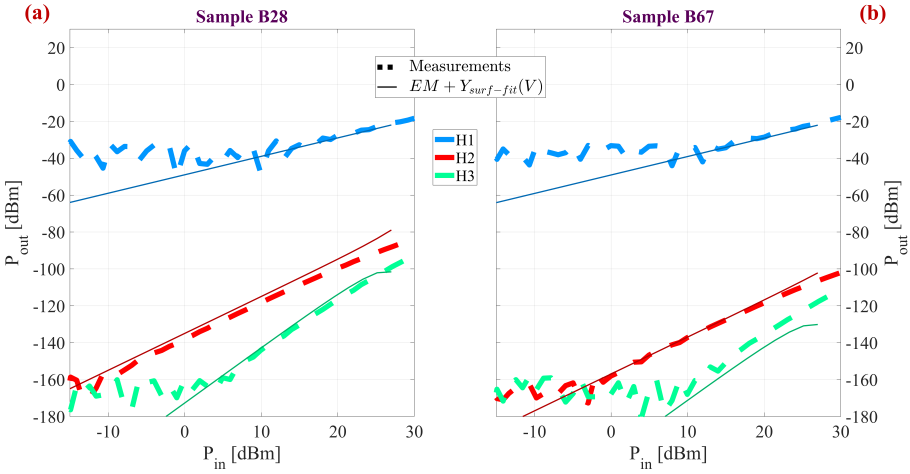


Figure 6.11: Measured and simulated power of the output components of the crosstalk structure on samples **B28** and **B67** for a 900 MHz input signal of power P_{in}. Low noise floor (-170 dBm) measurements courtesy of Incize **[152]**.

Figure 6.11 shows that the large-signal model fits well to the measured data. For both substrates the $H1$ component is accurately reproduced by the model to within 0.8 dB.

For the **B28** sample, at +15 dBm of P_{in}, the difference between model and measurements is of 3.3 dB in $H2$ and of 2.0 dB in $H3$.

For the **B67** sample, at +15 dBm of P_{in}, the difference between model and measurements is of 0.7 dB in $H2$ and of 5.5 dB in $H3$.

6.2.3 Inductive Meander Line

Another non-canonical 2-port structure considered for large-signal modelling is the inductive meander line whose layout is represented in **Figure 6.12**. The meander line conductor width is 16 µm and the lengths of the vertical segments are 384 µm with a 15 µm spacing between them. The distance to the ground lines is 50 µm.

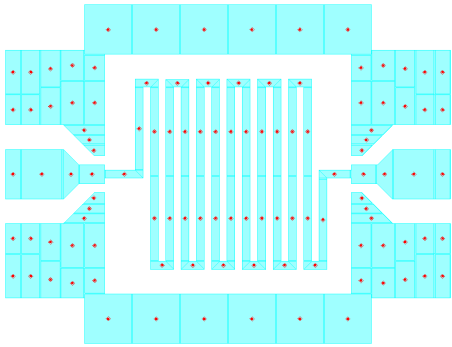


Figure 6.12: Two-port meander line layout and representation of the EM ports ($N = 110$).

The model to hardware correlation using the $EM + Y_{surf\text{-}fit}(V)$ approach for samples **B28** and **B67** are plotted in **Figure 6.13**, using the same non-linear $Y_{surf\text{-}fit}(V)$ that were used in the CPW line and crosstalk simulations.

Figure 6.13 shows that the large-signal model fits well to the measured data for both substrates in terms of the the $H1$ component, that is accurately reproduced by the model to within 0.2 dB.

For the **B28** sample, at +15 dBm of P_{in}, the difference between model and measurements is of 7 dB in $H2$ and of 8 dB in $H3$.

For the **B67** sample, at +15 dBm of P_{in}, the difference between model and measurements is of 6 dB in $H2$ and of 7 dB in $H3$.

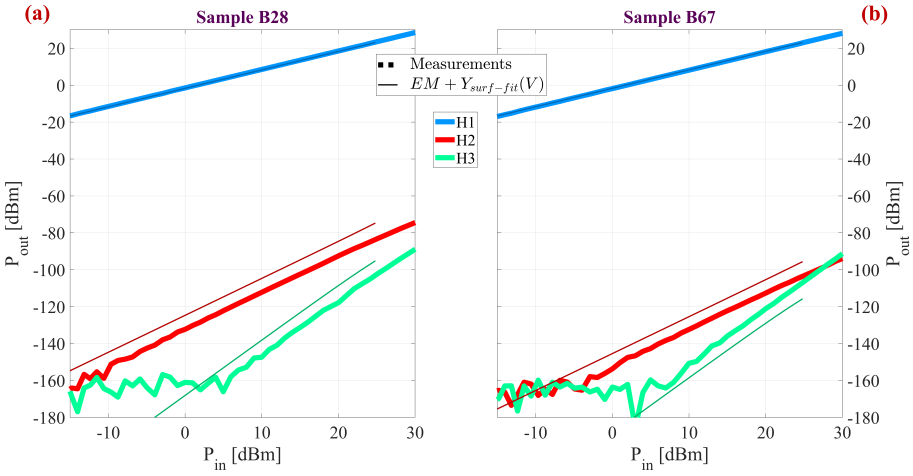


Figure 6.13: Measured and simulated power of the output components of the inductive meander line on samples **B28** and **B67** for a 900 MHz input signal of power P_{in}. Low noise floor (-170 dBm) measurements courtesy of Incize **[152]**.

6.2.4 Recap

Table 6.2 recaps the model to hardware correlation for the three considered layouts at 900 MHz using the $EM + Y_{surf\text{-}fit}(V)$ approach, in which all data is expressed in dBm and is taken a +15 dBm of fundamental input power.

		CPW		Crosstalk		Meander	
		Meas.	Model	Meas.	Model	Meas.	Model
B28	$H1$	+14.6	+14.6	-33.2	-34.0	+13.5	+13.3
	$H2$	-82	-84	-109	-106	-102	-95
	$H3$	-110	-113	-130	-128	-131	-123
B67	$H1$	+14.6	+14.6	-33.3	-34.0	+13.2	+13.3
	$H2$	-102	-104	-128	-127	-122	-116
	$H3$	-138	-141	-150	-155	-135	-142

Table 6.2: Recap of the model to hardware correlation for the three considered layouts using the $EM + Y_{surf\text{-}fit}(V)$ approach. All data is expressed in dBm and is taken a +15 dBm of fundamental input power at 900 MHz.

For a given substrate, **B28** or **B67**, the fundamental output fundamental power $H1$ varies by more than 45 dB for the different layouts, and the harmonic components $H2$ and $H3$ vary by more than 20 dB. The proposed $EM + Y_{surf\text{-}fit}(V)$ modelling approach captures the harmonic components of the output spectrum to within 7 dB of the measured data using the same $_{surf\text{-}fit}(V)$ for the simulations of the three very different 2-port layouts.

6.3 Chapter Summary

In this chapter, non-linear *surface impedance* elements were combined with an EM solver in order to propose a methodology enabling the simulation of substrate-induced non-linearities in an arbitrary layout.

The non-linear *surface impedance* elements were obtained from a TCAD tool and capture the non-equilibrium carrier response at the semiconductor substrate interface.

The EM tool calculates all linear electromagnetic interaction between all parts of the layout and through the linear substrate region (i.e. below the non-linear interface elements).

The methodology was first applied to CPW lines to verify the validity of the approach and to calibrate the non-linear surface element model.

It was then employed to simulate two complex passive RF layouts, significantly different from CPW lines, and from one another: a two-port crosstalk structure and an inductive meander line.

Model to hardware correlation was discussed for these devices on RFeSI80^{TM} and RFeSI100^{TM} substrates. Significantly different harmonic power levels are measured (at 900 MHz) between these different 2-port layouts, and the modelling approach captures well the layout's impact, correlating to the measured HD of all devices to within a few dB (maximum discrepancy of 7 dB).

To the author's knowledge, no simulation flow has yet been proposed in the current literature (2020) capable of offering a complete non-linear evaluation of a full layout's impact on an IC module's distortion.

It is then believed that such a simulation flow could be of high relevance to the EDA and IC design community, in particular for RF and mm-wave FEM's that have increasingly stringent linearity requirements.

Note that this chapter investigates the proposed simulation flow on few layouts, and at a single frequency, and only on TR substrates. Further work is required to rigorously evaluate this flow, especially when considering different types of RF substrate solutions.



7. Conclusion and Perspectives

Conclusion

Summary

At high frequency, the accurate modelling of parasitic elements is crucial to IC design.

Substrate behavior is a significant contributor to such parasitics, and its modelling is a challenge, not only under small-signal conditions due to strongly non-uniform resistivity profiles in semiconductor materials, but especially under large-amplitude excitations.

In this work, substrate impact on a variety of pertinent integrated devices was studied, under both small- and large-signal conditions.

To do so, the effective resistivity and linearity parameters were defined as RF substrate figures of merit, and their extraction procedures were described.

These figures of merit serve as reliable indicators of substrate loss, coupling, and induced signal distortion. It is required that such considerations be kept under careful control in front-end circuitry for advanced telecommunication applications that have stringent spectral cross-contamination specifications between adjacent communication bands.

In this thesis, both small- and large-signal modelling approaches were developed to account for such substrate effects.

The developed models are heavily based in material semiconductor physics, and, in this work, the physical charge-balance interplay was rigorously studied, shedding light on the inner workings of a wide range of silicon-based substrates under both quasistatic and strong non-equilibrium transient conditions.

In particular, the developed large-signal modelling scheme is demonstrated to be stable, i.e. to converge in both space and time, and to correlate well to a wide set of measurement data.

The impact of each considered parameter, be it a material parameter (traps, doping, interface charge, etc.), an excitation parameter (signal amplitude, frequency, etc.), or an environment parameter (temperature, dimensions and layout of the structure, etc.), is not only well captured by the model, but the data trends can be fully explained thanks to the deep physical understanding developed in this work, based on a set of key concepts such as *Fermi-level pinning*, *finite carrier inertia*, *drift and recombination time constants*, *partial equilibrium*, *available free carriers*, etc.

Discussion

HD at mm-wave

Trends and Requirements

Next-generation mm-wave telecommunication networks, such as 5G and applications in the automotive sector, will likely require ever more stringent linearity specifications. In this work, the increase in semiconductor-based substrate linearity with increasing frequency was demonstrated above the substrate's slow-wave mode (typically below 10 GHz for the considered substrates of this work).

Measurements and model results at 5.4 GHz of large-signal fundamental demonstrated a 25-30 dB increase in the linearity of trap-rich RFeSI^{TM} type substrates over data obtained at 50 MHz of fundamental frequency (**Figure 5.21 pg. 204**). The model predicts that such substrates should present 25 dB higher linearity at 28 GHz than at 900 MHz.

This means that the current commercialized trap-rich RFeSI70^{TM} to RFeSI100^{TM} products might well fulfil the linearity requirements as mm-wave 5G substrates, even though mm-wave 5G requires more linear solutions than the current RF 4G, for which the RFeSI^{TM} substrates were originally developed.

Characterization

In the large-signal experiments of this work, distortion simulations were offered up into the mm-wave range, while measurement data was limited to 5.4 GHz. As future work, model correlation to higher frequency data (at 28 GHz and above) is of high relevance, as at such frequencies: (i) the distributed nature of the passive devices becomes even more apparent, (ii) the series metallic losses increase significantly, and (iii) the dielectric relaxation frequency is achieved for substrates of even quite low resistivities.

Model Limitations

The developed model has a finite validity domain, and has not yet been demonstrated to account for several physical phenomena and their impact on the RF distortion levels. In particular, several important limitations of the model in its current form are highlighted here below.

Limited to CPW Geometries (so far)

The validated physical model is fundamentally based on a combination of 2D TCAD time-domain simulations. For these reasons, it is limited to geometries that are uniform in the 3rd dimension, and has only been applied

to CPW lines, for which the EM propagation terms can be modelled through closed-form expressions.

Though **Chapter 6** discusses a possible extension of the model to other types of 3D layouts, that approach comes with some hypotheses on the structure and substrate material, and is not (as of yet) a fully validated methodology.

Modelling of the Third Harmonic $H3$

In this work, the model fitting to HD measurements was performed with $H2$ as the sole fitting parameter, and, in general, the model to hardware correlation in terms of $H3$ (and other higher order harmonic components) was not considered. Multi-parameter fitting may be achievable for the model (in terms of $H2$ and $H3$ simultaneously, for example) but has not been demonstrated in this text, and constitutes future work.

Anomalous HD Substrate Behavior ("Dips")

Some substrates investigated during this research present Hk vs $H1$ curves that present different slopes than k:1. Such seemingly anomalous data has not been printed in this text, though in practice such trends cannot be said to be *extremely rare* occurrences. They are usually observed in trap-rich types of substrates that present low trap densities (i.e. a strong anneal process step) or high polysilicon contamination levels. Then it is quite typical for a characteristic *"dip"* in the Hk vs $H1$ curves to arise.

The model has predicted such dips under certain simulation conditions, though no wide-parameter-fitting was achieved to data from a measured sample.

"Dips" in HD curves were discussed in **[97]**, though we (the authors) no longer stand 100% behind the physical explanations given in that paper. Future research is warranted to understand the physical origins of such measured (and repeatable, on certain types of samples) HD behavior.

$H3$ Dependency on Contact Resistance

During on-wafer HD measurements of CPW lines, the $H3$ component is observed to vary strongly with contact quality, while the $H1$ and $H2$ are appreciably less sensitive.

In practice, the signature of a *"bad contact"* is hardly noticeable in the measured $H1$ and $H2$ data, while the $H3$ data is usually several tens of dB higher than when a *"good contact"* is in place. Usually, if the probe pads have had little use then the HD measurements are of good quality. However, when a DUT is heavily reprobed, the measured $H3$ depends strongly on the probe contact. The probe station operator is required to remain vigilant during HD

measurements with respect to such $H3$ behavior (in this work, some DUTs were heavily reprobed, being measured at multiple temperatures and fundamental frequencies).

The physical origin of this behavior is as of yet unknown, and adding resistive elements to the TCAD tool in an attempt to capture such behavior did not yield any fruitful results. Understanding this phenomenon is of interest to the community, and exploring its origins using the developed model is a path for future work.

Computation Time

The model approach is quite computationally expensive.

When running on 4 threads of a 2.20 GHz Intel® Xeon® Silver 4214 processor a single simulation point (i.e. at a given fundamental frequency, power-level (signal amplitude), DC bias point and temperature) of a CPW line (of length L), simulated over 10 signal time periods using 32 points per period, takes around $3.5 \cdot K$ hours, where K is the discretization factor in the direction of propagation equal to $K = L/\Delta z$ (combination of a series of short line length simulations of unit length Δz, see **Figure 4 pg. 127**). Concatenating 4 unit-length simulations then takes approximately 14 hours for the simulations of this work[1].

Extracting an equivalent circuit type of representation is then highly desirable, since including the full TCAD formulation in an IC design flow seems unreasonable with such long computation times. This was touched upon in **Chapter 6**, and is discussed as a perspective below.

[1]The TCAD mesh used is a little aggressive to ensure an accurate and converged solution. Some computation time can likely be gained by relaxing the it a little, although the mesh used is not far from the recommended guidance provided for the TCAD flow.

Perspectives

Several future endeavors of pertinence can be highlighted from the discussions in this thesis.

Applications

RF/mm-wave Substrate Development

The physical understanding and models of this text can be used to orient the development of future semiconductor substrate stacks. As immediate applications we can cite the development of GaN buffer layers grown on Si wafers, and the integration of FD-SOI on an RF substrate solution. In all cases that target RF frequencies and above, the impact of material interface and bulk parameters on the substrate's effective resistivity and linearity must be evaluated, and material-engineered solutions can be oriented by relying on the developed model.

Potential for RFIC Design

The large-signal model was validated extensively for the case of a CPW line, by combining the telegraph equations with TCAD results.

A method for extending the model beyond transmission lines to arbitrary layouts was explored in **Chapter 6**, where an EM solver was combined with the 2D TCAD results. This approach merits further work and validation, and, if proved to be robust, could find a practical application in an EDA design flow for RFIC designers.

Future work includes combining this methodology with active RF device models (from a foundry PDK) in the context of a front-end module to simulate the post-layout behavior of the circuit including the substrate's impact on the overall linearity performance. In **Figure 2.13** (**pg. 55**) the substrate's impact was demonstrated through measurements of a 5 GHz SPDT module by comparing the device fabricated on a HR wafer tho the same device on a TR wafer, with more than 15 dB linearity difference being observed between the two. The proposed EDA design flow really aims to capture such effects, and model to hardware correlations against measurements such as those constitute important next steps to validate the flow and to demonstrate its pertinence for a practical use-case of an RF SPDT switch design.

This way, the dominant contribution to non-linearity can be identified (active

devices vs. semiconductor substrate) for specific circuit modules, and substrate requirements can be determined and tailored to best suit these applications (HR, eSI70^{TM} to eSI100^{TM}, other).

Additional Considerations

Need for Accurate Trap Characterization

Since the non-linear model is based on physical material parameters, an accurate description of spatial and energy distributions of traps is required to make the most of the tool toward substrate analysis and design. However, extracting trap distributions from interfaces or volumes is a challenge when the Fermi-level is tightly pinned, i.e. when many traps are present, and this is usually the case for effective trap-passivated RF substrate solutions. It is then difficult to modulate trap occupancy through purely electrical stimuli, and other methods are then sought (such as techniques based on optical and/or thermal stimuli followed by transient spectroscopy).

The accurate extraction of trap parameters is required to take full advantage of the capabilities of the models developed in this work.

Other (Passive) Sources of HD

As substrates become more linear, as required by advanced generations of telecommunication standards, designers should remain vigilant with regard to the sources of signal distortion, which may not in all cases be dominated by the E-field dependence of the resistivity profile $\rho(E(x,y,z,t))$.

One example is non-linear permittivity that arises from the fact that in many materials the polarizability can saturate under high electric field. Then, the relation between the applied E-field and the material's polarization field P may no longer be strictly written as a linear relation of the type $P = \varepsilon_0 \chi_e E$, with the linear electric susceptibility χ_e being treated as a constant. In **[153, 154]** non-linear electric susceptibilities $\chi_e(E)$ of various sintered ceramics and glass ceramics were measured in the microwave frequency range under large-signal conditions. Such characterizations serve in the industry to develop filters with low harmonic crosstalk (between transmitter and receiver channels) for applications in cellular base stations **[155]**.

Another example is metal non-linearities when driven by large-amplitude RF currents that modulate the material's temperature, and hence its resistivity in time with the signal $\rho(T(I(t)))$.

While the main focus of this work was placed on the non-linearity of material resistivity as a function of the applied field $\rho(E(x,y,z,t))$ -which was considered to be dominant in all investigated substrates of this text-, other material sources of non-linearities may become significant, if not dominant, in next generation substrates, and or in different operating conditions (frequency, temperature, etc.).

ρ_{eff} at mm-wave

The metric of effective resistivity has been shown to be highly convenient for evaluating and benchmarking RF substrate performance. We note that its extraction can be slightly improved in some practical cases, such as:

1. When the CPW line is not implemented in continuous metal planes, but rather is made up of a mesh-array of shapes in order to satisfy foundry process design rules. In that case, the geometrical factors of F_{top} and F_{bot} (see **Section 2.1.2**) could be updated for higher accuracy results, based on the conformal mapping work proposed in **[156]** that models meshed CPW structures.
2. At high frequencies the geometrical factors F_{top} and F_{bot} may have some slight frequency dependencies caused by the presence of higher order modes. In some cases, F_{top} and F_{bot} can be updated to account for such dispersions based on the formulae proposed in **[157]**. The frequencies at which such considerations should be taken into account depend mainly on the CPW dimensions and on the substrate thickness (distance to a metallic measurement chuck), and for the main CPWs considered in this text, the procedure should be updated for parameter extractions targeting the high-end mm-waves/sub-THz range and above. At mm-wave frequencies, the existence of parallel-plate modes in on-wafer probed CPW lines of similar dimensions to those considered in this work is suggested to impact on the overall line losses starting already from several tens of GHz **[158]**.

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Appendices

A SRP Measurements and Simulations

This appendix aims to provide an overview of the general *Spreading Resistance Profile* (SRP) measurement technique as well as the way in which SRPs are simulated throughout this work.

A.1 SRP Measurement Principle

To perform an SRP measurement on a sample the wafer must first be ground to a bevel and polished along a shallow angle. Then, a small pair of probe needles are dragged along the beveled surface and the resistance between them is recorded. This principle is illustrated in **Figure 7.1**. The probe tips are usually spaced by a distance of the order of 100 µm.

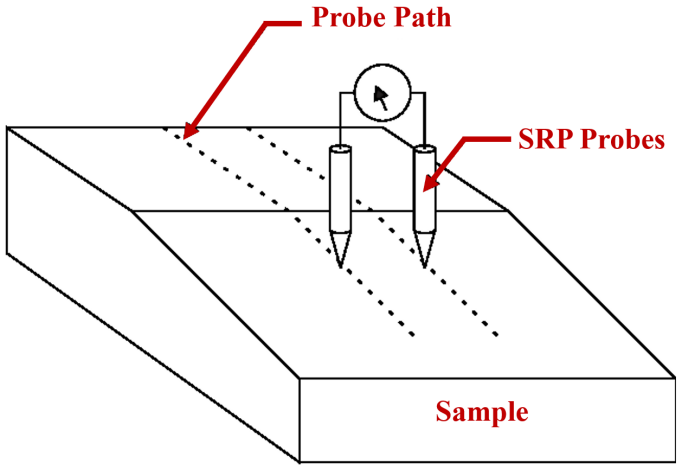


Figure 7.1: Concept of SRP measurements. From **[132]**.

The measured resistance is then converted into local resistivity at each probing location, and is performed knowing the geometrical factors involved that are determined by the probe's dimensions. In advanced SRP measurement set-ups a deconvolution algorithm is applied to account for local resistivities around the probes impacting the measured resistance at the considered location.

In practice, the bevel angle is usually shallow, between 10° and 15°, in order to achieve good spatial resolution in depth into the sample.

SRP curves in HR samples are not affected by the presence of oxide charges, as can be understood from **Figure 7.2** depicted here below, where it is plain

to see that any fixed charges at one of the top interfaces will not induce free carriers in the semiconductor bulk, as the material probed along the y' axis with a shallow angle α is then far from those charges, that are compensated for by induced free carriers within a few hundred nm (for usual fixed interface charge density levels).

The thickness of a polysilicon trap-rich layer is usually between a few hundred nanometers and several microns, and relevant data can be obtained over such depths during SRP measurements.

A.2 SRP Emulation using TCAD

In this work, measured SRPs are compared to simulated resistivity profiles. Because the different materials and their interfaces affect the vertical resistivity profile, the structure of **Figure 7.2** is simulated in a TCAD tool in order to extract resistivity along an air interface, as is the case during physical SRP measurements. This approach is supported by the findings in **[159]** that report on appreciably different carrier distributions, and therefore SRP results, along the bevelled sample than in the full sample.

By probing the resistivity along the cutline illustrated in white in **Figure 7.2**, the $\rho(y')$ data is extracted. In the figures of **Chapter 5** (**Figures 5.9, 5.11 and 5.22**) the simulated SRP is obtained in this manner, where $\rho(y)$ is plotted against the depth axis $y = y' \sin\alpha$.

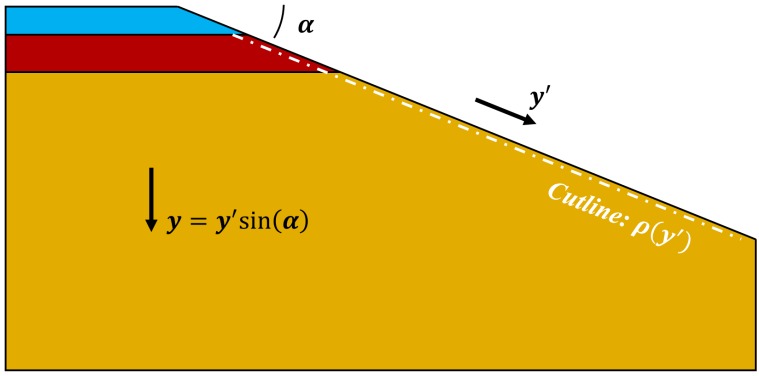


Figure 7.2: Cross section of a bevelled layered-heterostructure for resistivity profiling. Such a structure is simulated in this thesis to extract resistivity profiles along the bevel to compare to measured SRP data for samples **B28**, **B45**, **B46** and **B67** in **Chapter 5** (see **Figures 5.9, 5.11 and 5.22**).

B Large-Signal RF Measurement Set-Up

Figure 7.3 depicts the large-signal harmonic distortion set-up based on a Vector Network Analyzer.

In practice in this thesis five different set-ups were implemented, each corresponding to a different fundamental input tone frequency of either 50 MHz, 250 MHz, 900 MHz, 2.5 GHz or 5.4 GHz.

Each set-up sweeps the input power to the DUT from -30 dBm to +25 dBm.

Since the VNA, a four port PNA-X 26.5 GHz in our case, cannot sweep up to +25 dBm a power amplifier (**PA**) of fixed gain is connected between the **DUT** and the VNA's source **[93]**.

Since the **PA** is non ideal it is responsible for distorting the signal, introducing harmonic components due to its own non-liniarities. The signal must the be purified before being fed to the **DUT**, and this is achieved using pass-band **filters** centered around the fundamental frequency f_0 with significant attenuation at all harmonic frequencies of interest for measurements at $N \cdot f_0$.

At the measurement side, the VNA's **Receivers** have a maximum specified handling power above which they risk being damaged. It is then necessary to attenuate the received signal by a fixed amount, using controllable precision **attenuators** available in the PNA itself, before measuring its power. This is depicted in the signal path to **Receiver B** in **Figure 7.3**. Unfortunately, **Attenuator B** may attenuate the harmonic components to a level below the set-up's noise floor, such that they cannot be measured at **Receiver B**. This is of particular concern for measuring the low harmonics considered in this work originating from RF substrates, some of which are very linear.

A second path is then defined towards **Receiver D**. In this signal path, high-pass **filters** are inserted that serve to remove the fundamental frequency while preserving the harmonics. With the high-power fundamental removed, **Attenuator D** can be set to a low value (even to 0 dB), thereby lowering the noise floor and allowing **Receiver D** to pick out the harmonic power components down to quite low values.

The HD measurements are then performed in two steps. First, the input power $H'1$ is swept and the fundamental output power $H1$ is measured at **receiver B**. Second, the input power $H'1$ is swept over the same range and the harmonic component output power levels $H2$, $H3$, etc are measured at **receiver D**.

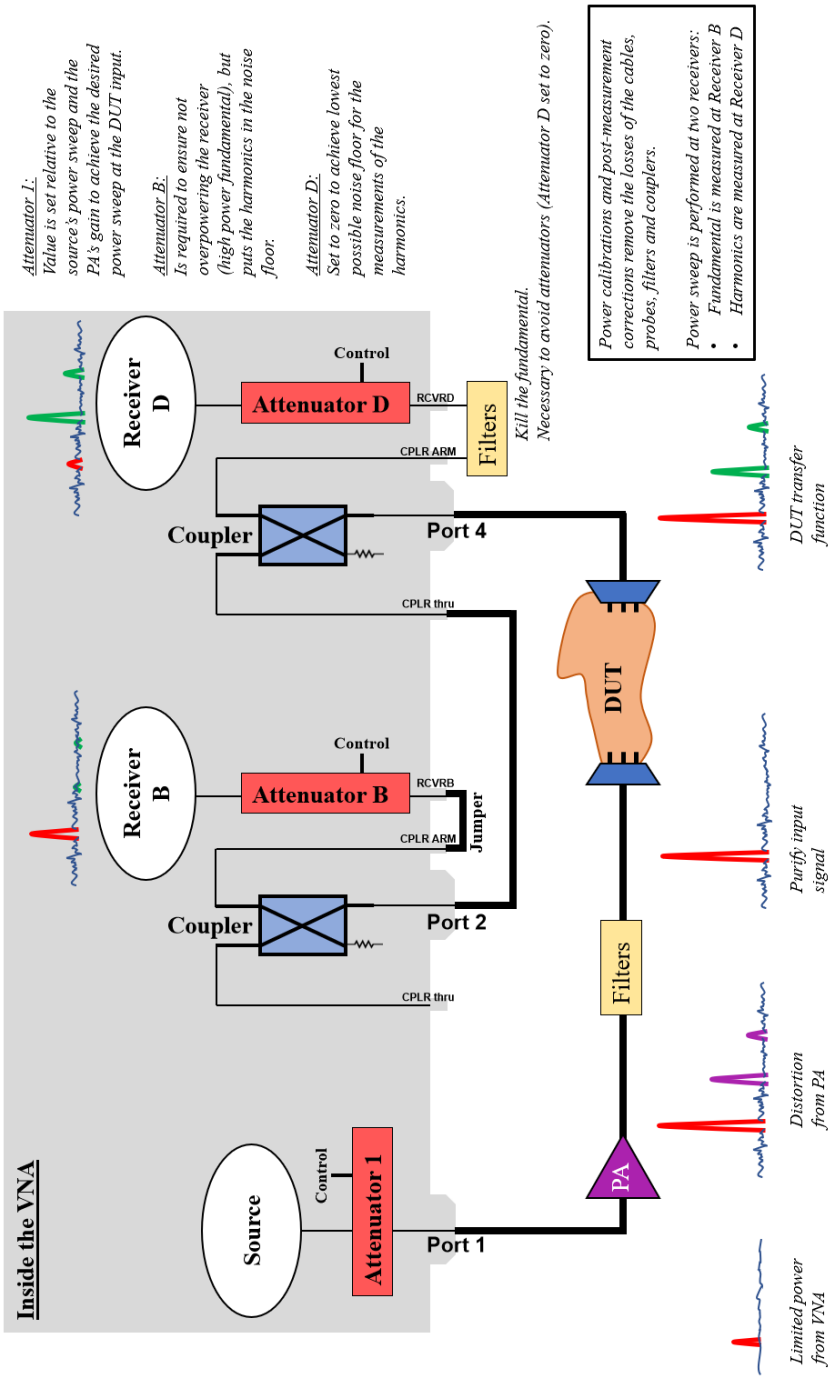
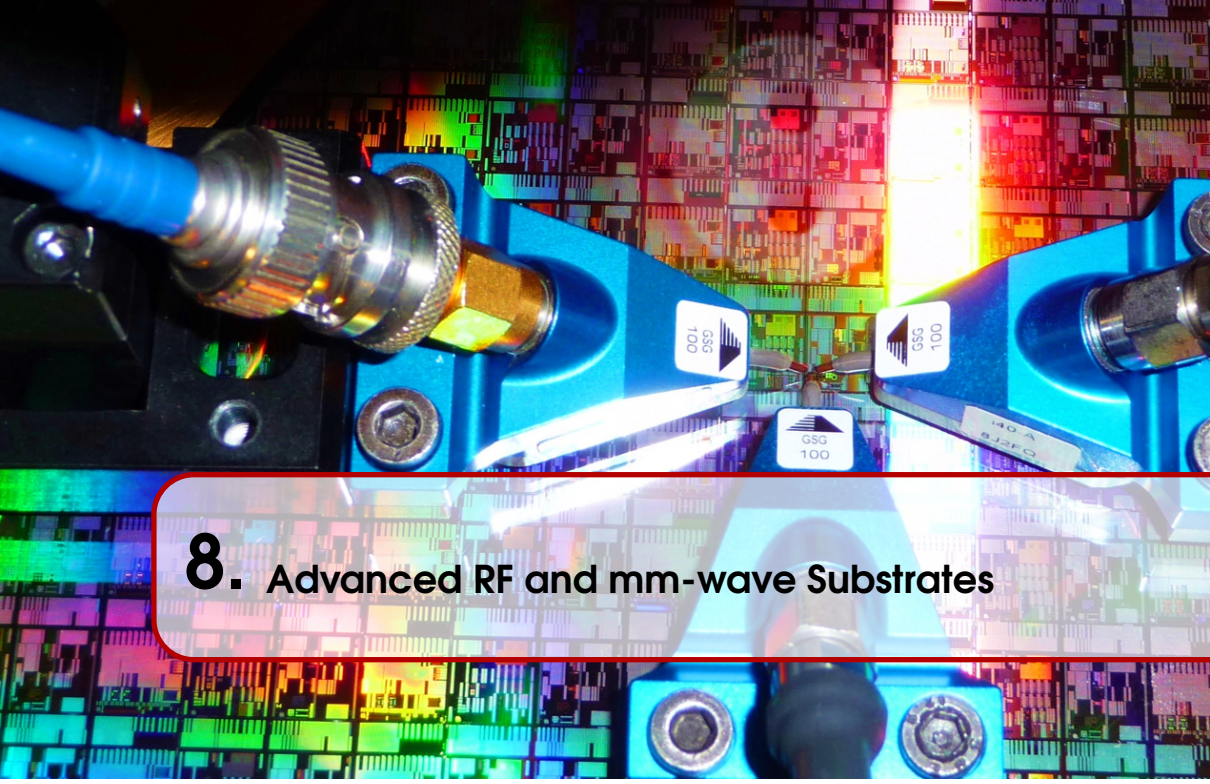


Figure 7.3: Practical implementation of the RF single-tone on-wafer harmonic distortion set-up.



8. Advanced RF and mm-wave Substrates

8.1 Introduction

This appendix chapter serves to review the various silicon-based substrate solutions that are published in the literature for RF and mm-wave applications.

So far, the focus of this thesis has been on the most common types of substrate processed in CMOS foundries: standard-resistivity silicon (Std), high-resistivity silicon (HR), and trap-rich RFeSI^{TM} SOI.

However, extensive research exists on other silicon-based solutions, to tackle low-free carrier densities at the interface, or even in the bulk, to create low-loss and highly linear wafers.

This chapter then aims to review all relevant solutions, that can be broadly categorized into two types of approach: (i) interface passivation of HR-Si, and (ii) bulk passivation of Si.

Furthermore, several novel RF substrate solutions were developed as part of this work, and both simulation and measured data are offered in this chapter to demonstrate the performance of the novel concepts.

8.1.1 Interface Passivation

Interface passivation schemes invariably take place at the Si/SiO_2 boundary in HR wafers, as they address the PSC effect that is responsible for degrading their RF performance. They can be arranged based on their physical working principles into the following categories:

1. **Deep-level traps** at the interface. When properly engineered, such traps can provide charge compensation at the interface and avoid a PSC layer formation. Several approaches are based on this principle:
   - Trap-rich **polysilicon deposition** was the first proposed PSC passivation technique [72], and has had a lot of traction since then [34, 37, 42, 44, 45, 91, 160]. This is the implementation used in RFeSI^{TM} SOI commercialized by Soitec, as has been extensively detailed in this text.
   - Trap-rich **amorphous silicon deposition** was naturally proposed as an alternative passivation technique, and has demonstrated similar quality as polysilicon [42, 161, 162]. It has had much less industrial traction than polysilicon, which may largely be due to its reduced stability to withstand high thermal process budgets.
   - High-energy **Argon implants** that damage the interface and introduce defects (sometimes referred to a *surface silicon amorphization*) has also been considered as a PSC passivation technique [160, 161, 163–169]. It has received some industrial interest [169], and its capacity to implement trap-rich type interfaces locally is attractive for some applications, as compared to the above solutions that necessarily passivate the wafer over its entire surface by construction.
2. Smart **patterns of doped P and N** regions can be implemented such that an array of depletion junctions is induced at the surface that strongly increase interface impedance [170–172]. This concept yields RF substrates of significantly higher quality than HR suffering from PSC, though not as high as trap-rich interface passivation solutions. Measured and simulated RF substrate FoMs will be presented and discussed in Section 8.2.
3. A **field-effect** passivation, by which a DC bias scheme is applied to lower level layers to control the surface impedance at the Si/SiO_2. Various pattern and biasing schemes can be used to passivate the PSC effect, and we shall discuss this novel solution further in Section 8.3.

8.1.2 Bulk Passivation

Bulk passivation solutions address both interface loss and bulk loss mechanisms. Then, bulk passivations are not required to start from high resistivity wafers, and in fact usually start from lossy silicon (Std or other). They can be arranged based on their physical working principles into the following categories:

1. The introduction of **deep-level traps** throughout the entire bulk-Si volume. When engineered correctly, this scheme can turn lossy silicon into a highly-resistive material. The traps offer a charge compensation mechanism at each point in the silicon bulk, ensuring low free carrier densities and hence a state of high resistivity. The traps are introduced using carefully selected impurities that are implanted at the wafer surface and then diffused throughout the entire bulk using a high-temperature anneal step. Two main impurities have been considered in the literature to passivate lossy silicon and turn it into a high quality material for RFIC applications:
   - **Gold (Au) -compensated** RF substrates fabricated from standard resistivity N-type silicon **[134, 135, 139–142, 147, 148]**. Measurement and simulation results of such substrates will be presented in **Section 8.4**, where the physical mechanisms at play are analyzed, enabling us to model and understand how the introduction of deep Au trap levels produces a highly linear and low-loss substrate.
   - Similarly, the effectiveness of **proton (H^+) -compensated** silicon was demonstrated in **[173–175]** to produce high-resistivity substrates. In those works, measurements of RF measurements confirmed the beneficial impact on the quality of integrated passive devices.
2. Substrate transformation through **silicon porosification** has been extensively investigated for RF applications **[86, 176–200]**. When correctly optimized, porous silicon presents excellent RF substrate FoMs, first, thanks to large trap densities present along the pore walls that ensure low carrier density and high resistivity (even when the starting wafers are often highly doped), and second, thanks to a strong reduction in substrate permittivity. Several types of porous silicon have been investigated in this work, and their RF FoMs will be discussed in **Section 8.5**, including porosification starting from Std wafers, and a post-CMOS localized porosification technique.

3. Passivation solutions based on **substrate removal** have also been developed. By replacing underlying silicon volume by air (or sometimes by low permittivity dielectrics), strong reductions in RF losses, substrate coupling and non-linearities are achieved. In other cases, instead of removing silicon matter, the passive devices are fabricated using micromachining processes as suspended structures located significantly above the lossy silicon material. Two main approaches are described here:

   - **Silicon removal through etching** has been demonstrated to produce high quality passive devices in [201–205]. These techniques target post-CMOS process applications
   - **Silicon removal by laser ablation** has been developed in [206, 207] as a post-CMOS step. By removing the lossy silicon material, higher quality inductors were demonstrated in [206], and the positive impact of these devices was demonstrated in an LNA from measured data. Similarly, measurements of switch modules were presented in [207], demonstrating strong linearity improvements thanks to the ablation of the silicon over its entire thickness.
   - Passive devices **suspended above the silicon** substrate have been presented in [208–214] with excellent quality factors. Using micromachining techniques, non-planar structures can be implemented that have negligible fields in the lossy silicon, including complex geometries such as solenoids.

As mentioned above, some of these alternative substrate solutions have been developed, characterized and modelled in the framework of this thesis, they are listed here, and are addressed in the following sections:

• Doped PN patterns	interface passivation of HR	**Section 8.2**.
• Field-effect structures	interface passivation of HR	**Section 8.3**
• Au-compensated Si	bulk passivation	**Section 8.4**.
• Porous Silicon	bulk passivation	**Section 8.5**.

In general, large free carrier densities should be avoided in the substrate materials to achieve high RF performance. This has been profusely discussed in **Chapters 3 and 4** using notably the concept of *available free carriers* based on physical analyses fueled by TCAD simulation and hardware measurements. Similar analyses will be made for the above listed substrate concepts to demonstrate the working principles behind their high-performance RF results.

8.2 PN Depletion Junction High-Resistivity Substrate

In this section, we present the so-called *PN-doped depletion-junction* (DP) substrates for RF applications.

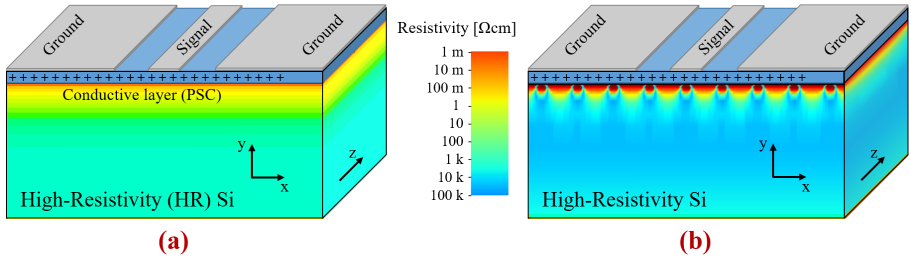
First, the substrate enhancement technique is described. Then, the results of proof-of-concept type demonstrators, fabricated and characterized at UCLouvain, are presented. The final section presents the best expected achievable results using state-of-the art processes (high resolution lithography) that are available in the advanced CMOS fabs of today (2020).

8.2.1 Concept

The concept addresses the PSC effect in a HR wafer, proposing a novel method of passivating it to achieve a low-loss and linear substrate solution.

The technique, which was patented by UCLouvain in 2019 **[170]**, can achieve high RF-substrate performances rivalling those of TR wafers, and relies physically on locally interrupting the PSC channel by inducing a chain series of buried depletion junctions at the Si/SiO_2 interface **[171, 172]**.

This is depicted in **Figure 8.1**, that compares the 2D resistivity profile in a HR substrate suffering from PSC **(a)** and in a DP type substrate **(b)**.



(a) **(b)**

Figure 8.1: Representation of the 2D resistivity profile in a HR substrate suffering from PSC **(a)** and in a DP substrate enhanced with buried PN depletion junctions **(b)**, viewed normal to the PN junctions.

The depletion junctions induced between adjacent P and N regions serve to impede the field propagation in unwanted directions. The conductive PSC path is interrupted which results in an increase of substrate effective resistivity in the direction perpendicular to the buried junctions[1].

[1] The ρ_{eff} of DP substrates is actually *directional*, as will be discussed further on.

8.2.2 UCLouvain Prototypes

Proof-of-concept passive demonstrators were developed, fabricated and measured at UCLouvain.

Fabrication

A total of 11 experimental wafers were processed starting from high-resistivity ($\rho_{nom} > 5$ kΩcm) Si substrates: 9 different DP samples as well as a reference HR sample and a reference TR sample.

First, a thermal oxide of 20 nm is grown atop each wafer in order to prevent channeling effects during implants [215, 216].

Next, a 50 keV phosphorous N^+ implant is performed over the entire wafer with a dose of $1 \cdot 10^{13}$, $3 \cdot 10^{13}$ and $1 \cdot 10^{14}$ cm^{-2} for the **DP -A**, **-B** and **-C** samples, respectively.

A mask is then patterned by photolithography over the top surface, defining resist regions of width WN^+ separated by a distance of WP^{++}, as shown in Figure 8.2.

A 30 keV boron P^{++} implant is then performed with a dose of $1 \cdot 10^{14}$, $3 \cdot 10^{14}$ and $1 \cdot 10^{15}$ cm^{-2} for the **DP -A**, **-B** and **-C** samples, respectively.

The photoresist is then removed and the samples are thermally annealed for dopant activation.

Finally 180 nm of SiO_2 is deposited by PECVD, and a 1 µm-thick aluminum metallic layer is deposited by electron-beam physical vapor deposition and patterned to define the RF passive structures atop the 200 nm of total oxide thickness. The considered devices are CPW lines and crosstalk structures defined parallel and at a 90° angle to the doping lines, as shown in Figure 8.2. The backside of the wafer is similarly metallized with 1 µm-thick aluminum and annealed to provide an ohmic DC contact.

Three doping pattern sizes, WP^{++} and WN^+, were considered: 1 µm and 3 µm for the **-1** samples, 2.5 µm and 7.5 µm for the **-2** samples, 5 µm and 12 µm for the **-3** samples, as illustrated in Figure 8.2.

Table 8.1 recaps the doping parameters and pattern sizes associated to the nine prototype DP samples.

A high-resistivity (HR) and a trap-rich (TR) wafer were also implemented as comparisons to these DP substrates. They are the **HRD1** and **TRu** samples presented previously in Chapter 5.

The implant energies were determined using the Athena process simulation tool from Silvaco. These energies were tailored to implement very thin doped

regions at the Si/SiO_2 interface by implanting through 20 nm of SiO_2. Higher energies will produce deeper N and P regions, and hence wider (in the vertical direction, from the Si/SiO_2 interface) depletion capacitances in between them, which results in lower substrate impedance. By running an Athena simulation followed by an Atlas simulation for each considered pairs of N and P implant energies, the proposed 50 keV and 30 keV were determined to yield the highest ρ_{eff} for a given pattern size (WN^+ and WP^{++} in the present case).

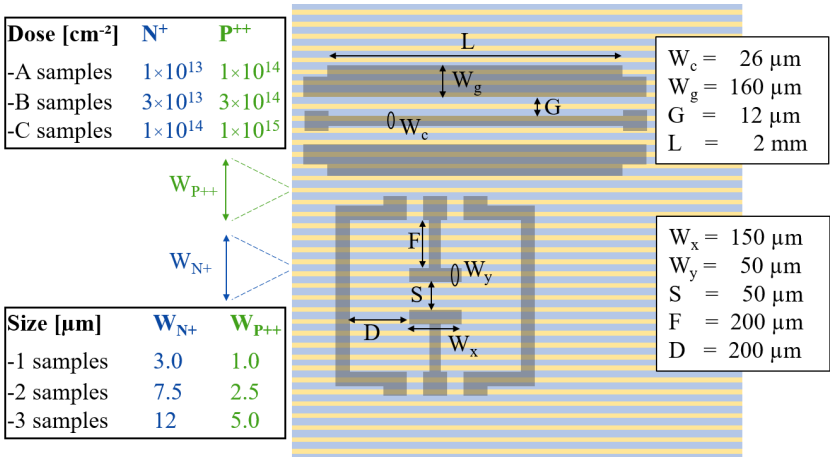


Figure 8.2: Pattern and sizing of the P and N doped regions relative to the CPW and crosstalk structures on the DP substrates.

WP^{++} / WN^+ [µm] / [µm]	Dose P^{++} / Dose N^+ [cm^{-2}] / [cm^{-2}]		
	$1 \cdot 10^{14}$ / $1 \cdot 10^{13}$	$3 \cdot 10^{14}$ / $3 \cdot 10^{13}$	$1 \cdot 10^{15}$ / $1 \cdot 10^{14}$
1 / 3	**DP-A1**	**DP-B1**	**DP-C1**
2.5 / 7.5	**DP-A2**	**DP-B2**	**DP-C2**
5 / 12	**DP-A3**	**DP-B3**	**DP-C3**

Table 8.1: Doping parameters associated to the nine UCLouvain prototype DP samples. All implants were made through 20 nm of thermal SiO_2. The N^+ implants are phosphorous at 50 keV over the entire wafer. The P^{++} implants are boron at 30 keV through the photoresist mask of pattern size WP^{++} / WN^+.

RF Performance: Effective Substrate Parameters from CPW Lines

The depletion junctions induced between adjacent P and N regions impede the field in unwanted directions. The conductive PSC path is interrupted which results in an increase of substrate ρ_{eff} in the direction perpendicular to the buried junctions. **Figure 8.1 (b)** presents the horizontal resistivity profile at the Si/SiO_2 interface in such DP substrates[2]. Although the resistivity in the P and N regions is low, they come in series with the depleted junctions characterized by very low free carrier density that are therefore highly resistive.

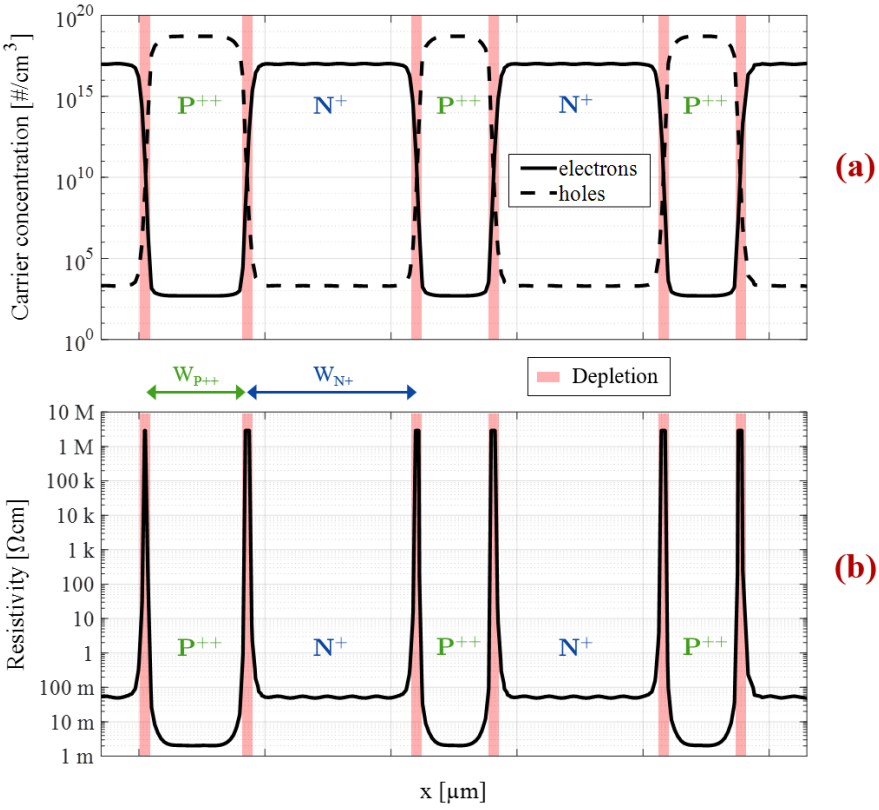


Figure 8.3: Electron and hole concentration **(a)** and local resistivity **(b)** in a DP substrate directly beneath the dielectric.

[2]Such profiles are obtained from Athena simulations of the full process flow described above, for each considered energy, dose and doping pattern size.

This is illustrated in **Figure 8.3** which presents the carrier concentrations and local resistivity as a function of the horizontal direction directly beneath the oxide, in which the red zones highlight the depletion regions that dominate the overall substrate impedance.

The red regions in **Figure 8.3** are defined as any region in which the local resistivity is higher than 300 Ωcm. Since these regions dominate the substrate impedance, it is desirable to have a large proportion of depleted volume, i.e. a large proportion of red colored regions[3].

Measurements and simulations of CPW lines are plotted in **Figure 8.4**.

Due to the PSC effect, the HR substrate presents low ρ_{eff}, high α (mainly shunt substrate losses), and $\varepsilon_{r,eff}$ and Z_C that converge towards 11.7 and 50 Ω at high frequency, respectively, as the propagation shifts out of the slow-wave mode. The TR sample shows high performance with ρ_{eff} above 5 kΩcm and low α (mainly series metallic losses).

The DP substrates show increased performance compared to the HR wafer.

The **DP-A1** sample shows the best performance values of all nine DP wafers because it has the highest density of PN junctions between signal and ground lines of the CPW, and because it has the widest depletion junctions due to it using the lowest doping levels[4]. It presents a high ρ_{eff} in the range of 2 kΩcm at 5 GHz and hence low total lineic RF losses α. The PN junction density in the **-1** samples is one per 2 µm (in the x-direction, see **Figure 8.3**), yielding 6 junctions between the signal and ground lines of the CPW[5] that drastically increase the substrate impedance between these parts of the RF device.

Athena process simulations estimate the depletion width of each junction of the **DP-A1** sample to be around 140 nm (defining here *depletion* as regions in which $\rho > 300$ Ωcm). The proportion of depleted volume in the interfacial silicon layer is then 7% density (140 nm / 2 µm). For prototype fabrication, this density was limited by the lithography resolution available in the university cleanrooms. Simulation results pertaining to a lithography available in state-of-the-art CMOS processes will be presented further on in **Section 8.2.3** where interfacial depletion densities higher than 40% are shown to be achievable (thanks to smaller WN^+ and WP^{++}).

[3] In a TR substrate the entire interface would be red, with a 100% proportion, at a value of 1 to several tens of kΩcm.

[4] Lower doping levels give better results due to wider depletion regions. However, lower doses are less robust against high densities of oxide charge, and too low doses risk not being sufficient to combat the PSC effect. This will be discussed further in **Section 8.2.3**.

[5] For the reference CPW line with a spacing S of 12 µm.

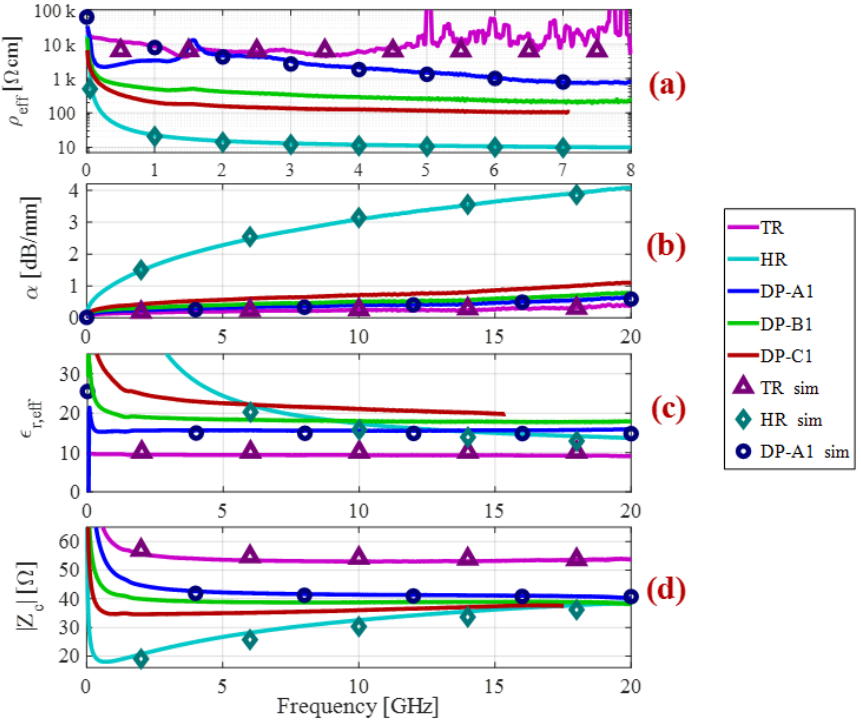


Figure 8.4: Effective electrical substrate parameters extracted from RF measurements of CPW-lines biased at 0 V DC. **(a)** Effective resistivity. **(b)** Lineic line losses. **(c)** Effective relative permittivity. **(d)** Characteristic line impedance.

Though they show lower performance than the **DP-A1** substrate, the higher-doped **DP-B1** and **DP-C1** samples still show significant improvement over the HR wafer. Due to the higher doping levels in the N and P regions, the interfacial depletion densities of samples **DP-B1** and **DP-C1** are respectively 4% and 2.5%, and consequently their ρ_{eff} values are lower.

Because the conductivity in the P and N regions is very high they can be consider as local equipotential regions. This has the effect of concentrating the E-field in the small depletion volumes in between them, which translates to a higher $\varepsilon_{r,eff}$ sensed by the overlying coplanar technology. Though undesired, the increase in $\varepsilon_{r,eff}$ is acceptable, as the **DP-A1** substrate presents a value of 15.6. Although this value is larger than the relative permittivity of silicon (11.7), it is a worthwhile trade-off enabling a 200-fold increase of the ρ_{eff} as compared to HR. For this reason the CPW-line of these DP-substrates are no

longer matched to 50 Ω and present Z_C values closer to 40 Ω[6].

Because there is then a series *RC* network at the interface, its impedance, which dominates the effective resistivity, decreases as frequency increases (and this frequency dependence is stronger for wider depletion regions). **Figure 8.4 (a)** shows such a $\rho_{eff}(f)$ trend for sample **DP-A1**, and that the TCAD simulations accurately model the impedance of such substrates over a wide band. A kink in the $\alpha(f)$ curves in **Figure 8.4 (b)** at around 14 GHz is a direct consequence of the $\rho_{eff}(f)$ behavior, as substrate losses increase as ρ_{eff} degrades at higher frequencies.

It is important to point out that the substrate's effective resistivity is directional using this enhancement scheme and that a co-design between the PN implants and the RF device should be performed simultaneously during layout. Indeed, the pattern of the PN implants serves to impede electrical field propagation in unwanted directions according to the needs of substrate loss or coupling mechanisms of the overlying devices. For example, different PN implant patterns should be used beneath CPW lines, inductors, antennas, RF switches, or between two areas to reduce crosstalk. As an example, and with reference to **Figure 8.2**, rotating the CPW line by 90° would lead to a very low ρ_{eff} and therefore to increased losses due to the facilitated conduction from the signal line to the ground lines through the P and N doped regions themselves. A pertinent example of PN line patterns to improve the quality factor of an integrated spiral inductor will be given in **Section 8.2.3**.

One idea to alleviate the co-design in terms of geometry of PN junctions together with the overlying devices is to pattern very small P and N regions in an array or checkerboard like manner. No hardware or simulation data is available[7], and more information on the concept can be found in **[170]**.

[6] Though this can be accounted for during design, it remains a little inconvenient, as in this case $\varepsilon_{r,eff}$ is expected to depend on CPW dimensions, in a similar manner as ρ_{eff} does, as explained in **Section 2.1.3** (see **Figure 2.6 pg. 42**). We shall see further on in **Section 8.2.3** that by significantly increasing the PN junction density these effects are alleviated.

[7] Requires a 3D process simulator.

RF Performance: Harmonic Distortion in CPW Lines

Large-signal measurements of the CPWs on the DP substrates were performed at 900 MHz and are compared to HR and TR results in **Figure 8.5**. The DP substrates achieve around 30 dB improvement in linearity over HR, with the **DP-A1**, **DP-B1** and **DP-C1** samples presenting a $H2$ level of respectfully -67 dBm, -73 dBm and -77 dBm at +15 dB of fundamental output power $H1$. A lower doped DP substrate shows slightly higher distortion, which might be attributable due to the wider depletion regions being more field sensitive. In any case, these samples highlight a trade-off between effective resistivity and linearity (ρ_{eff}(5 GHz) are 1.5 kΩcm, 300 Ωcm, and 120 Ωcm, respectively).

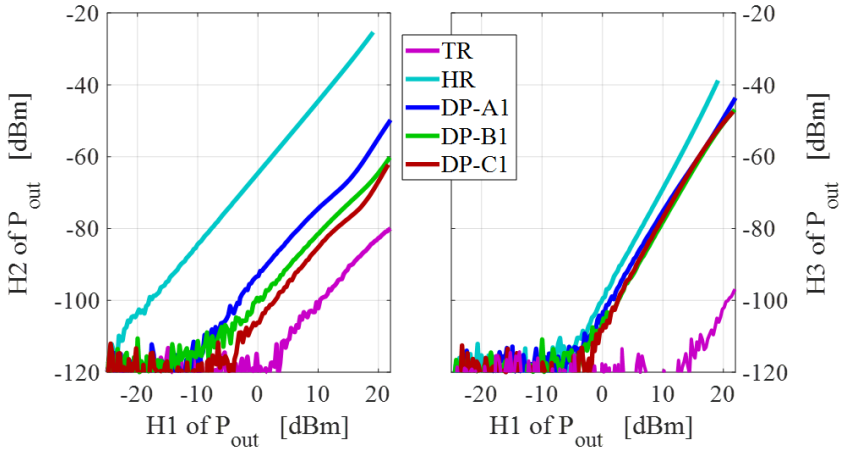


Figure 8.5: Harmonic distortion level power levels $H2$ and $H3$ vs fundamental power component $H1$ at the output of a 2.1 mm CPW line at 900 MHz, on HR, TR and DP substrates.

RF Performance: Substrate Coupling

Substrate coupling is evaluated thanks to the 2-port crosstalk structure, whose dimensions are given in **Figure 8.2** (it is the same crosstalk device as presented in **Figure 2.10 pg. 49**). The S_{21} coefficient from these measurements, plotted in **Figure 8.6**, evaluates the amount of coupling facilitated by the substrate between the two pads of the structure. The HR wafer shows high coupling due to the PSC effect, and a characteristic resistive plateau from 200 MHz to 8 GHz, while the TR sample presents a capacitive behavior over the measured frequency range with a 20 dB/decade slope. The DP samples show

strong improvement over the HR with over 25 dB increase in isolation at 1 GHz. While sample **DP-A1** places 25 PN junctions in between the two crosstalk pads, samples **DP-A2** and **DP-A3** only present 10 and 6 PN junctions, respectively, to impede the coupling between the two pads. For that reason, **DP-A1** shows the best improvement in substrate isolation, and **DP-A3** the worst, which remains however a significant improvement over the reference HR sample.

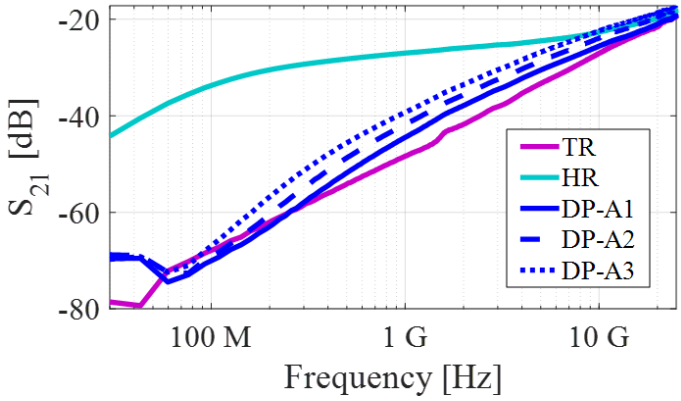


Figure 8.6: Coupling levels through the substrate between the two pads of the crosstalk on-wafer device on HR, TR and DP substrates.

Summary

In terms of RF FoMs, the UCLouvain prototype substrates achieve an effective resistivity in the range of a few kΩcm (up to 10 GHz) and a benchmark $H2$ linearity value of around -70 dBm (sample **DP-A1**) **[170–172]**.

These metrics, which already start to rival TR performance in the sub 6 GHz range, demonstrate well the concept of the DP technique.

Furthermore, industrial level lithography (in the tens of nm) will enable the fabrication of substrates with even higher RF performances still than these prototype samples (with µm-scale lithography from a university process) by packing a higher density of depleted junctions beneath devices, and this will be investigated through TCAD simulations in the next section.

The ρ_{eff} FoM of DP substrates is frequency-dependent, and though UCLouvain prototypes present ρ_{eff} below 1 kΩcm above 8 GHz, this frequency can be pushed up to mm-wave bands using a higher resolution lithography (up to 40 or 60 GHz, as discussed in the next section).

8.2.3 Simulation Study

In this section, TCAD simulations are employed in order to evaluate the substrate performance achievable using the DP substrate technique with access to higher resolution lithography[8]. PN patterns at the scale of a few hundred nm will be considered, as such resolutions are readily available in advanced FD-SOI design kits for back-gate implants while satisfying today's mask layout design rules.

Achievable Performance Using State-of-the-Art CMOS Lithography

At the time of writing (2020), the process design kits (PDK) of the 22 nm and 28 nm FD-SOI nodes support sub-200 nm wide P and N implant sizes as part of the back-gate process within their mask layout design rules [22, 23].

TCAD simulations are then run down to that size limit to evaluate the impact on the substrate RF FoMs. In this section, the P and N implanted regions do not overlap, and are characterized by equal doses (*Dose*) and by equal widths ($W = WP = WN$). Table 8.2 presents the results of a simulation study of the effective resistivity, extracted at 10 GHz, for several DP doping and sizing configurations.

From the results of the various configurations labelled from 1 to 7 in Table 8.2, the following observations can be made:

- **Dose Impact:**
  By comparing configurations 2 and 3 it is shown that higher doses produce lower values of ρ_{eff}, due to thinner depletion regions, as was discussed above in the case of the UCLouvain prototype substrates. However, higher implant doses are also more robust against high values of parasitic N_{ox}, as the substrate from configuration 2 fails to counter the PSC effect when N_{ox} is above 1 to $5 \cdot 10^{11}$ cm^{-2}, whereas the P-doped regions of configuration 3 are only inverted when N_{ox} is above 1 to $3 \cdot 10^{12}$ cm^{-2}. As a reminder, the highest N_{ox} observed in any measured sample in this work was $N_{ox} = 2.1 \cdot 10^{12}$ cm^{-2}, and doses of the order of 10^{13} cm^{-2} therefore offer a good compromise between sufficient robustness against parasitics and RF performance.

[8] As a reminder, the TCAD-based simulation approach of the RF FoMs, running an Athena process simulation followed by an electrical Atlas analysis, yielded accurate and predictive results for the UCLouvain prototype wafers that used µm-scale lithography PN patterns.

ρ_{eff}(10 GHz) [Ωcm]				N_{ox} [cm^{-2}]					
	Type	*Dose* [cm^{-2}]	*W* [µm]	$3\cdot10^{10}$	$5\cdot10^{10}$	$1\cdot10^{11}$	$5\cdot10^{11}$	$1\cdot10^{12}$	$3\cdot10^{12}$
1	/	/	/	300	140	70	20	13	6
2	PN	$1\cdot10^{12}$	1.5	850	960	1 000	280	50	10
3	PN	$1\cdot10^{13}$	1.5	780	770	740	710	680	19
4	PN	$1\cdot10^{13}$	0.2	5 800	5 400	4 700	4 200	3 800	30
5	P	$1\cdot10^{13}$	0.2	61	67	79	66	82	33
6	P	$1\cdot10^{13}$	0.5	160	190	280	640	980	65
7	P	$1\cdot10^{13}$	1.5	700	860	1 300	680	500	40

Table 8.2: Simulation study: effective resistivity (extracted at 10 GHz) pertaining to several DP doping and sizing configurations, for various densities of fixed interface charge N_{ox}. The silicon bulk in all considered configuration is 5 kΩcm P-type. All P and N implants are performed through a 20 nm thermal oxide and are respectively boron at 20 keV and phosphorous at 45 keV. A 180 nm SiO_2 deposition is then performed before defining the CPW line atop this material stack. Configuration **1** is the reference HR substrate without any PN implants. Configurations **5** to **7** use only P-type implants. Note: configuration **3** is quite close to the configuration implemented in the best UCLouvain prototype sample **DP-A1.**

- **Size Impact:**
  By comparing configurations **3** and **4** a clear benefit in ρ_{eff} is shown by increasing the junction density at the interface. A 200 nm lithography is readily available for below-BOX implants in FD-SOI fabs today (2020), and these simulations predict that by taking advantage of these capabilities 5 kΩcm values should be achievable at 10 GHz thanks to the DP concept. With an N_{ox} value of $1\cdot10^{11}$ cm^{-2} configurations **3** and **4** present an interfacial depletion density of 6.5% and 42%, respectively.
- **Are N-type implants necessary?**
  Configuration **7** is identical to **3** in which the N-type implants have been omitted, and it is shown in **Table 8.2** that the ρ_{eff} metrics are comparable. **7** does not require N-type implants as the positive N_{ox} induces electron-rich regions between the P-implanted zones, and so the overall carrier profiles in **7** and **3** are similar and yield similar ρ_{eff}.
  By comparing configuration **7** to **6**, which has a lower P sizing and separation W, a ρ_{eff} degradation is seen at low values of N_{ox}. This is due to the fact that a 500 nm separation between neighbouring P implanted

zones is insufficient to prevent fairly conductive electrical P-type contact between them due to free hole diffusion. For higher values of N_{ox}, in the range of $5 \cdot 10^{11}$ to $1 \cdot 10^{12}$ cm^{-2}, free electrons are in fact enforced in these regions, and a series of PN junctions is once again set up at the interface, raising ρ_{eff} to values close to 1 kΩcm (up until a very high N_{ox}, such as $1 \cdot 10^{12}$ cm^{-2}, creates an electron PSC even in the P-doped regions)[9].

Configuration **5** pushes this effect even further, using 200 nm P-type implants separated by 200 nm. In this case, the lateral diffusion between neighbouring P-type implants is not overcome for the considered N_{ox} values and no chain series of PN depletion regions is created in any of the simulations of configuration **5** (likely possible for some very narrow range of N_{ox}).

From these considerations, it appears that doses in the range of $1 \cdot 10^{13}$ cm^{-2} are the lowest values that retain robustness against parasitic N_{ox} as high as $1 \cdot 10^{13}$ cm^{-2}, and that using both P and N type implants along with pattern size of the order of a few hundred nm can produce very competitive RF substrate performance results at 10 GHz (around 5 kΩcm for configuration **4**).

In terms of non-linear performance, configuration **4** was evaluated using the large signal modelling approach presented in **Chapter 4**, using $N_{ox} = 5 \cdot 10^{11}$ cm^{-2}. This substrate achieves a $H2$ level of -79 dBm at +15 dBm of fundamental output power $H1$ at 900 MHz, which is within the range of RFeSI^{TM} substrate performance.

In terms of mm-wave performance, the simulations show that configuration **4** maintains a ρ_{eff} higher than 1 kΩcm up to 60 GHz for $N_{ox} = 0$ cm^{-2} and up to 40 GHz for $N_{ox} = 5 \cdot 10^{11}$ cm^{-2}. The $H2$ level simulated at a fundamental frequency of 25 GHz is -82 dBm at +15 dBm of fundamental output power $H1$, suggesting that trap-rich type substrates should outperform DP type substrates at mm-wave frequencies[10].

[9] A substrate passivation scheme relying on a certain value of parasitic oxide charge is of course of near-zero practical value.

[10] As we learnt from the discussions in **Section 5.8** (see **Figure 5.21 pg. 204**), an RFeSI80^{TM} substrate that presents a $H2$ FoM value of -80 dBm at 900 MHz sees that metric improve to around -100 dBm at 25 GHz, due to finite carrier inertia effects.

Integrated Spiral Inductors

The substrate improvement concept of buried depletion junctions interrupting the PSC layer in a HR substrate is applied via simulations to the design of high-quality RF inductors. Full-wave simulations are employed using Ansys HFSS software to compute the S-parameters of an integrated spiral inductor, illustrated in **Figure 8.8 (a)**, on several substrates: a TR, a HR, and two types of DP substrates, presenting respectively 5% and 35% of interfacial depletion density.

HFSS Substrate Definition and Calibration

The TR substrate is defined as having a homogeneous resistivity of 5 kΩcm below a 200 nm BOX.

In the HR substrate a 1.5 µm-deep layer with a resistivity of 1 Ωcm is introduced between the BOX and the high-resistivity bulk to model the PSC layer. This approach of modelling the PSC region as a single layer of silicon with a homogeneous resistivity is chosen in order to avoid ultra-fine meshing and unreasonable computation times in the three-dimensional full-wave solver.

For the enhanced DP substrates, additional 1.5 µm-deep shapes with 1 kΩcm resistivity are patterned inside a 1.5 µm-deep conductive 100 mΩcm layer for the modelling of the depletion junctions induced between adjacent P and N regions.

All of these discussed layers are depicted in **Figure 8.8 (b)**. The given depths and resistivities associated to the PSC and depletion regions are based on resistivity profiles obtained from the TCAD (Athena and Atlas) simulations, and are calibrated such that simulated CPW lines in HFSS fit to the measured data. These results are shown in **Figure 8.7**, where a good fitting between the HFSS data and the measurements is observed, demonstrating an efficient calibration of the substrates defined in HFSS[11].

[11] Though this material stack fits well to the measured CPW line data, it will not strictly fit to other layouts, as per the discussion on the impact of CPW dimensions on the extracted effective resistivity in **Section 2.1.3** (see **pg. 41**). From that discussion, we understand that the equivalent substrate stack presented here (in which the PSC interface is modelled by only a single 1.5 µm-deep layer of 1 Ωcm) will present some inaccuracies when considering other layouts than the CPW line from which this stack was determined. However, the characteristic dimensions of the other layouts considered in this section are close to that of the CPW used for substrate calibration (dimensions of the order of a few tens of microns), so any errors should remain quite small. Furthermore, the aim of this section is to evaluate roughly the achievable inductor quality factor on DP substrates, and not to provide very accurate predictive modelling.

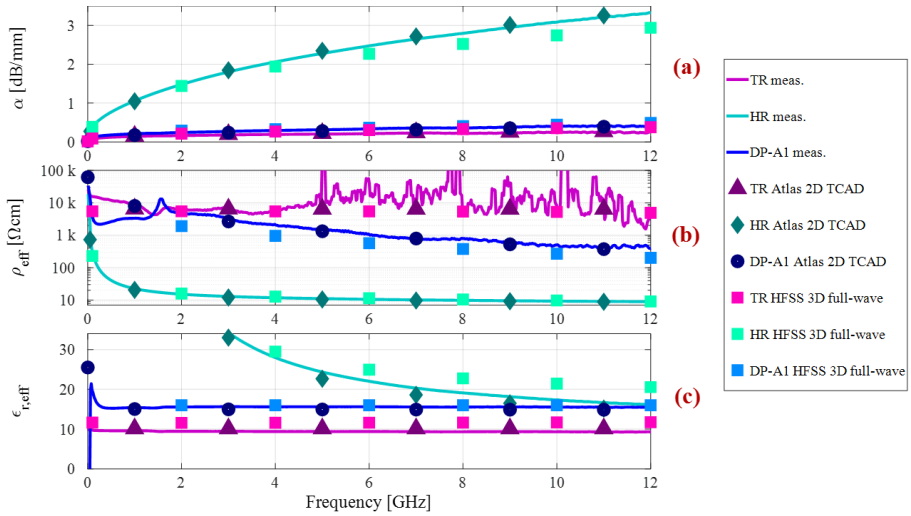


Figure 8.7: HFSS substrate calibration against CPW line measurements. **(a)** Effective resistivity. **(b)** Lineic line losses. **(c)** Effective relative permittivity. (Identical data as that presented in **Figure 8.4**, to which HFSS data points have been added in this figure).

RF Inductor EM Results

The calibrated substrates are then used to simulate other passive RF devices, such as an integrated spiral inductor. The designed inductor's layout is shown in **Figure 8.8**. It is a 3.5 turn spiral coil track that is 40 µm wide with a distance of 17 µm between each spiral and with an inner radius of 100 µm. The metal is 3 µm thick with a conductivity of $2.9 \cdot 10^7$ S/m, and is separated from the silicon by 200 nm of SiO_2 (as were the calibration CPW lines).

Figure 8.9 plots the inductance L and quality factor Q, calculated from the simulated two-port Y-parameters **[83]**.

On the TR substrate, the inductance boasts a peak Q-factor of 22 at 5 GHz for an inductance value of 35 nH, with a self-resonant frequency of 10.4 GHz.

When the device is transposed on the modelled HR substrate its quality at 5 GHz is poor, presenting a Q-factor of 1.4. The peak Q-factor drops to a value of 7.7 and its frequency point drops to 1 GHz. This reduction in Q is associated to the presence of the PSC layer that degrades the device's performance by

facilitating strong coupling between the parallel spirals of the inductance[12].

Therefore, by adding depletion junctions in a spiral pattern between the metallic spirals of the device, a drastic increase in substrate impedance between neighbouring spirals is achieved, which impacts positively on the overall Q-factor. This careful layout design is presented in **Figure 8.8**. The added depletion regions (shown in red) are placed in parallel spiral patterns between the metal spirals of the inductor (yellow). **Figure 8.8 (b)** highlights these depletion patterns (red) implemented beneath the BOX (blue) that interrupt the highly conductive P- and N-doped regions (green).

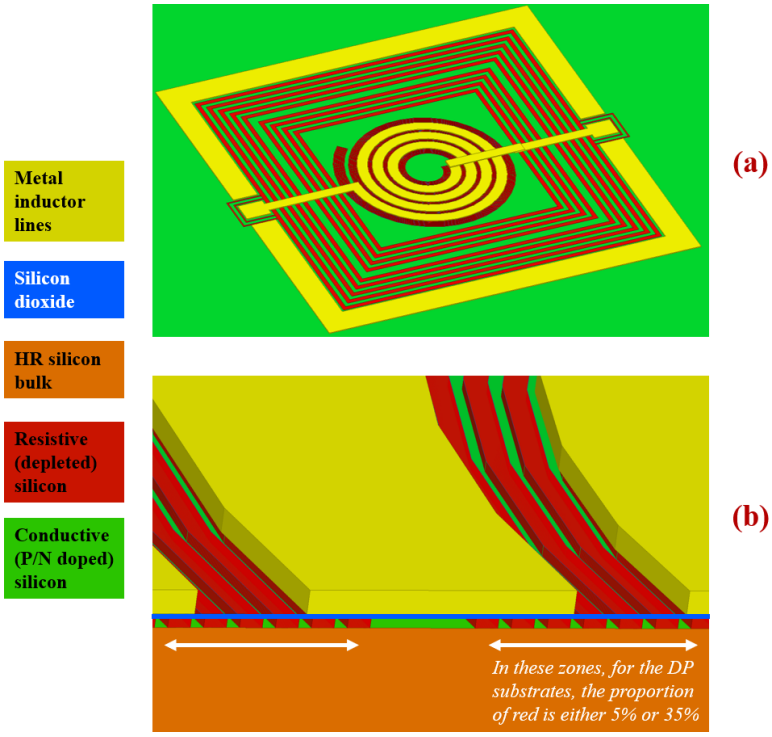


Figure 8.8: (a) Spiral inductor layout on depletion-enhanced substrate simulated using Ansys HFSS software. **(b)** Zoomed view of the highly resistive depletion regions (red) interrupting the conductive PSC layer (green) beneath the SiO_2 dielectric layer (blue).

[12] A simple lumped equivalent circuit model of an integrated inductor on TR and HR substrates is presented in [79], where insight is given on the PSC layer's influence on inductor Q-factor.

By adding a 5% density of depletion regions interrupting the conductive layer, the inductor's Q-factor is improved to a peak value of 17 at 2.2 GHz, and to a value of 7.2 at 5 GHz, as illustrated by the curve labelled as "DP (5%)" in **Figure 8.9**.

By increasing the depletion density to 35% (achievable in advanced CMOS foundries) the inductor quality is further improved, as shown by the curve labelled as "DP (35%)" of **Figure 8.9**.

For both considered DP substrate solutions, depletion junctions were also added to isolate the signal line of the spiral inductor from the RF-ground ring around it, using a set of concentric square patterns. Such patterns are also introduced around the signal port pads to isolate them from the ground lines as well, as can be seen from **Figure 8.8 (a)**.

For this optimized design, the Q-factor reaches a peak value of 22 at 4.3 GHz, and is at a value of 21 at 5 GHz, closely rivalling the performance on the TR substrate, and demonstrating the potential for this substrate-enhancement method for RF integrated passive inductors. We note a slight lowering of the inductor's self-resonant frequency on this DP substrate that is attributed to a slightly higher effective substrate permittivity sensed by the device, as discussed above (see **pg. 270**).

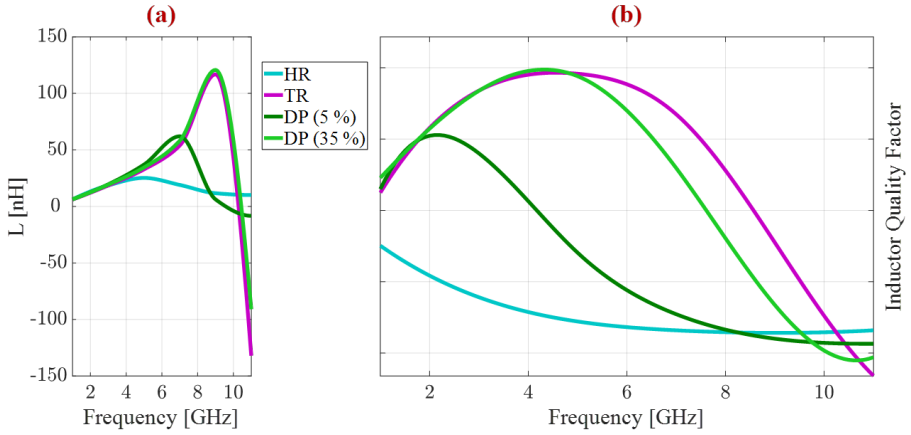


Figure 8.9: HFSS simulations of inductance **(a)** and quality factor **(b)** of integrated spiral inductors on HR, TR and depletion-enhanced (DP) substrates.

The work from this section concerning spiral inductors on DP substrates was published in **[171]**.

8.2.4 Summary

In this section, a novel surface passivation technique for HR samples was presented enabling high quality RF performance to be achieved in terms of substrate losses, passive quality factors, crosstalk interference levels, and linearity.

The concept was demonstrated thanks to RF FoM measurements of prototypes fabricated at UCLouvain.

The working principle is to tackle the parasitic surface conduction effect at the Si/SiO_2 interface by modifying interface impedance using P and N type doping patterns.

The PN passivation method is a local solution, and because of this it can find applications in bulk CMOS and in FD-SOI technologies as easily as in PD-SOI[13].

Simulation results predict competitive RF performance when taking full advantage of CMOS lithography. Indeed, by careful design of the PN depletion junctions it is shown that the RF performances can rival those of the widely used benchmark trap-rich solution[14].

[13] Solutions such as the deposition of a polysilicon layer over the entire wafer are incompatible with bulk technology. Furthermore, several challenges must be overcome to integrate trap-rich type solutions in UTBB FD-SOI technologies, such as the isolation quality of back-gate wells implemented in a defect-rich layer. At the time of writing (2020), the compatibility of a TR passivation solution within a UTBB platform has not yet been demonstrated.

[14] We also note that a DC bias can be applied to the P or N regions (relative to the substrate) in order to reverse bias the junctions and increase the depletion width, increasing the interface depletion density and thereby further improving RF performance **[170]**.

8.3 Field-Induced Depletion High-Resistivity Substrate

In this section, a surface passivation technique, that we shall name from here on as *Fiel-Effect* (FE) -passivation, is presented, that also addresses the PSC effect in HR wafers.

It is implemented by using patterns in a *lower-level layer* close to the Si/SiO_2 interface that are drawn below RF passives or interconnects (implemented in higher level metal layers of the BEOL). By applying DC voltages to these *lower-level* structures, the surface carrier density –and hence the interface impedance– can be controlled through the field-effect. In practice, these *lower-level layers* may be metallic layers of the BEOL, but may also be FEOL layers, such as polysilicon or even an SOI film. This concept was patented in **[217]** independently of the research of this thesis.

8.3.1 Concept

The approach is similar to that of DP substrates presented in the previous section, as the idea is to start from a high-resistivity silicon wafer and to passivate the oxide/silicon interface such that there is no longer a strong conduction channel (through a continuous PSC layer) that severely degrades the effective resistivity sensed by coplanar circuitry.

The concept is shown in **Figures 8.10, 8.11 and 8.12**, that illustrate how applying DC biases to the *lower-level* structures can enhance the substrate's effective resistivity in order to render an overlying RF passive (half of a CPW line depicted in these figures) less lossy (and more linear).

The silicon bulk is high-resistivity (5 kΩcm) P-type, and an interfacial charge density of $N_{ox} = 3 \cdot 10^{11}$ cm^{-2} is included at the Si/SiO_2 interface.

In those figures, TCAD simulation results of half of a CPW implemented in a top metal layer, named "Metal 2", are depicted, beneath which several lines in a lower material layer are defined. Metal 2 is 1 µm-thick aluminum and is set at a distance of 5 µm from the Si/SiO_2 interface. The lower material layer is defined as 50 Ωcm P-type polysilicon (without any traps) that is set 200 nm above the Si/SiO_2 interface. Then, under these conditions, the flatband voltage V_{fb} in this layer relative to the substrate interface is calculated as approximately -3 V (using **Equation 3.50 pg. 82**).

In **Figures 8.10 and 8.11** an *array-like* structure is considered for the FE-passivation shapes. One polysilicon line in two is depicted in a light gray color, and the DC bias voltage V_{fe1} is applied to all such light gray lines. The other lines, depicted in dark gray, have the DC bias voltage V_{fe2} applied to them.

V_{fe1} and V_{fe2} are applied (relative to the substrate) on each polysilicon shape through high impedance elements such that these lower-level shapes can be considered as RF-floating, and isolated from each other. Each polysilicon line is 500 nm wide, and the distance to the next adjacent lines is 1.5 µm.

Figure 8.10 (a) depicts the carrier concentration in the substrate when $V_{fe1} = V_{fe2} = 0$ V is applied. Then, the interface suffers from PSC, and the effective resistivity sensed by the CPW line is of the order of 190 Ωcm[15].

Figure 8.10 (b) depicts the case when $V_{fe1} < V_{fb}$ and $V_{fe2} > V_{fb}$. Under these conditions, a series of P and N type regions are then induced at the interface, and the depletion junctions in between them serve to increase interface impedance. This principle highly resembles that discussed for the DP-substrates from the previous section. The effective resistivity, taken at 10 GHz, is then improved to around 800 Ωcm, substantially reducing the substrate losses[16].

Figure 8.11 (a) depicts the carrier concentration when $V_{fe1} < V_{fb}$ and $V_{fe2} < V_{fb}$. In that case, holes are induced beneath all poly shapes and interrupt the interfacial electron-PSC[17]. The interface depletion junction density is doubled compared to the previous bias condition, and the substrate effective resistivity sensed by the CPW line is then simulated as 1.5 kΩcm at 10 GHz.

Figure 8.11 (b) depicts the carrier concentration when $V_{fe1} = V_{fe2} = V_{dep-opt}$, where $V_{dep-opt}$ is the optimal depletion voltage point that produces the highest interface impedance below all poly-shapes. The interface depletion density is then maximized (PSC still exists in between the poly-shapes), and the substrate effective resistivity sensed by the CPW line is approximately 3.8 kΩcm at 10 GHz.

[15] This value is significantly higher than the value of around 30 Ωcm that we have been used to seeing from HR samples with an N_{ox} of the order of $3 \cdot 10^{11}$ cm^{-2} in this thesis. The reason for the higher ρ_{eff} in this section is due to the large distance t_{ox} of 5 µm separating the CPW line from the Si/SiO_2 interface.

[16] The dimensions used for the polysilicon shapes (width 500 nm, separation 1.5 µm) yields one depletion junction at the interface every 2 µm. In terms of *depleted interface density* (as defined in the previous section dedicated to DP substrates) the FE substrates considered here achieve around 3%. If design rules allow, closer packed poly layers can increase this density. We note that the impact of poly to poly coupling on the ρ_{eff} may then limit the gain brought by closer packing (depends on poly resistivity and on all dimensions).

[17] No hole-type electrical connection occurs between two neighbouring regions below the poly-shapes due to the fairly wide poly to poly separation of 1.5 µm, which allows for the electron-PSC to be established in those regions independently of values of V_{fe1} and V_{fe2}. If the separation was smaller and/or the N_{ox} lower, a careful design would need to be performed in order to avoid conductive hole-type channel over the interface when applying this bias condition of $V_{fe1} < V_{fb}$ and $V_{fe2} < V_{fb}$.

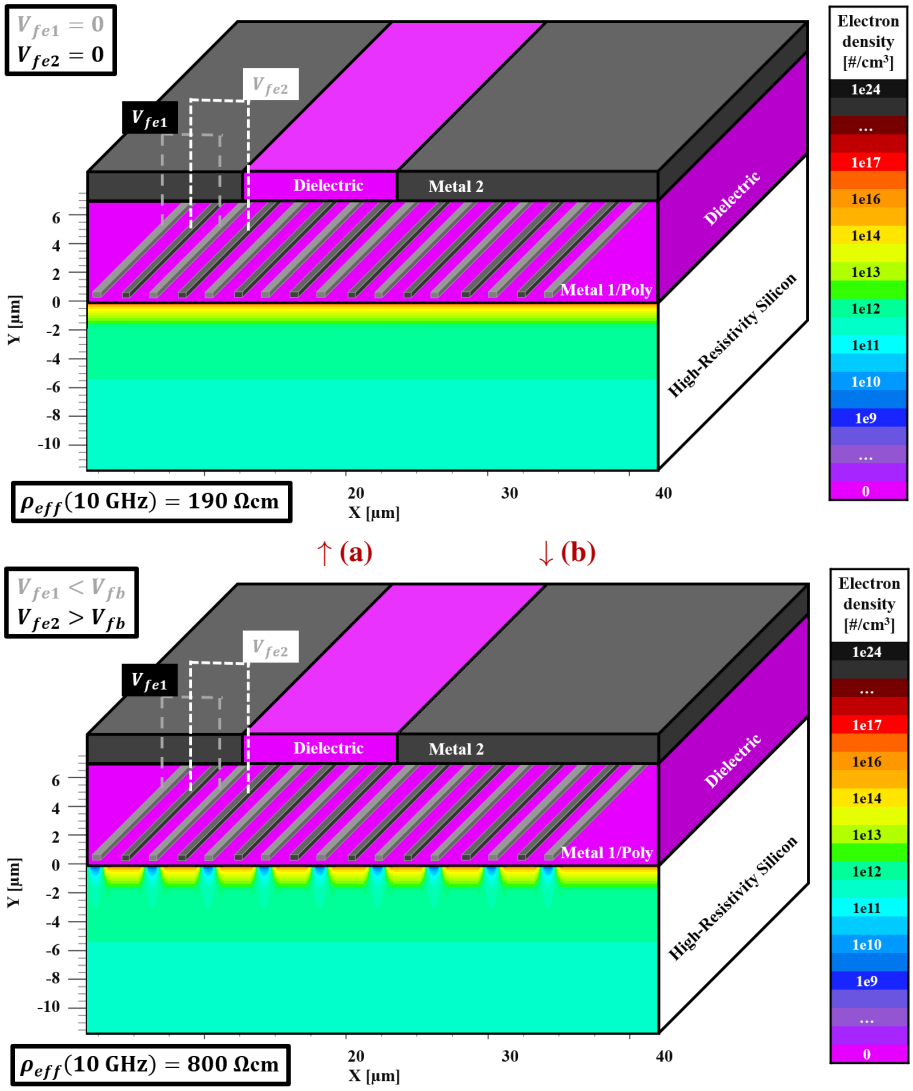


Figure 8.10: Carrier profile in a HR substrate (with PSC) in which the field-effect passivation scheme is implemented using lower-level layers to control the interface impedance, below a CPW line in "Metal 2" (5 µm above the Si/SiO_2 interface). **(a)** When $V_{fe1} = V_{fe2} = 0$ V, the ρ_{eff} sensed by the CPW is around 190 Ωcm at 10 GHz. **(b)** When $V_{fe1} < V_{fb}$ and $V_{fe2} > V_{fb}$, the $\rho_{eff}(10\ \text{GHz})$ is improved to around 800 Ωcm.

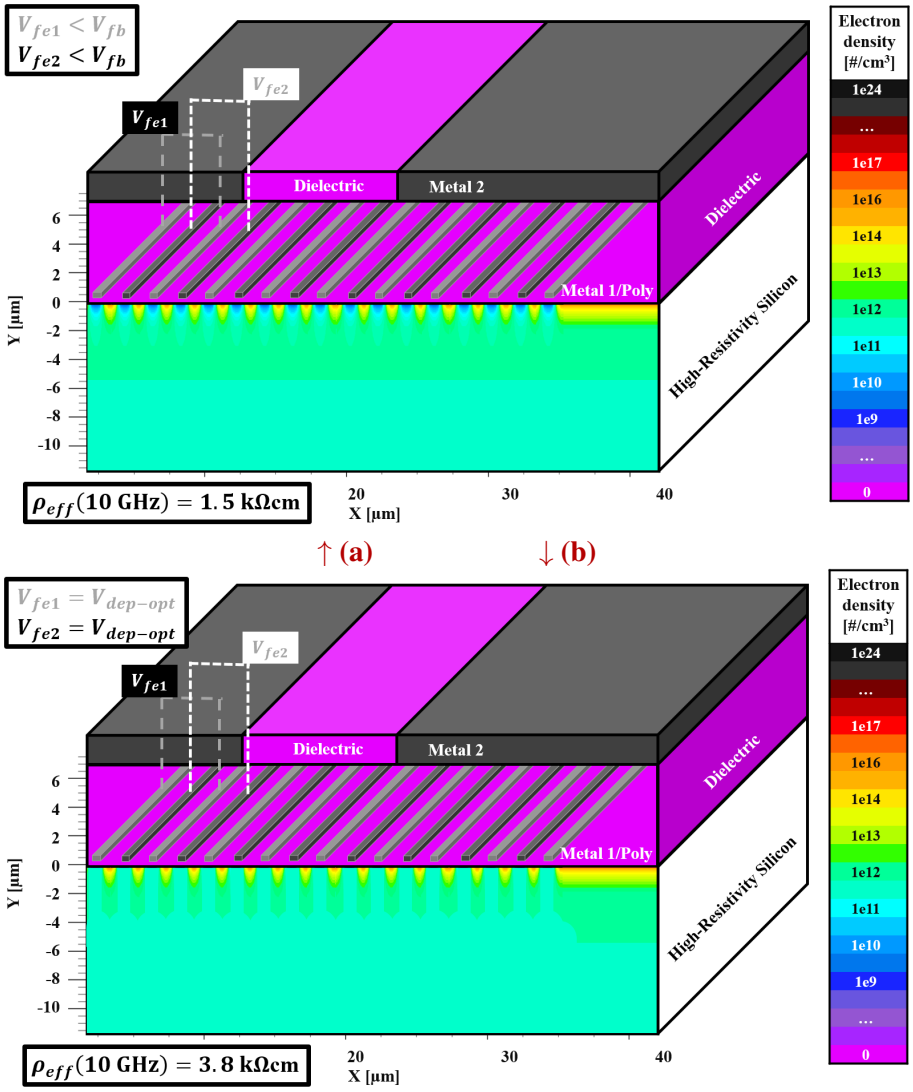


Figure 8.11: Carrier profile in a HR substrate (with PSC) in which the field-effect passivation scheme is implemented using lower-level layers to control the interface impedance, below a CPW line in "Metal 2" (5 µm above the Si/SiO_2 interface). **(a)** When $V_{fe1} < V_{fb}$ and $V_{fe2} < V_{fb}$, the ρ_{eff} sensed by the CPW is around 1.5 kΩcm at 10 GHz. **(b)** When $V_{fe1} = V_{dep-opt}$ and $V_{fe2} = V_{dep-opt}$, the ρ_{eff}(10 GHz) is improved to around 3.8 kΩcm.

Finally, we might consider a *continuous-plane* for the FE-shape implemented below the CPW line to which $V_{dep-opt}$ is applied. **Figure 8.12** illustrates this scheme, and plots the carrier concentration profile in the silicon. In that case, the surface is perfectly well passivated, and an effective resistivity of around 12 kΩcm is achieved at 10 GHz. In a high-quality trap-rich substrate with 5 µm of dielectric material between this CPW line and the Si interface, the ρ_{eff} would be of the order of 100 kΩcm. The reason for the lower value of 12 kΩcm observed here is due to the finite resistivity of the polysilicon lower-level layer, which then becomes the dominant contributor to the value of ρ_{eff}. For the simulated resistivity ($\rho_{poly} = 50$ Ωcm) and thickness ($t_{poly} = 100$ nm) of this layer, the ρ_{eff} is acceptably high. However, if we were to replace ρ_{poly} by the value of 1 Ωcm, simulations inform us that ρ_{eff} drops to 1.0 kΩcm[18].

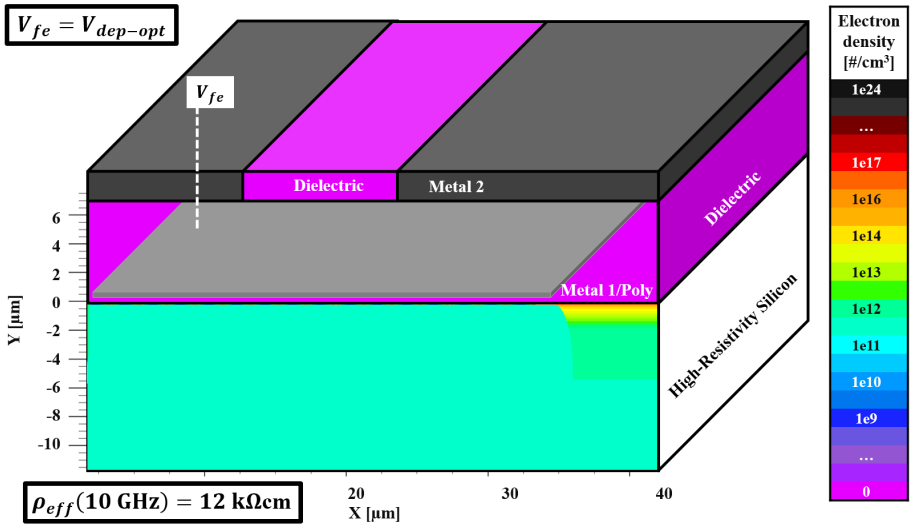


Figure 8.12: Carrier profile in a HR substrate (with PSC) in which the field-effect passivation scheme is implemented using a uniform lower-level layer to control the interface impedance, below a CPW line in "Metal 2" (5 µm above the Si/SiO_2 interface). **(a)** When $V_{fe} = V_{dep-opt}$ the ρ_{eff} sensed by the CPW is around 12 kΩcm at 10 GHz.

[18] The difference in doped-poly work functions was accounted for, and the bias applied in the two simulations are such that the surface potential at the Si/SiO_2 is precisely the same. Any substrate impedance differences (i.e. ρ_{eff}) are then attributed solely to differences in ρ_{poly}.

The extracted parameters from the small-signal TCAD-based simulations of the CPW lines considered on all the substrates discussed above are plotted over frequency in **Figure 8.13**. The performances discussed above focused on the 10 GHz data, and **Figure 8.13** highlights the frequency dependencies, that are particularly noteworthy for the 2nd, 3rd and 4th simulated curves, that pertain to *array-like* solutions that induce a series $R-C$ type network and the Si/SiO_2 interface.

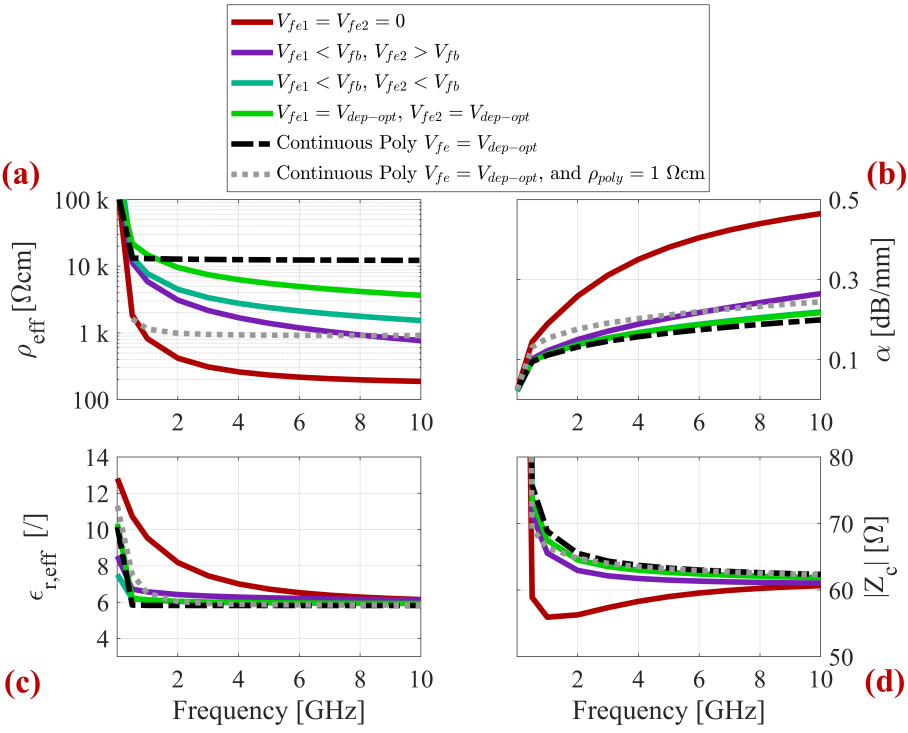


Figure 8.13: Effective parameters extracted from RF simulations of CPW-lines on various FE-passivated substrates. The reference CPW line (1 µm-thick aluminum, W_C =26 µm, S =12 µm) is implemented at a position of 5 µm above the Si/SiO_2 interface. A fixed charge density of $N_{ox} = 3 \cdot 10^{11}$ cm^{-2} is defined at this interface, and the silicon bulk material is 5 kΩcm P-type. The polysilicon passivation shapes are 10 nm-thick and 50 Ωcm P-type (except for the last simulation, where $\rho_{poly} = 1$ Ωcm). **(a)** Effective resistivity. **(b)** Lineic line losses. **(c)** Effective relative permittivity. **(d)** Characteristic line impedance.

8.3.2 Discussion

On the similarities between the FE passivation and DP passivation schemes:

- Strong similarities in the carrier distributions using these two passivation techniques are responsible for similarities in the RF FoM values and behavior.
- The RF FoMs depend heavily on the interfacial depletion density, and hence the achievable quality of the passivation is determined by process lithography limits.
- Both passivation schemes are local, and can find integration paths in PD-SOI, FD-SOI, and bulk CMOS technologies.
- The ρ_{eff} FoM is frequency-dependent in the *array-like* implementation due to the series $R-C$ nature of the surface impedance. In practice, sufficiently high interfacial depletion densities can be achieved by respecting the design rules of low-level materials available in advanced CMOS and SOI processes such that the effective resistivity can be maintained above a few kΩcm up to a few tens of GHz.
- For the *array-like* FE-passivation schemes (not *continuous-plane* type), a co-design is necessary between the RF device's layout and the FE-passivation shapes.

On applying $V_{dep-opt}$ in practice:

- The best results are achieved in terms of ρ_{eff} if an optimized depletion voltage $V_{dep-opt}$ can be applied.
  - An idea is to implement a voltage-regulation scheme in order to achieve a depletion condition, regardless of PVT variations.
  - However, the $V_{dep-opt}$ to be applied to attain high substrate FoMs may be within quite a narrow range, which may be impractical. This range depends on the distance from the FE layer to the Si/SiO_2 interface, but also, depends on the value of the parasitic N_{ox}. It would then be necessary for the IC designer wanting to implement such a $V_{dep-opt}$ biasing scheme to have an estimate value of N_{ox}. Depending on these parameters, it is to be understood that a $V_{dep-opt}$ value beyond a few volts may be impractical.
  - In the simulations pertaining to a *continuous-plane* depletion-inducing arrangement at 200 nm from the Si interface, simulations revealed that there is approximately a 200 mV bias range that allows for the CPW to sense a ρ_{eff} of at least 1 kΩcm.

- If the field-effect layer to be biased is closer to the interface, for example 20 nm, which could arise in practice using the active SOI film in a UTBB FD-SOI node, then the aforementioned 200 mV range will reduce to a mere 20 mV.
- If the layer is moved further away from the Si interface, the acceptable biasing range to achieve decent ρ_{eff} increases, but so too does the absolute value of $V_{dep-opt}$ (close to the flatband voltage).
- We note that $V_{dep-opt}$ may be multi-valued if the fixed oxide charge density is non-uniform over the Si/SiO_2 interface. Such consideration may be a source of a lack of robustness of exact $V_{dep-opt}$-based approaches.

Continuous-plane solution vs. array-like solution:

- While applying $V_{dep-opt}$ –necessary for the *continuous-plane* solution– may require an accurate control of the applied bias, this condition can be lifted if alternate *array-like* P and N type regions are defined at the interface through the field-effect (see **Figure 8.10 (b)** and **Figure 8.11 (a)**).
- The *continuous-plane* solution remains very attractive from a designer's point of view, as it alleviates the co-design between the passivation shapes and the RF device.
- It is possible to design a viable *array-like* solution implemented using metallic layers as the filed-effect arrangements with little effect on the CPW's line parameters, while, for the *continuous-plane* solution, a layer of significantly higher resistivity must be used (details in the next point below).

On the resistivity and thickness of the FE layer when implementing a continuous-plane solution:

- We have seen that decent results are achievable for a 100 nm tick layer of 50 Ωcm resistivity.
  - We point out that if the layer was only 10 nm tick, then similar RF FoM results would have been achieved using 5 Ωcm resistivity, as both implementations would contribute similarly to the line's absolute G parameter.
- Using a 100 nm tick layer of 1 Ωcm significantly deteriorated the RF results.
- Decreasing the resistivity further will continue to lower the ρ_{eff} parameter, until the slow-wave mode is brought about. Then, an RF equipotential

sets up in the layer, and there is no longer any V^2/R type loss within it. The field distributions are significantly changed, and the line becomes highly capacitive, and its characteristic impedance and propagation constant are highly modified. If the plane becomes close to being of metallic properties, inductive coupling (Eddy currents) to the plane will further impact on the line's characteristics (not an accountable-for effect using a semiconductor TCAD tool).

8.3.3 Summary

In this section, a novel surface passivation technique for HR samples was presented enabling high quality RF performance to be achieved.

The working principle of these so-called "FE" substrates is to tackle the parasitic surface conduction effect at the Si/SiO_2 interface by modifying interface impedance using bias voltages applied to low-level shapes by field-effect.

The concept was demonstrated thanks to TCAD simulations of the ρ_{eff} substrate FoM, and a discussion was included on the considerations to keep in mind when wanting to reproduce the proposed FE-passivation schemes in practice.

Recently (2021), this novel interface passivation scheme was demonstrated to be effective in GlobalFoundries' 45RFSOI process on HR wafers **[218]**. In that work, we demonstrate that an effective resistivity increase from a few hundred Ωcm to value of 2 kΩcm is achieved thanks to the appropriate biasing of field-effect passivation structures below top-level metal CPW lines, along with a linearity increase of more than 20 dB.

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8.4 Au Compensated Silicon

To provide bulk substrate passivation, doping silicon with gold (Au) atoms has been considered in [134–142] in order to implement high-resistivity substrates, notably for RF applications. It is commonly accepted that gold atoms in substitutional sites in crystalline silicon introduce two main deep-level trap states: a donor level at approximately $E_V + 0.34$ eV and an acceptor level at approximately $E_C - 0.54$ eV [136, 141, 143–146].

UCLouvain, in collaboration with the University of Southampton, has worked to characterize and model Au-compensated substrate samples [147, 148], and the main results are reviewed in this section.

8.4.1 Fabricated Au-Si Samples

Au-compensated silicon samples were fabricated at the University of Southampton, and metal deposition and patterning of the RF structures was performed in UCLouvain's cleanroom facilities.

The process starts from a standard N-type (phosphorous-doped) silicon wafer with a nominal resistivity of 56 Ωcm, which corresponds to a phosphorous donor density of $N_{Ph-D} = 9 \cdot 10^{13}$ cm^{-3}.

Gold atoms were then implanted at the backside of the wafer with a dose of $4 \cdot 10^{13}$ cm^{-2} at an energy of 100 keV.

The sample is subsequently annealed at 950°C in order to diffuse the Au atoms throughout the substrate in order to passivate the entire bulk volume.

An optimized combination of slow-cooling followed by a quenching step is applied to bring the samples back to room temperature, in order to maintain as many Au atoms in active substitutional sites (which contribute deep-level trap centers) rather than in interstitial sites (which do not) of the crystal lattice.

In depth details of all of these processing steps given in [141].

Then, 200 nm of SiO_2 is deposited atop the samples, followed by 1 µm of aluminum in which the RF devices are patterned.

The substrates used were 625 µm thick, and so if the Au atoms were to distribute evenly over this thickness, the volumetric density would be $N_{Au} = 4 \cdot 10^{13}/0.0625 = 6.4 \cdot 10^{14}$ cm^{-3}. It was shown in [135] from Secondary Ion Mass Spectrometry (SIMS) profiling along with SRP profiling that though more Au atoms end up at the front and back interfaces of the wafer, there remains more than $N_{Ph-D} = 9 \cdot 10^{13}$ cm^{-3} gold atoms deep within all parts of the bulk material, enabling sufficient doping compensation and conferring local resistivities higher than 5 kΩcm in every region of the sample.

8.4.2 Working principle

The working principle can be explained in an analogous manner to that of trap-rich substrates, that was detailed in **Chapter 3 Section 3.3 pg. 87** based on a charge compensation analysis. To avoid low-resistivity, charge-balance must avoid including large free carrier terms n and p, whose presence degrade RF FoMs. In the silicon bulk, any ionized thermal dopants (Phosphorous, Boron, etc.) should then be compensated for by ionized trap states such that the Fermi level E_F is deep in the band gap.

Figure 8.14 illustrates the charge balance at an arbitrary point in the Au-compensated and phosphorous-doped silicon material. Donor states are depicted in purple, while acceptors are shown in blue. A phosphorous level is plotted at energy $E_{Ph-D} = E_C - 0.045$ eV, and gold donor and acceptor levels are plotted at energies $E_{Au-D} = E_V + 0.34$ eV and $E_{Au-A} = E_C - 0.54$ eV, respectively.

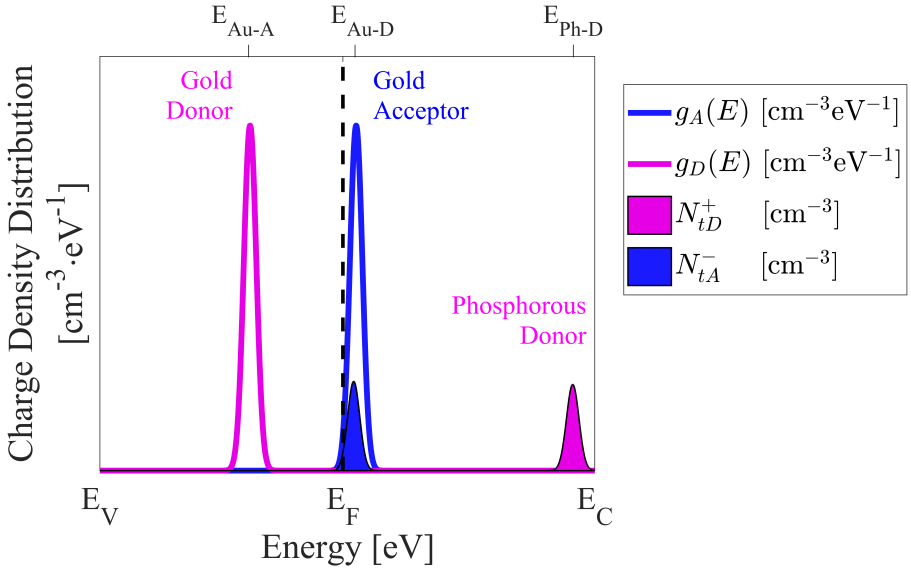


Figure 8.14: Representation of the Fermi level location and trap occupancy in Au-compensated silicon with background N-type phosphorous doping.

These states are depicted as thin distributions labelled as $g_A(E)$ and $g_D(E)$[19], and the integral of the product of each trap distribution by the occupation function over energy yields the total density of ionized gold/phosphorous atoms in the material, expressed in cm^{-3}, according to:

$$N_{tA}^{-} = \int_{E_V}^{E_C} g_A(E) \cdot F(E - E_F)\, dE \qquad [\mathrm{cm}^{-3}] \qquad (D.1)$$

$$N_{tD}^{+} = \int_{E_V}^{E_C} g_D(E) \cdot \big(1 - F(E - E_F)\big)\, dE \qquad [\mathrm{cm}^{-3}] \qquad (D.2)$$

$$g_A(E) = N_{Au} \cdot \delta(E - E_{Au-A}) \qquad [\mathrm{cm}^{-3}\mathrm{eV}^{-1}] \qquad (D.3)$$

$$g_D(E) = N_{Au} \cdot \delta(E - E_{Au-D}) \qquad [\mathrm{cm}^{-3}\mathrm{eV}^{-1}] \qquad (D.4)$$

$$F(\Delta E) = \big(1 + \exp\{\Delta E / kT\}\big)^{-1} \qquad [\,/\,] \qquad (D.5)$$

Where $\delta(x)$ is the Dirac delta distribution function.

In the example curves of **Figure 8.14** the gold states are in a density 5 times higher than the phosphorous state, which is a similar ratio to that in the fabricated samples, as described above with $N_{Au} = 6.4 \cdot 10^{14}$ cm^{-3} and $N_{Ph} = 9 \cdot 10^{13}$ cm^{-3}.

Assuming that free carriers contribute in negligible quantity to the charge balance (true if E_F is deep in the band gap), E_F can be solved for graphically from **Figure 8.14** as the position which yields the same total purple area N_{tD}^{+} and total blue area N_{tA}^{-} [20]. The first term corresponds solely to the ionized thermal phosphorous donors, as the gold donor levels are not ionized. The second term corresponds to the proportion of ionized acceptor gold states for the given E_F value. This Fermi level is very deep, close to mid gap in fact, conferring to the material very low free carrier densities and hence very high resistivity.

In general, when N-type compensation is required (i.e. when considering a sample with thermal donors close to E_C), the Fermi level in Au-Si samples will lodge close to $E_{Au-A} = E_C - 0.54$ eV. If $E_F = E_C - 0.54$ eV, the bulk resistivity will be of 45 kΩcm (slightly N-type).

[19] The representations of $g_A(E)$ and $g_D(E)$ with finite widths in **Figure 8.14** serve to facilitate the reader's understanding. In the TCAD simulator, these distributions are considered as Dirac delta functions, as described by **Equations D.3 and D.4**. In that case, **Equations D.1 and D.2** reduce to $N_{tD}^{+} = N_{Au} \cdot F(E_{Au-A} - E_F)$ and $N_{tD}^{+} = N_{Au} \cdot (1 - F(E_{Au-D} - E_F)$.

[20] Put into mathematical form, if the bulk is N-type with a thermal donor density of N_{D-th}, then the Fermi level will be at a position such that the following relationship is satisfied: $N_{Au-A} \cdot F(E_{Au-A} - E_F) = N_{D-th} \cdot \big(1 - F(E_{D-th} - E_F)\big) \approx N_{D-th}$.

And when P-type compensation is required (i.e. when considering a sample with thermal acceptors close to E_V), the inclusion of Au impurities will see the Femi-level lodge close to $E_V + 0.34$ eV. If $E_{Au-D} = E_F = E_V + 0.34$ eV, the bulk resistivity is around 700 Ωcm (P-type).

From this, we easily understand that the highest performance Au-compensated substrates should start life out as N-type.

The net ionized trap density depends on the Fermi level and hence on the applied E-field, which will contribute to the total charge to be compensated in the substrate, by either free carriers or trapped charge. The total ionized trap density is limited to a finite value due to a finite density of introduced Au. For the samples under consideration, this maximum charge compensation through ionized Au centers is limited to $N_{Au} = 6.4 \cdot 10^{14}$ cm^{-3} (assuming a uniform distribution of the implanted Au and that all Au atoms are in an active substitutional site). Though this value is sufficient to balance the background doping level while ensuring a highly resistive state, it is not high enough to pin the Fermi level close to E_{Au-A} (for an N-type compensated sample) for applied voltages of a few volts over an SiO_2 thickness of 200 nm[21]. Before looking at the RF results, we can then already state that we expect some substrate impedance modulation by the applied electrical signals (DC and RF).

[21] While this is the case in usual trap-rich substrates employing polysilicon, in which the total trap density is orders of magnitudes higher than the $6.4 \cdot 10^{14}$ cm^{-3} considered here for the Au-Si sample. See typical trap distribution parameters used in **Chapters 3 and 5**.

8.4.3 RF Performance Results

Both small- and large-signal measurement and simulation results pertaining to CPW lines fabricated on the Au-Si samples are plotted in **Figure 8.15**, where the interface Fermi level is plotted in **(a)**, and the effective resistivity and $H2$ level are plotted in **(b)** and **(c)**.

The simulated Au-Si substrate includes an interfacial oxide charge density of $N_{ox} = 10^{11}$ cm^{-2}.

The effective resistivity is always above 10 kΩcm for every applied DC bias. This is because the Fermi level is deep in the band gap at all interface regions other than directly beneath the CPW's central signal line. **Figure 8.15 (a)** shows that for zero applied DC field, the interface Fermi level is at $E_{F0_{AuSi}}$, which corresponds to a point close to $E_{Au-A} = E_C - 0.54$ eV, as expected. Hence, there is no PSC, as the gold density is sufficient to provide the surface passivation for the considered N_{ox} of 10^{11} cm^{-2} (while there is a PSC in the non-Au-compensated silicon sample, as it is shown that $E_{F0_{Si}}$ is close to E_C). At 0 Volts of DC bias, the entire interface, including directly below the CPW's central line, is in a state close to mid gap, i.e. highly resistive. The simulated ρ_{eff} at 0 V is then around 100 kΩcm, which is close to the maximum achievable value at 25°C of around 400 kΩcm[22]. The measurement point at 0 V is in the noise detection floor, because the extracted substrate G parameter is extremely low and close to zero. In practice, it is a challenge to extract ρ_{eff} values larger than 20 kΩcm, and is practically impossible to extract a ρ_{eff} above 100 kΩcm[23]. That data point is then set to 100 kΩcm as a default in this plot, and serves as a fairly rough indicator of the true $\rho_{eff}(V = 0)$ of the sample.

At other DC bias points, ρ_{eff} lowers appreciably due to the presence of inversion or accumulation regions below the signal electrode (see $E_F(V)$ curves in **Figure 8.15 (a)**), though remains high, above 10 kΩcm, (these values are in the measurement detection range) as these regions come in series with the near-intrinsic resistivity regions between the CPW's signal and ground lines. This measured $\rho_{eff}(V)$ behavior is in agreement with the simulated data.

[22] The maximization of $\rho_{Si} = (q\mu_n n + q\mu_p p)^{-1}$ at 25°C for optimal Fermi-level position yields $\rho_{Si-MAX}(T = 25) \approx 250$ kΩcm, considering usual carrier mobilities of silicon, i.e. not considering any additional scattering due to the Au implants (additional scattering due to Au centers is not included in the considered TCAD simulations either). Due to the 200 nm layer of SiO_2 (infinite resistivity), the maximum ρ_{eff} of the considered CPW line is then slightly increased, to $\rho_{eff-MAX}(T = 25) \approx 400$ kΩcm for such a MOS stack of material.

[23] At least using the CPW dimensions and measurement equipment considered in this work.

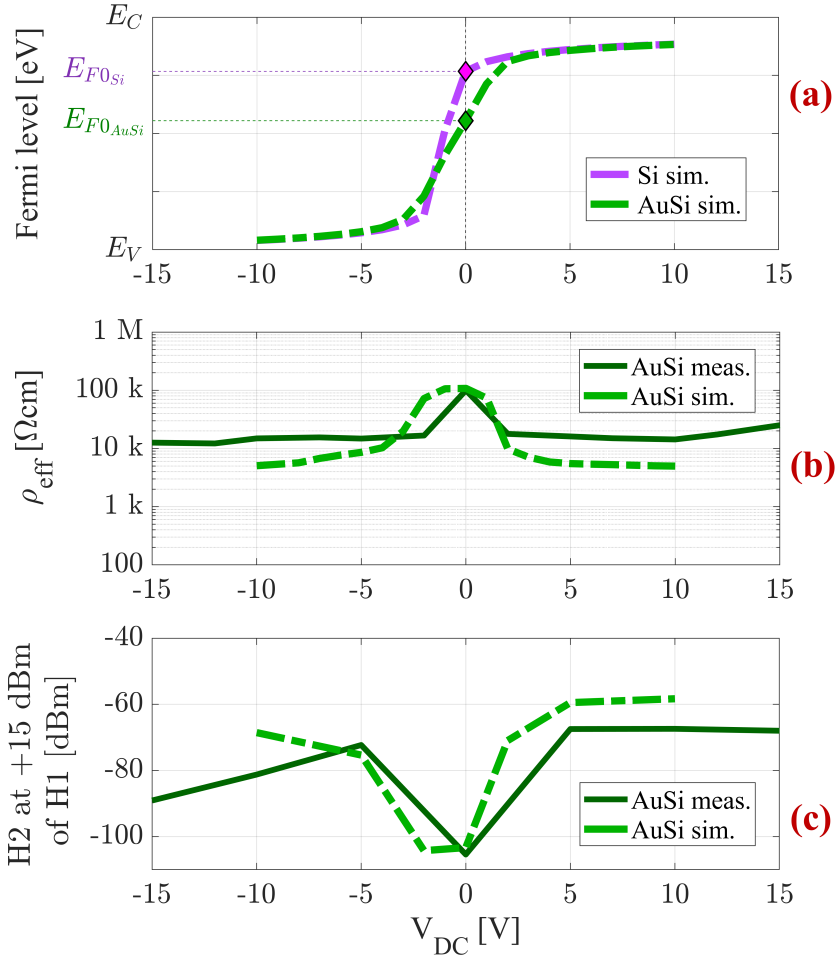


Figure 8.15: Simulated electrical parameters of a CPW line as a function of applied DC voltage V_{DC} implemented on an Au-compensated silicon substrate. **(a)** Position of the equilibrium Fermi level at 100 nm below the oxide layer. **(b)** Effective resistivity, extracted above slow-wave mode. **(c)** Second harmonic level for +15 dBm of output fundamental.

In terms of harmonic distortion levels, the large-signal model also correlates well to the hardware data. As extensively discussed in **Chapters 3 and 5**, the $H2$ level is strongly dependent on the number of *available free carriers* in the substrate that the RF signal can modulate. At a bias of 0 Volts extremely few

carriers are present in the semiconductor due to deep Fermi level positions at every location. The substrate is then very linear, with a $H2$ level below -100 dBm, which is of similar quality to the best in-class RFeSI^{TM} trap-rich substrate from Soitec, see **Section 5.9.1 pg. 206**.

However, when the DC bias induces inversion or accumulation layers below the central CPW electrode, the large-amplitude RF signal can then more strongly modulate the overall substrate impedance, as these *available free carriers* are alternately pushed away from and then pulled towards the silicon region below the signal line. The $H2$ remains quite low in absolute value, with the measured data remaining below -65 dBm over the considered bias range. This physical interpretation was verified by analyzing the free carrier distributions in the transient simulation results. The linearity variations of more than 30 dB in the $H2(V)$ curve are well captured by the large-signal simulations, further validating the robustness of the modelling approach.

From a theoretical standpoint, we note that by substantially increasing the Au impurity concentration, Fermi level pinning over several Volts of DC bias should be achievable. Then, though the bulk resistivity may slightly decrease as the Fermi level could move further away from mid gap **[135]**, the $\rho_{eff}(V)$ and $H2(V)$ should improve[24] and become flat over an extended bias range.

Measurements of other pertinent RF passive devices are presented in **[148]** on this same Au-Si sample. They include an integrated RF spiral inductor[25], a mm-wave coupled line band pass filter[26], and the reference 2-port crosstalk structure[27]. It is shown in **[148]** that the RF performance of those devices are identical in quality to the same devices implemented on a trap-rich substrate[25,26,27].

Finally, measurements performed over a 25°C to 200°C temperature range reveal that the Au-Si samples suffer similar degradations in the RF FoMs ρ_{eff} and $H2$ as trap-rich samples, and for the same reasons[28].

[24] Improvements should certainly be observed in the $H2$ levels at bias points other than 0 V. Depending on the exact location of $E_F(V=0)$, the $\rho_{eff}(V=0)$ may slightly increase or slightly decrease when increasing the active Au concentration.

[25] Identical device as presented in **Section 2.2.1** (**pg. 45**) on HR and TR substrates.

[26] Identical device as presented in **Section 2.2.2** (**pg. 47**) on HR and TR substrates.

[27] Identical device as presented in **Section 2.3** (**pg. 49**) on HR and TR substrates.

[28] Due to an increased intrinsic carrier density n_i in the bulk that reduces the resistivity and adds more *available free carriers* that raise $H2$. See **Section 5.6** (**pg. 190**).

8.5 Porous Silicon Substrates

In this section, we propose and discuss another type of silicon-based RF substrate solution: porous silicon (PSi). This material can be locally formed from a silicon wafer by electrochemical dissolution of bulk crystalline silicon [176], and an optimized porosification process can lead to a PSi substrate that fulfills the requirements for highly integrated RF SoCs, combining high resistivity and strong linearity. For these reasons, the potential of PSi for RF applications has not gone unnoticed [177–195], and in this work, we further research the RF performances of PSi substrates. Porous materials have lower dielectric constants than their bulk counterparts, which results in lower crosstalk levels and coupling parasitics[29].

At UCLouvain, the RF research group has developed high quality PSi for RF applications fabricated starting from standard resistivity (1-10 Ωcm) Si wafers [86, 196], in contrast to the most widespread flavor of PSi substrates that is fabricated starting from heavily doped (5-20 mΩcm) Si wafers [179–182, 184, 186, 188–194].

Developing a PSi fabrication process starting from standard Si wafers has several advantages. The first is an economical one, as mΩcm wafers typically cost several times the price. A second is the fact that mΩcm wafers present a higher source of impurity contamination to the process equipment and are undesirable in some fabs.

The porosification step renders the wafers significantly more fragile and generally less mechanically stable. It will then be a challenge to handle wafers that have been porosified prior to the CMOS process chain (PRE-PSi substrates) in fabs, as well as in the dicing and packaging industries with high yield rates. For these reasons, post-CMOS process porous silicon (POST-PSi) has been proposed for the first time by UCLouvain's research group [198–200].

In this work, Section 8.5.1 describes the different types of PRE-PSi and POST-PSi samples developed at UCLouvain, and details their fabrication processes.

Then, Section 8.5.2 presents the RF performance results of the PSi samples and benchmarks their RF FoMs against the most common types of RF substrates, such as HR and TR.

[29] We can note that porous dielectrics are already used in advanced BEOL processes to implement *low-k* materials around the lower metal layers to reduce parasitic capacitive coupling close to the active devices [219].

8.5.1 Fabricated PSi Samples

In this work, three different PSi samples are considered:

- **PRE-PSi-S:** starting from a standard P-type silicon (nominal 10 Ωcm) wafer and porosified at the top side, over the entire surface of the wafer, up to a depth of 50 µm. This porosification is performed *before* the patterning of the RF devices.
- **PRE-PSi-m:** starting from a highly doped P-type Si wafer, with a nominal resistivity in the milliohm-centimeter range (10 mΩcm), and porosified at the top side over the entire surface of the wafer, up to a depth of 50 µm, *before* the patterning of the RF devices.
- **POST-PSi-m:** starting from a highly doped P-type Si wafer (10 mΩcm), and porosified from the back side *after* the patterning of RF devices. This porosification is not performed over the entire wafer surface, but only takes place locally beneath the RF passive devices, in order to preserve the mechanical strength of the overall sample.

The details of their respective processes are described hereunder.

PRE-PSi-S

To obtain the **PRE-PSi-S** substrate **[86, 196]**, a 3-inch standard resistivity (10 Ωcm) silicon wafer is exposed to an electrolyte that is a 2:1 mixture of hydrofluoric acid (HF 49%) and ethanol. The anodization is then conducted at a current density of 10 mA/cm^2 for 100 minutes. This process yields the mesoporous PRE-PSi-S substrate, porosified over 50 µm and with an average porosity of 65% over this depth (evaluated by weight measurements) and with a pore size of less than 5 nm in diameter, as shown in **Figure 8.16 (a)** and **(b)**.

The substrate is then annealed in oxygen at 300°C for 2 hours in order to strengthen the microstructure, and then in nitrogen at 420°C for 2 hours in order to stabilize the structure.

On top, a 500 nm SiO_2 layer is deposited at 300°C by PECVD, followed by a 1 µm-thick layer of aluminum deposited by PVD for the definition of the RF passives by photolithography and wet etching.

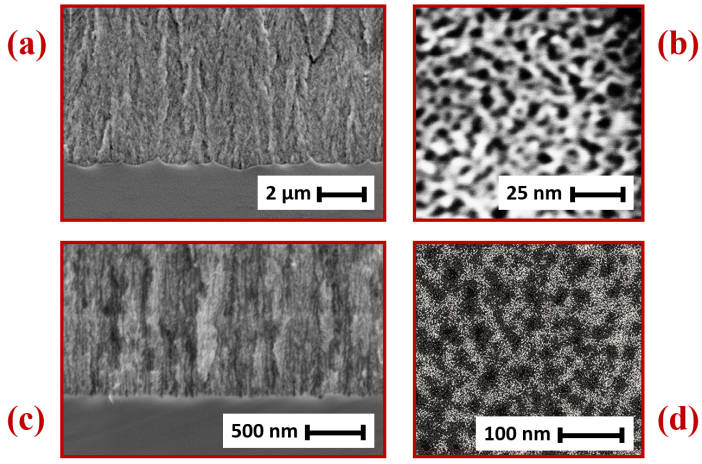


Figure 8.16: SEM images of the two PRE-PSi samples. **(a)** cross-section and **(b)** top-view (wafer front side) of the **PRE-PSi-S** sample. **(c)** cross-section and **(d)** top-view (wafer front side) of the **PRE-PSi-m** sample.

PRE-PSi-m

To obtain the **PRE-PSi-m** substrate **[86, 196]**, a 3-inch strongly-doped p-type silicon wafer (10 mΩcm) is exposed to an electrolyte that is a 1:1 mixture of hydrofluoric acid (HF 49%) and ethanol. The anodization is then conducted at a current density of 75 mA/cm^2 for 40 minutes. This process yields the mesoporous **PRE-PSi-m** substrate, porosified over 50 µm and with an average porosity of 50% over this depth (evaluated by weight measurements) and with a pore size of around 15 nm in diameter, as can be seen from **Figure 8.16 (c)** and **(d)**.

The **PRE-PSi-m** sample then undergoes the same strengthening and stabilizing anneals as the **PRE-PSi-S** substrate, along with a 500 nm deposition of SiO_2 followed by a 1 µm-thick aluminum layer from which the RF passives are then patterned.

POST-PSi-m

To fabricate the **POST-PSi-m** sample **[198–200]**, first, an *etch-stop* layer is deposited atop a strongly-doped p-type silicon wafer (10 mΩcm), followed by 500 nm of SiO_2, followed by 1 µm of aluminum, which is then patterned (photolithography and wet etching) to define the RF passive devices.

The thin *etch-stop layer* must be resistant to the HF-based electrolyte [197].

After protecting the frontside RF devices with a HF-resistant layer, porous silicon is then formed starting from the backside of the wafer to reach all the way to the frontside of the substrate. The PSi growth starts from openings made in a backside mask, that are aligned beneath the RF passive devices of interest. An over-etching ensures that the porous layer is present under the whole RF device (CPW line), as shown in **Figure 8.17 (a)**. Due to the isotropy of the porous silicon growth, the porous layer is largely extended laterally at the backside over a distance that is of the order of the substrate thickness.

The porosification is performed in an adapted electrochemical cell from the backside. Its particularity is to not involve the frontside of the wafer and therefore not to affect the RF circuits. PSi is prepared by anodization in a 3:1 volume solution of HF(49%):ethanol. The result is a mesoporous silicon with pore sizes in the rage of a few tens of nanometers, and a porosity close to 70%.

As the final step, the frontside protective layer is removed.

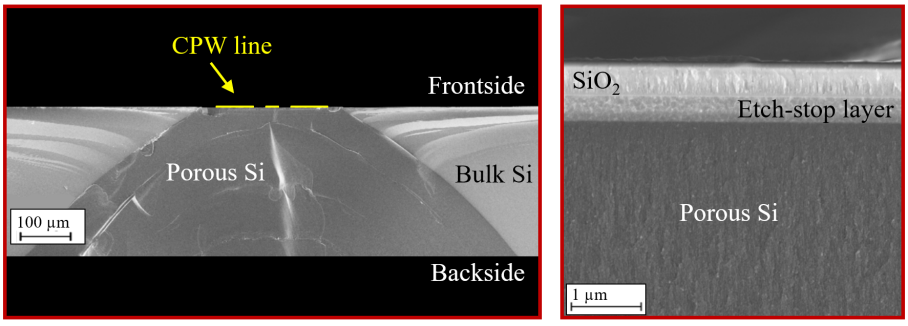


Figure 8.17: Cross-section (SEM images) of the **POST-PSi** substrate **(a)** over full substrate thickness, and **(b)** magnified view at the frontside of the wafer.

Figure 8.17 (b) is a magnified image performed at the frontside of the sample and shows the SiO_2 layer and the *etch-stop layer* above the porosified silicon. It confirms that the porosification reached all the way to the *etch-stop layer*, and that there is no longer any bulk silicon remaining beneath the RF devices.

8.5.2 RF Results

Both small- and large-signal measurement results pertaining to CPW lines fabricated on the three types of PSi substrates are plotted in **Figure 8.18**, and are compared to the measured RF FoMs of reference HR and TR samples.

All three PSi samples present an effective resistivity in the range of 5 to 10 kΩcm, demonstrating a deep position of the Fermi level not only at the interface, but also in the bulk[30].

The increase in resistivity through the porosification process is of approximately 3 orders of magnitude for the **PRE-PSi-S** sample and of approximately 6 orders of magnitude for the **PRE-PSi-m** and **POST-PSi-m** samples. Such drastic increases can be explained by a combination of reduced mobility and reduced free carrier density. By removing a large amount of the silicon bulk material during the porosification process, the effective mobility is decreased due to the reduced conduction paths available through the substrate and to scattering at the pore walls. Though such mechanisms surely have an appreciable impact on the overall value of ρ_{eff}, a mobility reduction of 3 to 6 orders of magnitude seems unreasonable. Then, the more likely hypothesis accounting for most of the increase in ρ_{eff} is that interface trapping states at the pore walls enforce a Fermi level deep in the band gap while providing bulk charge compensation for the background dopants, in an analogous fashion to the trapping effects presented for the case of Au-compensated Si (see **Section 8.4 pg. 292**).

PSi wafers present significantly lower effective relative permittivities than Std, HR or TR substrates. The **POST-PSi-m**, **PRE-PSi-S** and **PRE-PSi-m** substrates show effective relative permittivities of 3.5, 3.5 and 5.5, respectively, which correspond to a permittivity reduction of around 65%, 65% and 45%, respectively. These values correlate well with the measured (by weight) porosity of the PSi layers in the **PRE-PSi-S** and **PRE-PSi-m** samples, that were found to be of 65% and 50%, respectively[31].

Figure 8.18 (c) plots the large $H2$ power level at the output of an 8 mm-long CPW line, from from which 13 dBm has been subtracted, vs fundamental level $H1$ at 900 MHz, on the HR, TR and PSi substrates. The subtraction of 13 dBm should yield a decent estimation of the HD level that would occur at the output

[30] The lossy nature of the < 10 Ωcm starting wafers has been well counteracted by the bulk passivation.

[31] It is difficult to evaluate accurately the porosity of the **POST-PSi-m** sample by weight due to the localized nature of the process.

of the reference 2.1 mm-long line on the same substrates (see **Figure 5.18 pg. 200**). The 8 mm-long lines were measured because the PSi substrates are highly linear, and the induced $H2$ at the output of a 2.1 mm-long line is difficult to detect using UCLouvain's HD testbench due to its limited noise floor level. In fact, the **POST-PSi-m** sample's HD was too low for UCLouvain's testbench to detect, and it was then measured using *Incize*'s setup **[152]** with a significantly lower noise floor, as can be observed from **Figure 8.18 (c)**[32].

[32] That curve (black dashed line) is around 20 dB above the setup's detection floor, as demonstrated by the measurement of linear quartz substrates using that testbench in **[152]**.

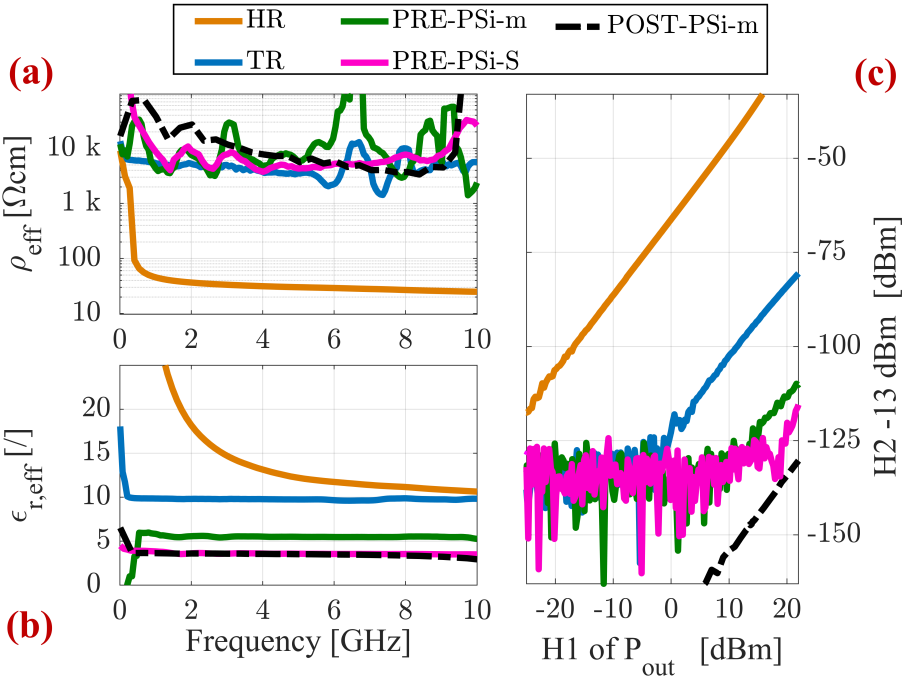


Figure 8.18: Effective electrical substrate parameters extracted from RF measurements of CPW-lines biased at 0 V DC ($W_C = 26$ µm, $S = 12$ µm). **(a)** Effective resistivity. **(b)** Effective relative permittivity. **(c)** Large-signal $H2$ level, from which 13 dBm has been subtracted, vs fundamental level $H1$ at the output of an 8.0 mm CPW line at 900 MHz, on HR, TR and PSi substrates. The subtraction of 13 dBm should yield a decent estimation of the HD level that would occur at the output of the reference 2.1 mm-long line on the same substrates (see **Figure 5.18 pg. 200**).

At +15 dBm of output fundamental power $H1$, the **PRE-PSi-m**, **PRE-PSi-S** and **POST-PSi-m** samples present $H2$ levels at -120 dBm, -130 dBm[33], and -145 dBm, respectively, making these samples the most linear silicon-based substrates presented in this thesis.

[33]Rough estimation from the measurements that are quite noisy at $H1 = +15$ dBm.

8.5.3 Summary

As an RF substrate solution, porous silicon can achieve high effective resistivity and record-high substrate linearity.

Furthermore, thanks to its low permittivity, substrate noise coupling levels and associated parasitics in PSi wafers are reduced compared to conventional Si substrate solutions over the entire frequency range.

Porous silicon is usually grown from fairly conductive (10 mΩcm) silicon wafers so as to facilitate the electrochemical processes, though growth from a standard resistivity wafer has been demonstrated with good RF results **[196]**.

While porous silicon's mechanical stability may lead to yield issues in the during various processing steps, a post-CMOS process approach has been proposed by UCLouvain and its RF performance has been demonstrated **[197–200]**.

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8.6 Recap of Silicon-Based RF Substrate Solutions

Table 8.3 recaps the advantages and disadvantages of all reviewed RF substrate solutions in this chapter, in terms of RF performance figures of merit and also in terms of ease of compatibility with integrated technologies.

As has been presented in the above sections, the RF figures of merit for a given substrate solution depend on many parameters (trap density, nominal doping, interface charge, available lithographic resolution, available implants, etc.). For this reason, the values given in **Table 8.3** are to be understood as *approximate values* associated to any considered family of RF substrates. They are listed with the main purpose of comparing these solutions to one another. Precise values and the discussions pertaining to them are given above in this work, in the specific sections dedicated to each substrate.

	RF Performance		Technology Compatibility			
	ρ_{eff} [Ωcm]	HD [dBm]	PD-SOI	UTBB	Bulk	MEMS
Std	10	-25	+ +	+ +	+ +	+ +
HR	50-200	-35	+ +	+ +	+ +	+ +
TR	3k-50k	-90	+ +	-	- -	+ +
Damage implants	$>$ 1k	<-60	+	+ +	+ +	+
DP	$>$ 1k	-70	+	+ +	+ +	+
FE	$>$ 1k	/	+ +	+ +	+ +	+
Porous	$>$ 30k	<-100	-	- -	-	-
Au-Si	$>$ 10k	-90	- -	- -	- -	+ +

Table 8.3: Recap and comparison of the all considered RF substrate solutions in this text in terms of RF figures of merit and of compatibility with various types of silicon-based RF technologies.

Std and HR wafers offer the poorest RF performances among the listed solutions. However, despite this, several RF-oriented technologies (notably sub-30 nm UTBB-FD-SOI nodes) implement these as substrates due to a combination of manufacturing/compatibility issues and/or pricing considerations.

The well-known TR solution boasts excellent results and has good compatibility with PD-SOI technologies, since the BOX/Si interface can be engineered over the whole wafer *prior to CMOS-processing* without having any effect on the above-BOX layers dedicated to the implementation of active SOI devices. Due to these considerations, compatibility with bulk and UTBB nodes is challenging.

Three other interface passivation schemes are envisaged to overcome these limitations by offering localized interface passivation solutions performed *during CMOS-processing* (i.e. can avoid the active device regions). These are the DP, FE and damage-implant (usually by Argon) substrate solutions. Though their RF metrics lag slightly behind those of TR substrates, they remain competitive and provide easier integration paths with certain technologies.

The bulk passivation schemes of porous silicon and Au-compensated silicon both demonstrate excellent RF performances, closely rivalling or even surpassing those offered by TR. They do however require process steps of higher complexity to implement, at least relative to the other mentioned substrate solutions, and their implementation in practice is more of a challenge.

Below are listed a series of additional comments pertaining to the information and metrics of **Table 8.3**:

HD: Values pertaining to the $H2$ power component at the output of the reference CPW line (L=2.1 mm, W_C=26 µm, S=12 µm) measured/simulated at 900 MHz of large-signal fundamental excitation at +15 dBm of $H1$ at output (and at 25°C). Due to bias dependencies on some substrates, the values given here are rough for comparison's sake. Precise data was given in the above sections for each type of substrate.

ρ_{eff}: Taken above the substrate slow-wave mode (and at 25°C). Due to bias dependencies rough representative values are given for comparison's sake. Some substrates present frequency-dependencies (**DP**, **FE**), once again, the values given here are rough. Precise data was given in the above sections for each type of substrate.

UTBB & PD-SOI: **UTBB** refers to FD-SOI technologies with thin BOX layers, while **PD-SOI** refers to technologies of thicker BOX. Solutions based on implants (**DP** and **Damage implants**) are more easily implemented through thinner layers.

Damage implants: Refers to high-resistivity substrates that have had their interface (with the dielectric material) passivated through amorphization by high-energy implants (typically Argon). The values pertaining to these substrates are taken from the literature as well as from measured samples that were not presented in this work.

MEMS: Refers to technologies of Micro-Electro-Mechanical Systems. For RF applications, electrically controlled mechanical switches exhibit very high-performance metrics. Typically, active devices (such as CMOS) are not part of a MEMS technology process. MEMS processes often run on silicon-based wafers, and substrate solutions are also then required for RF MEMS platforms.

Au-Si: Au is an undesirable element in the processing fabs of CMOS devices to avoid equipment contamination, since Au has high diffusivity and is a deep-level trap in Si capable of significantly affecting device behavior through its presence. For these reasons, easier compatibility is foreseen with **MEMS** platforms.

Porous: Porosification renders the wafers significantly more fragile and less mechanically stable. It is then foreseen as a challenge to handle wafers that have been porosified prior to the CMOS process chain (PRE-PSi substrates) in fabs, as well as in the dicing and packaging industries with high yield rates (though perhaps the possibility will emerge despite these difficulties). For these reasons, post-CMOS process porous silicon (POST-PSi) appears as a strong contender to integrated porous silicon into a full IC fabrication flow. POST-PSi still remains a challenge, justifying a significantly more complex compatibility metric assigned to porous in the above table than for other substrate solutions. For **UTBB** nodes the integration is harder still to foresee, since an etch-stop layer must be created that remains compatible with back-gate functionalities at the below-BOX interface.

8.7 Other Noteworthy Substrate Considerations

8.7.1 Vertical Parasitic Surface Conduction in 3DICs

In the context of 3D integration, which involves the stacking of two IC chips with high interconnect density between them, vertical vias are employed that pass completely through the chip's thickness, i.e. through its silicon substrate. These *through-silicon vias* (TSVs) are used as an alternative to wire-bond and flip chip techniques to enable 3D integrated circuits. Thanks to TSVs, inter-chip connection density can be extremely high, using connection lengths which are very short (the substrate thickness).

An example of a TSV structure is given in **Figure 8.19**. It consists of a vertical cylindrical metal interconnect that is insulated from the silicon substrate by a dielectric, usually SiO_2. A TSV is then a MIS structure, and, like every MIS structure considered in this thesis, it is subjected to an impedance to ground nodes and other circuit nodes via the substrate, and such impedances can be dominated by semiconductor effects that occur at Si/SiO_2 interfaces.

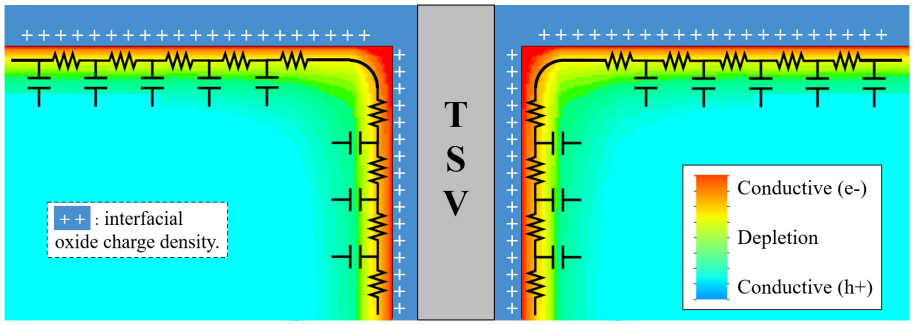


Figure 8.19: Cross sectional view of a TSV in a p-type substrate with PSC at all Si/SiO_2 interfaces, induced by fixed oxide charges. The carrier concentrations are illustrated, and the impedance network in the silicon is overlaid.

The TSV structure presented in **Figure 8.19** is implemented in a standard resistivity P-type substrate (10 Ωcm), and fixed positive oxide charge has been included in the TCAD simulation at all Si/SiO_2 interfaces, not only at the top side of the chip, but also along the TSV's insulator walls.

A vertical PSC then exists along these interfaces, and this PSC can be in electrical contact through a conductive path to a front side PSC, and/or even to

a back side PSC[34]. The conduction layer along the TSV walls can be modulated by the applied DC bias on the TSV relative to the substrate.

Such effect have been proved to explain the behavior of seemingly anomalous measured CV data between a fabricated TSV and the handle substrate **[220–224]**. In those works, a combination of vertical PSC effects and back side PSC effects was determined to be responsible for dominating the TSV to substrate impedance in certain bias and frequency conditions.

The intent of this section is not to go in depth into any TSV and substrate modelling, but to illustrate to the reader how PSC effects, that have been profusely discussed in this thesis, can have significant impact in 3D ICs (while purely planar technology and passives have been consider thus far in this work). The reader will realize that, in the context of RF signaling through TSVs, substrate and PSC considerations will impact on RF loss, coupling and on non-linear substrate-induced signal distortion. For linear TSV modelling of such effect, the interested reader is invited to consult **[222, 223, 225]**.

[34]Since in 3D ICs the back side of the wafer is passivated with a dielectric in order to implement interconnect bumps and/or a metallic *redistribution layer* (RDL).

8.8 Chapter Summary

In this chapter, several RF substrate solutions with high effective resistivities and low non-linear distortion levels were presented.

These were broadly categorized into two types: (i) interface passivation of HR-Si, and (ii) bulk passivation of Si.

A brief review of interface passivation schemes based on various ways to implement traps at the oxide interface with a HR bulk was performed.

Then, two novel **interface passivation** schemes, developed in this thesis, were presented.

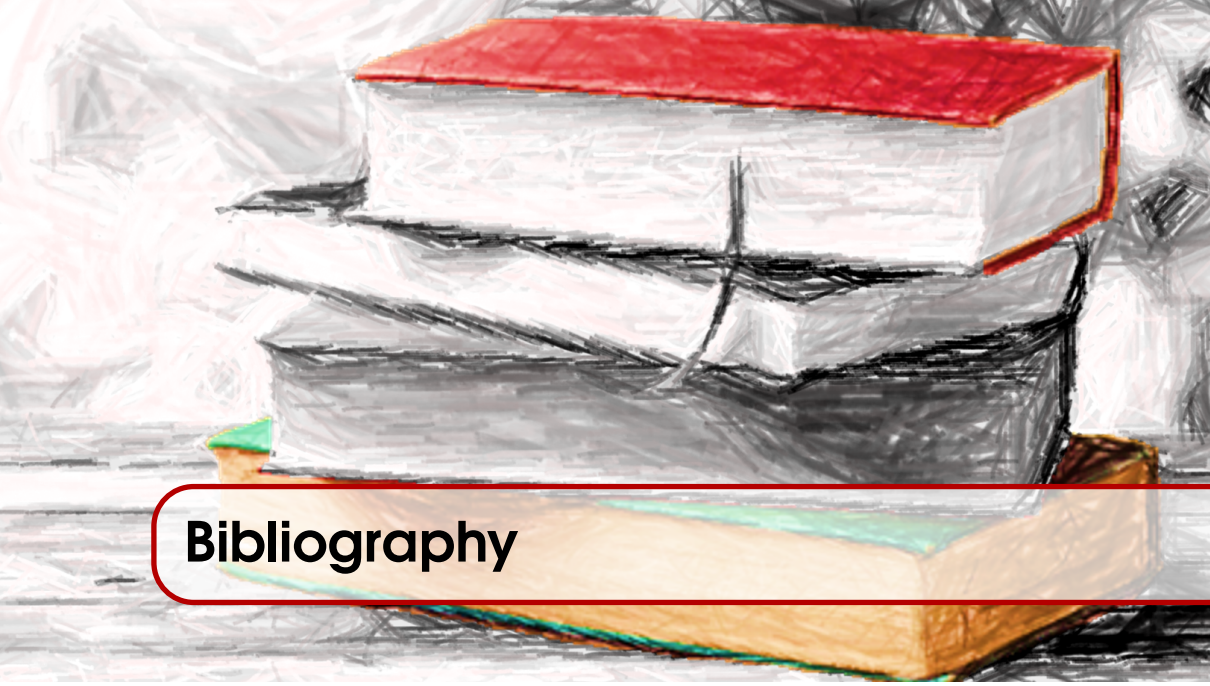
The first, based on P and N implants at the surface, saw its concept demonstrated through the measurements of fabricated prototype samples. By making use of advanced lithography capabilities (resolutions available in foundries today), simulations predict that the PN interface passivation can serve to implement competitive substrate solutions.

The second is based on the field-effect to passivate the interface, by using a biasing scheme applied to lower level patterned shapes to control the surface potential in the semiconductor substrate. Simulation results predict that good RF passivation is achievable, and an extensive discussion is given on the practical considerations to be aware of.

Next, two **bulk passivation** solutions were discussed.

The first is based on the introduction of Gold atoms in the silicon bulk that create deep-level trap states. These traps offer a charge compensation mechanism at each point in the silicon, which ensure a deep-Fermi level position while balancing fixed interface charges and/or ionized thermal dopants. Low free carrier densities, and hence high resistivity, are then achieved. Static simulations confirm the working principle based on physical interpretations and analysis, and then dynamic large signal simulations along with measured sample data demonstrate the RF substrate's excellent FoMs. The well-documented Au centers in silicon enable a fairly accurate modelling of the trap energy distributions, and we are able to demonstrate under that knowledge excellent correlations of the large-signal model developed in this thesis to the measured data.

The second bulk passivation solution, based on porous silicon, not only offers high effective resistivity and linearity metrics, thanks to a high density of traps introduced along the pore walls, but also offers reduced effective substrate permittivity, enabling lower substrate capacitive coupling for reduced crosstalk and higher quality factor passives (such as spiral inductors). Several samples were developed at UCLouvain and the RF characterizations were presented in this work. In terms of RF FoMs, the porous substrates are of extremely high quality, with the considered samples showing 20 dB to 45 dB lower distortion levels than the ultra-high linearity state-of-the-art RFeSI100^{TM} SOI trap-rich (300 mm). Furthermore, a post-CMOS localized porosification scheme was developed at UCLouvain in order to propose a viable integration scheme for the industry.



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