Identification of RF harmonic distortion on Si substrates and its reduction using a trap-rich layer

Daniel C. Kerr, Joseph M. Gering, Thomas G. McKay[1], Michael S. Carroll, César Roda Neve[2] and Jean-Pierre Raskin[2]

RF Micro Devices, Greensboro, NC
Tel: (336) 678-8857, Fax: (336) 678-0531, email: dkerr@rfmd.com
[1]RF Micro Devices, Scotts Valley, CA
[2]Microwave Laboratory, Université catholique de Louvain, Louvain-la-Neuve, Belgium

***Abstract* — Harmonic distortion (HD) is measured from coplanar waveguide (CPW) structures on various substrates at 900 MHz, and significant distortion for silicon substrates is demonstrated for the first time. For an input power of +35 dBm, 2nd and 3rd harmonic levels of -47 and -57 dBm, respectively, are measured for a thru calibration structure on oxidized high-resistivity silicon (HRS) substrates, and as high as -23 and -20 dBm, respectively, for longer lines and thinner oxides. These levels are high compared to a full cellular transmit switch product spec of -45 and -40 dBm for 2nd and 3rd harmonics, respectively, at similar power levels. The contribution of the silicon substrate to high harmonic levels is investigated experimentally, and an efficient technological solution based on the introduction of a trap-rich layer is demonstrated.**

***Index Terms* — Harmonics, High Resistivity Si substrate, Non-linear measurements, RF switches, SOI technology.**

I. Introduction

High Resistivity Silicon (HRS) substrates are promising for RF applications due to reduced substrate loss and coupling, which enables RF cellular transmit switches for SOI using HRS handle wafers [1, 2]. RF switches have high linearity requirements: for instance, current III-V RF switch products specify less than -45 and -40 dBm for 2nd and 3rd harmonic power (H2 and H3), respectively, at +35 dBm input power. As these requirements become even more stringent for advanced multimode phones and 3G standards, it is important to investigate even small contributions to Harmonic Distortion (HD).

II. Harmonic distortion from silicon substrates

Figure 1 gives the block diagram of the setup used to measure on-wafer HD under a 50 Ω power sweep at 900 MHz. The dynamic range at +36 dBm input power is over 110 dB. The vector network analyzer (VNA) provides the signal source and high dynamic-range receivers. A Power Amplifier boosts the drive signal to provide +5 to +36 dBm at the input to the device-under-test (DUT). Filtering and attenuators minimize the system harmonics and component interactions. The system is calibrated with the power meter using the VNA's internal calibration routines to provide an accurate drive signal level and to measure the power at the 2nd and 3rd harmonics.

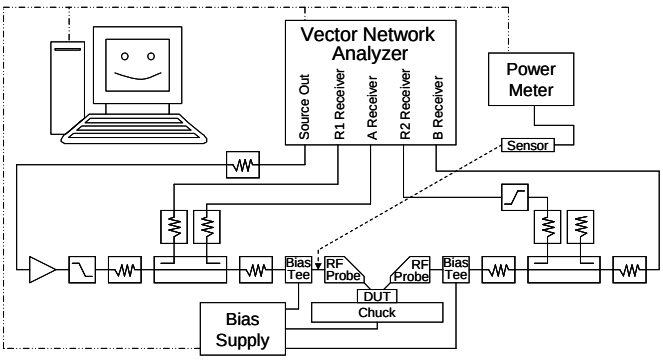

Fig. 1. Block diagram of the on-wafer, 50-Ω power sweep setup used to measure harmonics at 900 MHz.

The structure used for all measurements is a 50-Ω CPW line. In all cases, the metallic CPW line is lying on a thin dielectric on top of the substrate, as shown in Fig. 2(a).

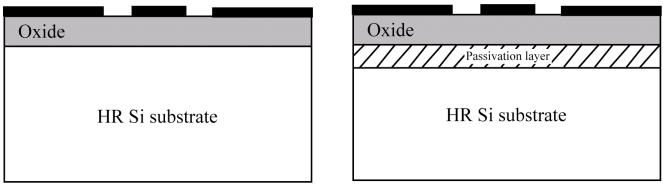

Fig. 2. Cross-section of a typical CPW line on oxide on a HRS substrate (left) and on passivated HRS substrate (right). Typical dimensions: 40 µm conductor width, 24 µm gap, and 208 µm ground width.

Experiments were run using variations in the metal type (Al, Cu, Au) and thickness, and dielectric type (thermal

oxide, CVD oxide, nitride) and thickness, as well as substrate (silicon, quartz, ceramic, and silicon with trap-rich layer).

Fig. 3 shows measurements for Au metal lines over 500 Ω-cm n-type silicon and quartz substrates. The measured H2 and H3 are -47 and -55 dBm, respectively. For the first time, significant harmonic distortion is found at input power levels greater than 10 dBm. The measurements from the quartz substrate indicate the noise floor of the measurement system, which is also obtained using the ceramic calibration substrate.

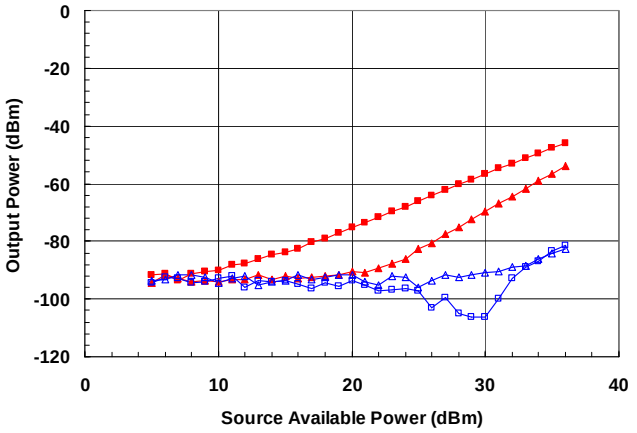

Fig. 3. Measured H2 (squares) and H3 (triangles) from a thru line on oxidized 500 Ω-cm n-type silicon (full symbols) and quartz substrates (open symbols). Line length is 0.7 mm.

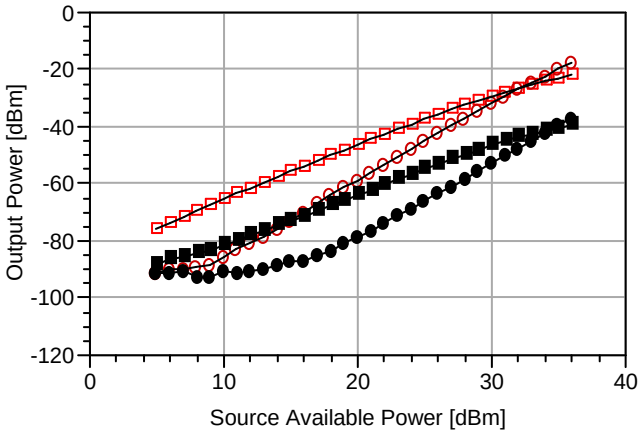

Fig. 4. Measured H2 (squares) and H3 (circles) from a thru (0.6 mm, full symbols) line and a longer line (2.1 mm, open symbols) on 60 nm-thick oxide on HRS substrate.

Fig. 4 shows the effect of the line length on HD for CPW lines lying on an oxidized 1 kΩ-cm p-type silicon substrate. The dielectric is only 60 nm-thick, which results in high electric fields at the silicon interface. Very high levels of HD are seen for the 2.1 mm-long line, at -23 and -20 dBm for H2 and H3, respectively.

To eliminate the possibility that the metal or dielectrics are the cause, Fig. 5 compares HD from a CPW line over HR SOI with and without a metal shield. The metal shield is connected to the CPW ground, and reduces HD to the noise floor. Although effective in some situations, it results in a relatively high capacitance to ground, degraded inductors, and has no benefit for devices in the SOI device layer.

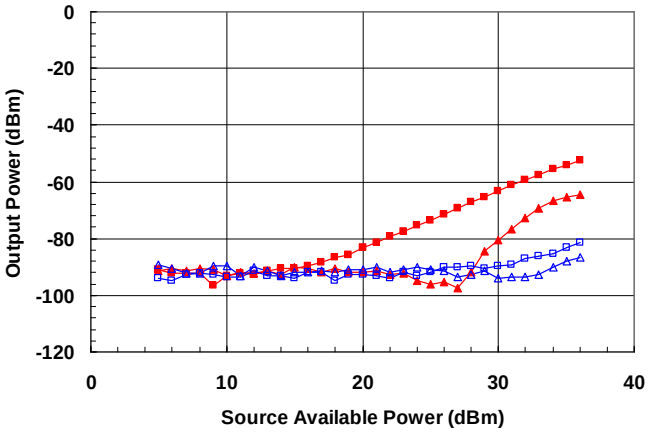

Fig. 5. Measured H2 (squares) and H3 (triangles) from a thru line on a HR SOI substrate with no shielding (full symbols) and with shielding (open symbols).

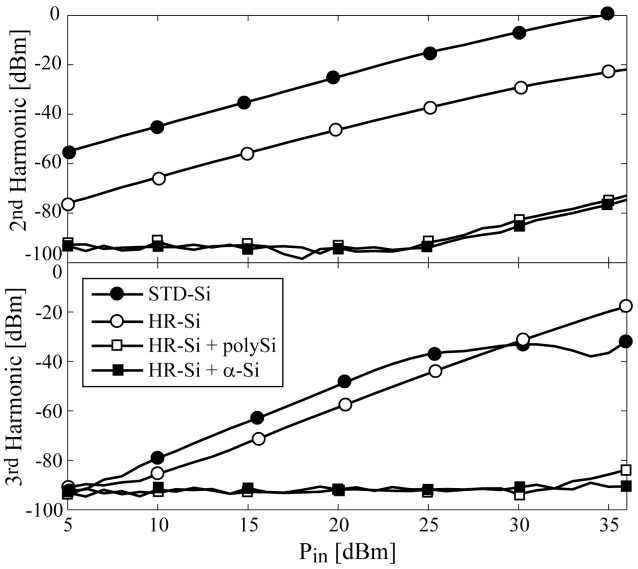

Fig. 6. Measured H2 and H3 from a 2.1 mm-long CPW line on various oxidized (60 nm of oxide) Si substrates: 20 Ω-cm, 1 kΩ-cm, and two types of HRS substrates with trap-rich layer. The trap-rich layer significantly reduces HD by at least 50 and 65 dB for H2 and H3, respectively.

Fig. 6 shows the effect of different silicon substrate resistivities. The 1 kΩ-cm substrate has lower HD over most of the power sweep. The response of HD to DC bias is shown in Fig. 7. It was found that for this HRS substrate, HD is bias dependent, but there is no DC bias which universally reduces HD.

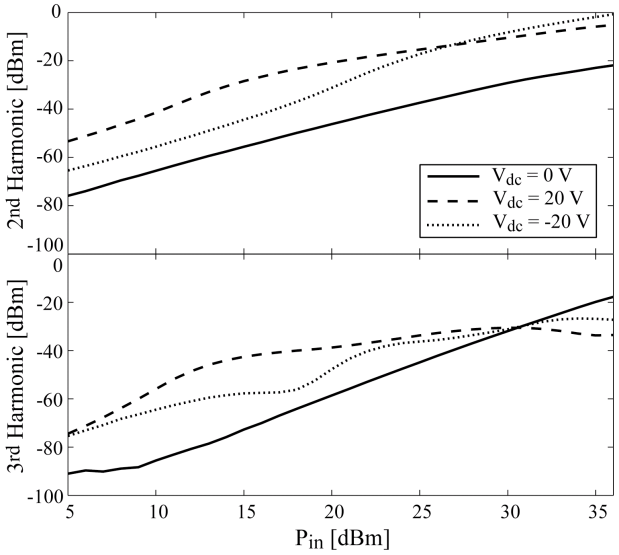

Fig. 7. Measured H2 and H3 for a 2.1 mm long line on oxidized (60 nm of oxide) HRS substrate for different DC biases applied to the center conductor of CPW line. The DC bias increases HD for all power levels.

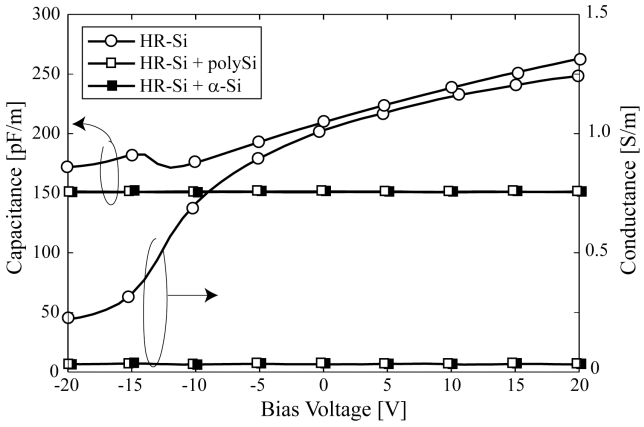

Fig. 8. Extracted capacitance and conductance from small-signal S-parameter measurements at 900 MHz versus DC bias applied to the center conductor of the CPW line.

III. Origin of Distortion

The origin of the HD is nonlinear capacitance (C) and conductance (G) related to the changing distribution of free carriers inside the silicon substrate. The transmission line C and G can be extracted using small-signal S-parameter measurements versus DC bias, as shown in Fig. 8. The extracted values can be directly related to HD if the non-quasistatic behavior of the substrate is not important. The variation of the C and G parameters versus DC bias clearly appears in the case of the CPW line lying on the HR-Si substrate.

IV. Substrate Passivation

It is known that HRS substrates suffer from a parasitic surface conduction (PSC) layer caused by fixed oxide charge [3-6]. This PSC degrades transmission line losses and RF isolation, and also serves as the source for electrons for regions beneath CPW signal line. In order to eliminate PSC, some authors have shown that a trap-rich polycrystalline layer on the HRS substrate improves transmission line losses (Fig. 9) and isolation [5-8].

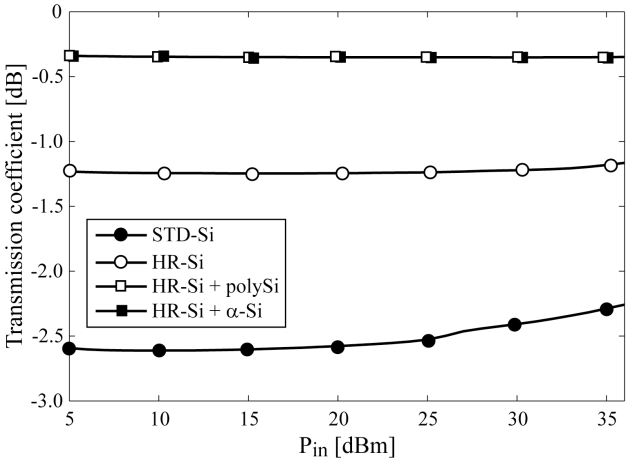

Fig. 9. Measured transmission coefficient for various substrates. Substrates with polysilicon or amorphous silicon have significantly lower transmission line losses.

Fig. 6 also shows the harmonics of Al metal lines on thermally-oxidized HRS p-type substrates with a trap-rich layer. A 300 nm-thick polycrystalline silicon film is deposited directly on the HRS substrate, and a 60 nm-thick oxide was grown on top of the polysilicon layer. For the first time, it is shown that substrate passivation with a trap-rich layer reduces impressively the measured harmonics to the noise floor, namely, at least a 50 and 65 dB reduction in H2 and H3, respectively. Moreover, as shown in Fig. 10 the DC bias applied at the central conductor of the CPW line has only a weak impact on HD thanks to the high-density of traps which pin the bias conditions at the SiO_2/Si interface.

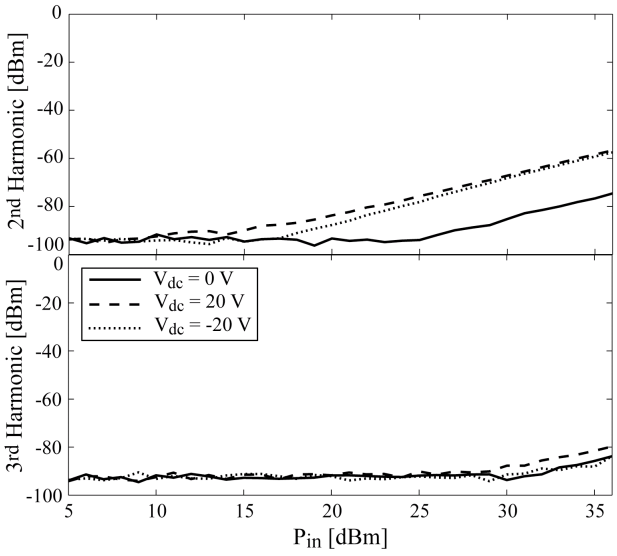

Fig. 10. Measured H2 and H3 for polysilicon passivated HRS substrate versus DC bias applied to the center conductor. The structure has 60 nm oxide over the passivation layer.

As explained above, thanks to the high density of traps in the polysilicon or amorphous silicon layer located at the SiO_2-Si interface, the surface potential at this interface is nearly fixed and then external DC bias or large amplitude RF signal applied to the line do not impact the distribution of carriers inside the Si substrate. Constant values for C and G parameters versus DC bias are indeed measured in Fig. 8. These measurements demonstrate the high efficiency of the trap-rich layer to drastically reduce the harmonic distortion originating from the HR Si substrate as previously shown in Fig. 6.

V. Conclusion

Harmonic distortion is measured from coplanar waveguide structures on various substrates at 900 MHz, and significant distortion for high resistivity silicon substrates is demonstrated for the first time. The measured levels of H2 and H3 are high compared to a full cellular transmit switch product spec of -45 and -40 dBm.

Harmonic distortion in Si substrate has been reduced by at least 5 orders of magnitude thanks to the introduction of a trap-rich layer at the SiO_2-Si interface. This technological solution is then extremely promising for the development of highly linear RF blocks on HR silicon substrate required for the future communication systems.

Acknowledgement

The authors wish to acknowledge Dr. Dimitri Lederer for the design and the fabrication of the passivated HR silicon substrates.

References

[1] C. Tinella, O. Richard, A. Cathelin, F. Reaute, S. Majcherczak, F. Blanchet, and D. Belot, “0.13 µm CMOS SOI SP6T antenna switch for multi-standard handsets”, *Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*, Jan. 18-20, 2006, p. 58.

[2] T. McKay, M. Carroll, J. Costa, C. Iversen, D. Kerr and Y. Remoundos, “Linear cellular antenna switch for highly-integrated SOI front-end”, *IEEE International. SOI Conference*, 2007.

[3] A.C. Reyes, S.M. El-Ghazaly, S.J. Dorn, M. Dydyk, D.K. Schroder and H. Patterson, “Coplanar waveguides and microwave inductors on silicon substrates”, *IEEE Trans. Microwave Theory Tech*., 43(9), pp. 2016-2021, 1995.

[4] Y. Wu, H.S. Gamble, B.M. Armstrong, V.F. Fusco, J.A.C. Stewart, “SiO_2 interface layer effects on microwave loss of high-resistivity CPW line”, *IEEE Microwave and Guided Wave Letters*., 9(1), pp. 10-12, 1999.

[5] H.S. Gamble, B.M. Armstrong, S.J.N. Mitchell, Y. Wu, V.F. Fusco, J.A.C. Stewart, “Low-loss CPW lines on surface stabilized high-resistivity silicon”, *IEEE Microwave Guided Wave Let*., 9(10), pp. 395-397, 1999.

[6] D. Lederer, R. Lobet and J.-P. Raskin, “Enhanced high resistivity SOI wafers for RF applications”, *IEEE International SOI Conference*, Charleston, South Carolina, October 4-7, 2004, pp. 46-47.

[7] D. Lederer, B. Aspar, C. Laghaé and J.-P. Raskin, “Performance of RF passive structures and SOI MOSFETs transferred on a passivated HR SOI substrate”, *IEEE International SOI Conference*, Niagara Falls, New York, USA, October 2-5, 2006, pp. 29-30.

[8] D. Lederer and J.-P. Raskin, “New substrate passivation method dedicated to high resistivity SOI wafer fabrication with increase substrate resistivity”, *IEEE Electron Device Letters*, vol. 26, no. 11, pp. 805-807, November 2005.