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RESEARCH

A Novel High-Performance CMOS VCRO Based on Electrically Doped Nanowire FETs in 10 nm Node

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Abstract
In this paper, the idea of electrically doped (ED) Nano-scale TFETs is used to design a non-tunneling n-type NWFET with an additional gate named the side-gate (SG). The work function of SG and the effects of its voltage on the performance of the ED-NWFET device are analyzed. A conventional p-type NWFET and the proposed n-type ED-NWFET are used to design a CMOS inverter, which exhibits considerable dependency on the voltage of the side-gate. Three stages of this inverter are used to design a CMOS voltage-controlled ring oscillator (VCRO), which has a high frequency range of 89.2 to 465 GHz for the side-gate voltage range of 0 to 1 V. Consequently, it has a high frequency tuning range of approximately 136%. The tuning range, phase noise, figure of merit (FoM) and the figure of merit with tuning range (FoM_T) of the proposed VCRO are superior in comparison with other reported VCROs. The proposed VCRO also has excellent linear frequency-voltage characteristics in the side-gate voltage range of 0.2 to 0.5 V. This linear VCRO exhibits superior performance, including a wide frequency range, compared to other linear VCROs. The results presented in this paper have demonstrated the efficacy of the proposed Nano-scale device engineering-based circuit design technique for applications over a wide frequency range.

Keywords Nanowire (NW) FET · Electrically Doped (ED) · CMOS inverter · Voltage-Controlled Ring Oscillator (VCRO)

1 Introduction

In recent CMOS circuit research, the CMOS ring oscillator has many significant applications such as the high-speed clock signals, the modern internet of thing (IoT) [1], communication circuits [2]. S. A. Sedigh Ziabari et al. in [3] presents a new Step Doped Drain and Source Nanowire FET (NWFET) using doping profile engineering. A CMOS inverter and ring oscillator (RO) based on this device are proposed and investigated. In this work the device engineering-based circuit design is accomplished. A step doping profile in the source and drain is proposed. The effect of the profile decreases the *off-current* and subthreshold swing and increases the *on–off current ratio.* The oscillation frequency of the CMOS ring oscillator designed base on the proposed NWFET, and its power consumption are dependence on the height of the doping step. S. Seifollahi et al. in [4] the Nano-scale double-gate FET-based CMOS ring oscillator is proposed. In this circuit by a special changing the source and channel doping concentration, the oscillation frequency is slightly increased. The device engineering-based ring oscillator design strategy is also used in this paper. A gallium nitride (GaN)-based 9-stages ring oscillator is presented by Z. Zheng et al. in [5]. The CMOS ring oscillator design based on Si Gate-All-Around Nanowire MOSFET is presented by K. Nayak et al. in [6]. Various researches have been accomplished on the characteristics and performance of VCOs, such as modification of the oscillation frequency range in 180 nm CMOS Technology [7], design of three and nine stages voltage-controlled ring oscillators in TSMC 0.18-μm CMOS technology with the maximum oscillation frequency 5.9 GHz [8], investigation of an area-efficient

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high-performance VCO in Nano-scale CMOS [9], the design and performance analysis of a 15-GHz five-stage voltage-controlled ring oscillator in the 130-nm CMOS technology with 1.8 V power supply for high-speed applications [10], the performance assessment and characterization of CMOS VCRO with emphasis on high frequency, low area, and low phase noise at different values of power supply [11], investigation the effects of scaling on the performance of a floating-gate metal–oxide–semiconductor (FGMOS) transistor-based VCRO [12]. Several designing high figure of merit (FoM) CMOS VCOs with oscillation frequency above 100 GHz in Si-based technologies have been reported in recent years [13–16].

In the CMOS ring oscillators and VCROs, some of design goals and characteristics such as the scaling, the level of bias, the power consumption, the value and range of oscillation frequency, the phase noise, and the figure of merit have been considerable. One significant strategy to design and modify these circuits in the Nano-scale is device-based circuit engineering [4–6]. The Nanowire FET is a considerable choice because of the reduced short channel effects (SCEs) due to appropriate electrostatic treatment, the superior on–off current ratio, suitable compatibility with CMOS fabrication process [6]. On the other hand, the electrically doping idea to design Nano-scale tunneling FETs is a considerable method [17–19]. It can be useful to design none-tunneling Nano-scale FETs for special circuit applications. In this work, we concentrate on the silicon NWFET-based CMOS ring oscillator and the design of a CMOS voltage-controlled ring oscillator (VCRO) based on p-type NWFETs and n-type electrically doped (ED) NWFETs and various evaluation of the proposed VCRO.

2 Proposed Electrically Doped-NWFET

Figure 1(a) shows the cross-section of a *n*-type NWFET and its schematic symbol. The source and drain have uniform *n*-type doping concentration (N_{DS} and N_{DD}) of 1×10^{19} cm^{-3} and the channel is intrinsic. The drain and source lengths are 15 nm each and the channel length (L_G) is 10 nm. The material of the device is silicon with a thickness and width of 5 nm. The oxide is SiO_2 with a thickness of 1 nm. The distance between the side gate and the gate is 1 nm. Devices with 1 ~ 2 nm of Lgg can be built [20, 21]. The side gate provides additional control on the *source* in the junction region between the *source* and the *channel*. The *p*-type NWFET is designed by inverting the source and drain doping types with similar doping concentrations. The device-level simulations have been done using the 2D ATLAS device simulator. The model used in simulation is the non-equilibrium Green's function (NEGF) due to its high accuracy in modeling the

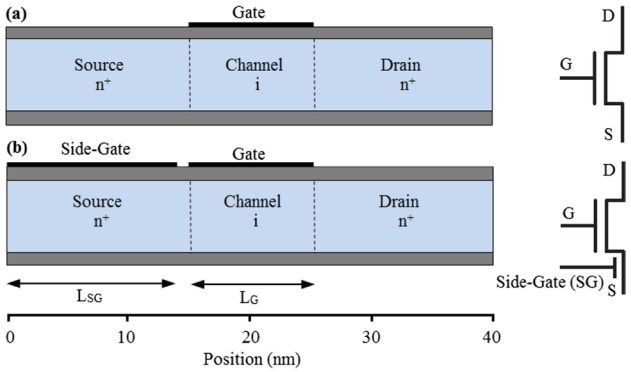

Fig. 1 **a** Cross section of NWFET and its schematic symbol, **b** cross section of ED-NWFET and its proposed schematic symbol

electron quantum behavior for the *on*- and *off*- states in these dimensions [22, 23].

In device-level engineering approaches to design high-performance Nano-scale tunneling FETs, an important direction is the idea of electrically doping various regions of the FET. In a MOS structure with bias V_M on the metal gate, the relationship between the Fermi levels (E_F) of metal and semiconductor is expressed as follows:

$$E_F(metal) - E_F(semiconductor) = -qV_M \tag{1}$$

For $V_M \neq 0$, the semiconductor Fermi level is unaffected by the bias because the current flow is assumed to be zero. Therefore, with $V_M > 0$, E_F *(metal)* has downward movement based on the value of V_M [24]. Accordingly, the idea behind 'electrically doping' the source of the FET is that it can provide additional control. The initially heavily doped N^+ for source, channel and drain are converted into P^+-I-N^+ (source-channel-drain) by the metal work function of the gates and the applied bias. By the selection of identical appropriate work functions of the control gate (CG) on the channel and the polarity gate (PG) on the source, these regions change to the intrinsic types. The source is changed to the P^+ region by the application of a negative bias voltage to the PG. This type of device is known as Electrically Doped (ED)-TFET. Variation of the polarity gate voltage changes the electric field and so the energy levels in the energy band diagram. This treatment is similar to changing the doping concentration of the source. Therefore, the external bias level of the PG can control the ED-TFET characteristics such as the *on-current*, the *off-current*, the threshold voltage, the sub-threshold swing, and improve the device performance for digital or analog applications [17–19]. The electrically doped idea can be useful method to design none-tunneling FETs in Nano-scale for achieving special circuit applications, which is considered in this paper. The proposed electrically doped non-tunneling (ED)-NWFET

and its schematic symbol are presented in Fig. 1(b). In this device, the 'electrically doped' idea is implemented on the n^+ source by implanting a side-gate (SG) with a length of 14 nm.

2.1 Proposed VCRO Design Methodology

The design strategy of the CMOS voltage-controlled ring oscillator is based on proposing a *n*-type electrically doped SOI-NWFET with two separate gates. The methodology comprises the following four steps.

a) First, a *n*-type electrically doped NWFET is designed to achieve an additional gate on the source named the side-gate (SG). This terminal controls the electrical characteristics of the source and consequently that of the device commensurate with its metal work function (WF) and voltage.
b) The above *n*-type ED-NWFET and a conventional *p*-type NWFET are used to design a CMOS inverter with its delay dependent on the side-gate voltage in a distinct WF.
c) A voltage-controlled ring oscillator (VCRO) is designed using the inverter from step (b) and its characteristics is investigated.
d) The oscillation frequency (f_{osc}) of the VCRO is calculated for different side-gate voltages. The instantaneous power and the average DC power consumption of the oscillator are also calculated.

3 Characteristics of the Proposed ED-NWFET

Our device simulation using the 2D ATLAS device simulator with the non-equilibrium Green's function (NEGF) model is first calibrated based on the drain-to-source current (I_{DS}) versus gate-to-source voltage (V_{GS}) characteristics reported in [22] and illustrated in Fig. 2. It can be seen that our simulation results and the results of [22] match very closely.

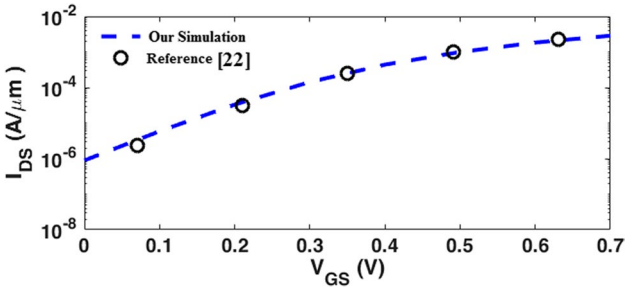

Fig. 2 Calibration of the simulation result with the result reported in [22]

Figure 3 illustrates the energy band diagram (EBD) of NWFET for the source doping concentrations (N_{DS}) of 1×10^{19}, 0.5×10^{19} 0.2×10^{19} and 1×10^{18} cm^{-3}. It also shows the EBD of ED-NWFET for the side-gate work function of 4.6 eV with $N_{DS}=1\times10^{19}$ when $V_{SGS}=0$ V and $V_{GS}=V_{DS}=0$ V. Figure 3 shows that decreasing the N_{DS} of NWFET moves the source conduction band (CB) and valence band (VB) upward. Comparing the energy bands of ED-NWFET with NWFET at $N_{DS}=1\times10^{19}$, the proposed additional gate (SG) on the source of the ED-NWFET device moves the EBD upward, which has a similar effect to that of decreasing the N_{DS} in NWFET. Consequently, the proposed device illustrated in Fig. 1(b) is named the electrically doped (ED) NWFET.

Figure 4(a) and Fig. 4(b) show the electron concentration of NWFET for N_{DS} of 1×10^{19} cm^{-3} and 1×10^{18} cm^{-3}, while Fig. 4(c) shows the electron concentration of ED-NWFET for the side-gate work function of 4.6 eV for $N_{DS}=1\times10^{19}$ cm^{-3}, $V_{SGS}=0$ V, $V_{GS}=0$ and $V_{DS}=0$ V. Clearly, the electron concentration at the source of the ED-NWFET in Fig. 4(c) is lower than that of the NWFET in Fig. 4(a) for the same value of $N_{DS}=1\times10^{19}$. Therefore, it can be concluded that the effect of the side-gate on the source electron concentration of the device is similar to that of decreasing the source doping concentration of the NWFET from 1×10^{19} cm^{-3} to 1×10^{18} cm^{-3} as shown in Fig. 4(a) and Fig. 4(b), respectively. Therefore, the results of Fig. 4 reinforce the observation made above from the energy band diagrams of Fig. 3. A distinct source doping concentration is determined in manufacturing process and it is invariable and uncontrollable after manufacturing. We use the electrically doped idea to provide an additional terminal for FET in order to control the source doping profile

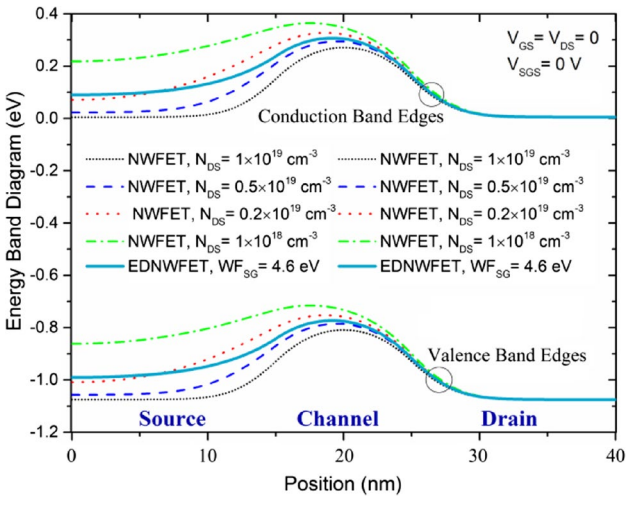

Fig. 3 The energy band diagram (EBD) of NWFET for N_{DS} of 1×10^{19}, 0.5×10^{19}, 0.2×10^{19} and 1×10^{18} cm^{-3} and ED-NWFET for $N_{DS}=1\times10^{19}$ with $WF_{SG}=4.6$ eV, $V_{SGS}=0$ V and $V_{GS}=V_{DS}=0$ V

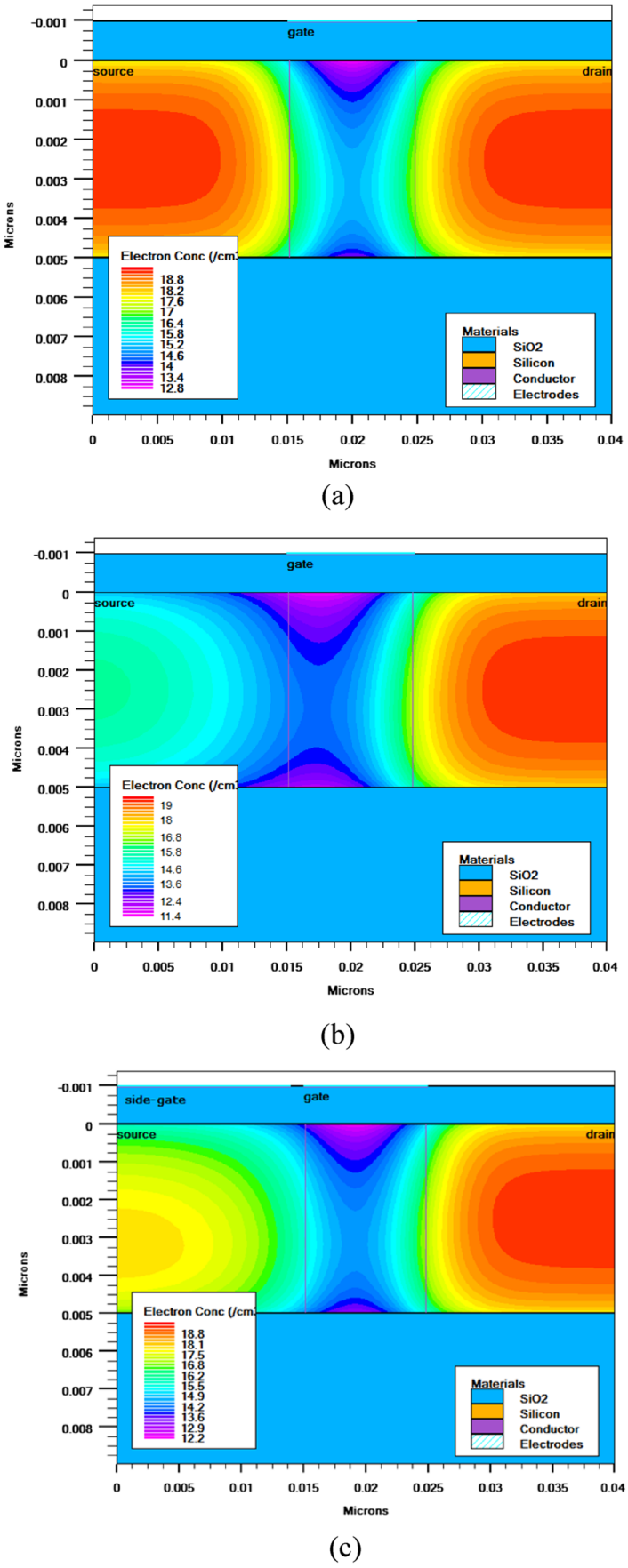

Fig. 4 The electron concentration of NWFET for the source doping concentrations (N_{DS}) of (**a**) 1×10^{19} and (**b**) 1×10^{18}; (**c**) electron concentration of ED-NWFET for $N_{DS}=1\times10^{19}$ with $WF_{SG}=4.6$ eV, $V_{SGS}=0$ V and $V_{GS}=V_{DS}=0$ V

by an external applied bias. The voltage-controlled source can provide different circuit applications such as the CMOS inverter and the voltage-controlled ring oscillator. Therefore, a designed circuit based on the type of device has an additional terminal which can control, modify or improve its characteristics using applied bias.

Figure 5 shows the drain-source current versus V_{GS} of the NWFET and ED-NEFET for the side-gate work function (WF_{SG}) of 4.2 and 4.6 eV. The side-gate to source voltage (V_{SGS}) and the drain to source voltage (V_{DS}) are 0 V and 1 V, respectively. It is observed that the side gate of the ED-NWFET with work function of 4.2 eV leads to decrease in the *on-current* ($V_{GS}=1$ V) and slight increase in the *off-current* ($V_{GS}=0$ V) compared to the NWFET. By increasing WF_{SG} to 4.6 eV the drain-to-source current (I_{DS}) is reduced considerably in both the *on-* and *off-states*. To analyze this further, the conduction bands of NWFET and ED-NWFET for the side-gate work functions (WF_{SG}) of 4.2 eV and 4.6 eV are illustrated in Fig. 6 in both the *on-state* ($V_{GS}=1$ V) and the *off-state* ($V_{GS}=0$ V). It can be seen in Fig. 6 that, compared with NWFET, the side-gate in the proposed ED-NWFET raises the *source* energy bands in the *on-state*. The amount of increase is higher with higher value of the side-gate work function (WF_{SG}). This behavior is similar to the effect of decreasing the doping concentration of the *source* as illustrated in Fig. 3, and consequently decreasing the *on-current* which was illustrated in Fig. 5. Moreover, Fig. 6 shows that in the *off-state*, the side-gate with WF_{SG} of 4.2 eV leads to a slight reduction in the channel potential barrier and consequently, a slight increment in the *off-current* that was observed in Fig. 5. However, the increased WF_{SG} of 4.6 eV leads to a considerable increase of the conduction band in the *off-state*, and therefore reducing the *off-current* by nearly an order of magnitude as seen in Fig. 5. In all the subsequent analysis presented in the rest of this paper, the SG work function is assumed to be 4.2 eV.

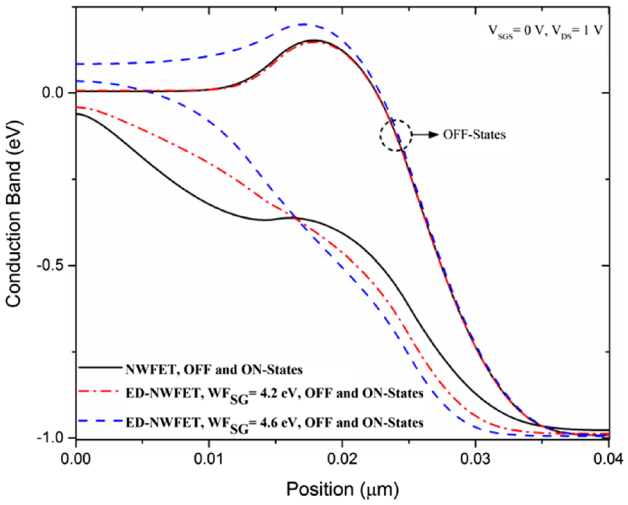

Fig. 6 The conduction bands of NWFET and ED-NWFET with $V_{SGS}=0$ V and $V_{DS}=1$ V for $WF_{SG}=4.2$ eV and 4.6 eV, in the *on-state* ($V_{GS}=1$ V) and *off-state* ($V_{GS}=0$ V)

The conduction bands of NWFET and ED-NWFET for $V_{SGS}=0$, 0.2 and 0.4 V in the *on-* and *off-states* are shown in Fig. 7. The positive bias applied to the side-gate causes the electric field to permeate through the *source* and move the energy band diagram downward. This behavior is similar to increasing the source doping concentration. The positive bias applied to the side-gate changes the level of energy bands and consequently, influences the device characteristics such as *off-current*. The ability to control these important parameters of the NWFET using the proposed side-gate will provide flexibility and improve circuit-level performance.

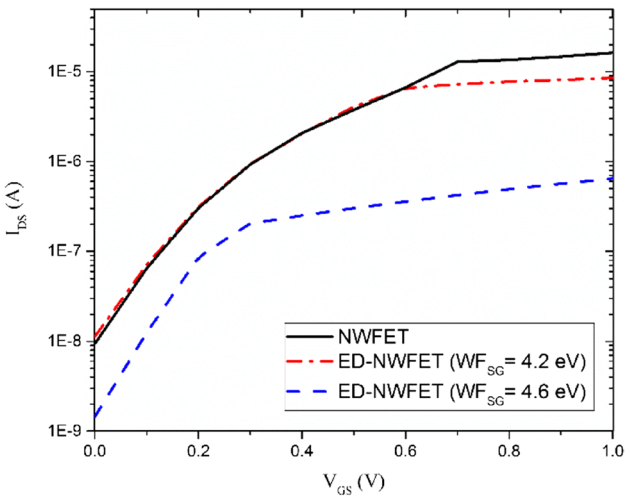

Fig. 5 The drain-source current versus V_{GS} of NWFET and ED-NEFET with $V_{SGS}=0$ V and $V_{DS}=1$ V for $WF_{SG}=4.2$ eV and 4.6 eV

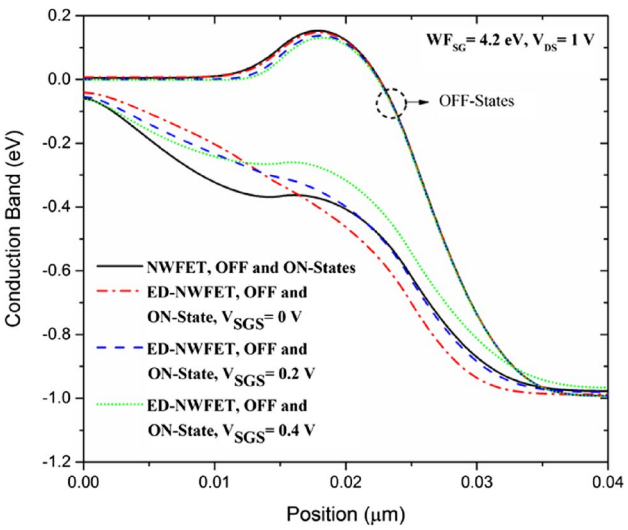

Fig. 7 The conduction bands of NWFET and ED-NWFET for $WF_{SG}=4.2$ eV in *on-* and *off-states* for $V_{SGS}=0$, 0.2 and 0.4 V

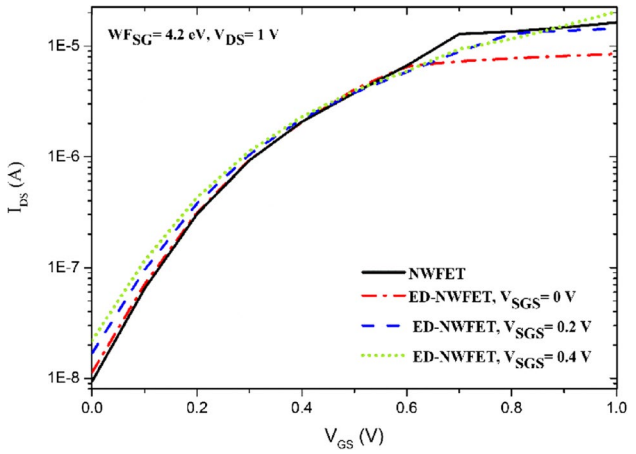

Fig. 8 The drain-source current versus V_{GS} of NWFET and ED-NWFET with WF_{SG}=4.2 eV and V_{DS}=1 V for V_{SGS}=0, 0.2 and 0.4 V

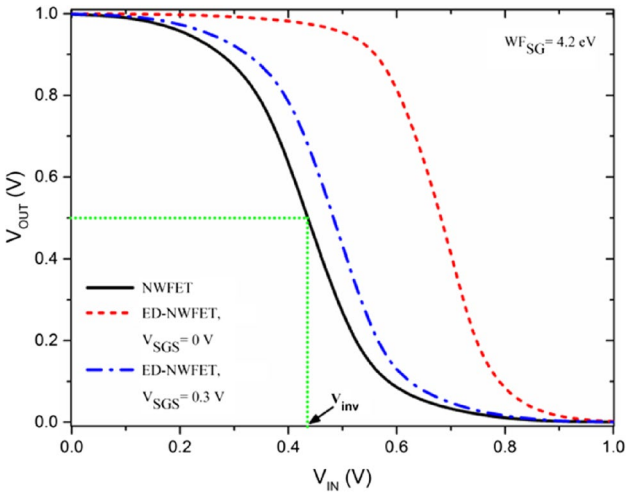

Fig. 10 Voltage transfer characteristics (VTC) of the inverters designed using n-type NWFET and n-type ED-NWFET for V_{SGS}=0 and 0.3 V with WF_{SG}=4.2 eV

Figure 8 shows the drain-source current versus V_{GS} of the NWFET and the ED-NWFET for V_{SGS}=0, 0.2, and 0.4 V. This figure illustrates that the *on-current* (V_{GS}=1 V) increases with the increment of the side-gate voltage. In the *off-state*, increasing V_{SGS} increases the *off-current* (V_{GS}=0 V) due to the decrement of the potential barrier in the *off-state* as exhibited in Fig. 7.

4 Application of ED-NWFET and Results – Voltage-Controlled Ring Oscillator

Figure 9(a) shows a CMOS inverter designed using a *p*-type NWFET without any changes and the proposed *n*-type ED-NWFET of Fig. 1(b). The side-gate of the *n*-type device is an independent input terminal of the CMOS inverter. Figure 9(b) shows the proposed CMOS voltage-controlled ring oscillator (VCRO) designed using three stages of the inverter. The oscillation frequency relationship for a distinct value of V_{SGS} is $f_{osc} = 1/(2 \times N \times t_d)$, where N and t_d are the number of inverter stages and the propagation delay per stage, respectively. The V_{SGS} is a voltage control terminal of the proposed VCRO, which has an influence on t_d, and in consequence f_{osc}. All the simulations have been carried out using ATLAS/Mixed-Mode.

4.1 Transfer Characteristics of the ED-NWFET-Based Inverter

First, we compare the voltage transfer characteristic (VTC) of the inverter of Fig. 9(a), which uses an *n*-type ND-NWFET proposed in this paper, with the VTC of an inverter using a conventional n-type NWFET. Figure 10 shows the voltage transfer characteristics (VTC) of a CMOS inverter using a conventional n-type NWFET and that of the inverter of Fig. 9 (a) which uses the proposed n-type ED-NWFET for V_{SGS} values of 0 V and 0.3 V with WF_{SG}=4.2 eV. In comparison with the *n*-type NWFET-based inverter, the metal work function of the SG in the inverter of Fig. 9(a) shifts the VTC to the right for V_{SGS}=0 V, whereas for V_{SGS}=0.3 V the effect of the metal work function is compensated by the increased side-gate voltage, and consequently the amount of shift is reduced. The inversion voltages (V_{inv}) of these three inverters are 0.43, 0.48 and 0.68 V. In order to analyze V_{inv}, we use the *r* criterion of the CMOS inverter [25]

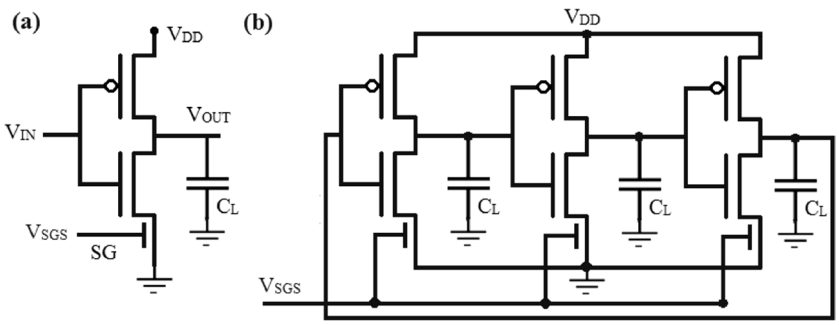

Fig. 9 **a** the CMOS inverter designed using p-type NWFET and the n-type ED-NWFET of Fig. 1(b), **b** the proposed CMOS voltage controlled ring oscillator (VCRO)

to determine the inverter threshold characteristics which is defined by

$$r = \beta_p/\beta_n = W_p v_{sat-p}/W_n v_{sat-n} \quad (2)$$

where, W_p and W_n are the gate widths of the p- and n-type transistors, $v_{sat\text{-}p}$ and $v_{sat\text{-}n}$ are the carrier saturation velocities for the p- and n-type devices, respectively. Increasing r leads to increase in V_{inv} [25]. In this work, only the $v_{sat\text{-}n}$ is varied in the different designs of the inverter, and therefore the r values are commensurate with the variations of $v_{sat\text{-}n}$. To analyze the increase of V_{inv} in the ED-NWFET-based inverter for $V_{SGS}=0$ V in comparison with that of the NWFET-based inverter, the square of wave function or the probability density of electron is calculated for both the NWFET and ED-NWFET devices, which are shown in the Fig. 11. It can be seen in this figure that the probability density of electron in the channel of ED-NWFET is more than that of NWFET. Therefore, the velocity of electron ($v_{sat\text{-}n}$) in its channel is less compared with that of NWFET [26]. The lower $v_{sat\text{-}n}$ leads to increase in the value of r, and consequently increases V_{inv}.

4.2 Transient Response of the ED-NWFET-Based Inverter

Figure 12 illustrates the transient response of the two inverters using conventional n-type NWFET and the proposed n-type ED-NWFET with $V_{SGS}=0.2$, 0.4, 0.9 and 1 V. The inverter based on ED-NWFET has the highest delay at $V_{SGS}=0.2$ V and the least delay at $V_{SGS}=1$ V. Increasing V_{SGS} above 0.2 V compensates the effect of WF_{SG}, and consequently the delay is decreased with increasing V_{SGS}.

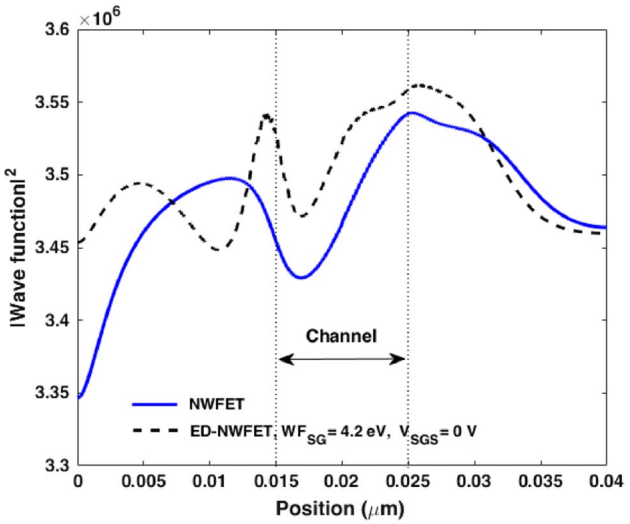

Fig. 11 The square of wave function or the probability density of electron calculated for NWFET and ED-NWFET with $V_{SGS}=0$ V

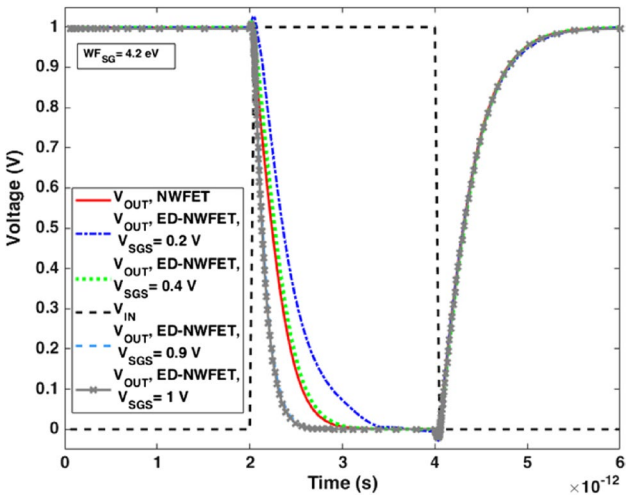

Fig. 12 The transient response of inverter to input pulse for NWFET and ED-NWFET at $V_{SGS}=0.2$ and 0.4 V

It is obvious that the delays for V_{SGS} values of 0.9 V and 1 V are approximately identical. In the other words, the decrease in delay with increasing V_{SGS} is saturated after $V_{SGS}=0.9$ V.

5 Performance of the Proposed VCRO

The voltage output signal of the ring oscillator (RO) designed using the conventional n-type NWFET measured form the third-stage input node is shown in Fig. 13(a) and has an oscillation frequency of 4.16×10^{11} Hz. Figure 13(a) also exhibits the DC supply instantaneous power (p_{VDD} (t)). The average DC power ($P_{VDD\text{-}Av}$) is calculated from p_{VDD}(t) by integrating it from 0 and $T_t=12\times10^{-12}$ s. $P_{VDD\text{-}Av}$ for this RO is 0.0038 W at the oscillation frequency of 4.16×10^{11} Hz. The output signals of the voltage-controlled ring oscillator (VCRO) of Fig. 9(b) based on the proposed n-type ED-NWFET are illustrated in Fig. 13(b), (c) and (d) with $V_{SGS}=0.2$ V, 0.3 V and 0.4 V respectively. The oscillation frequencies and the corresponding values of $P_{VDD\text{-}Av}$ are 2.49×10^{11}, 3×10^{11} and 3.512×10^{11} Hz, and 0.0025, 0.003 and 0.0034 W, respectively. In this VCRO, increasing V_{SGS} leads to increase in f_{osc} and $P_{VDD\text{-}Av}$. The reason of this treatment is the increase of the DC power supply current commensurate with the increase of V_{SGS}.

Figure 14 illustrates that the f_{osc} increases with increasing V_{SGS} from 0 to 1 V. The value of f_{osc} for $V_{SGS}=0$ V is 89.2 GHz and is named f_{min}; while the value of f_{osc} for $V_{SGS}=1$ V is 465 GHz and is named f_{max}. The frequency tuning range is given by

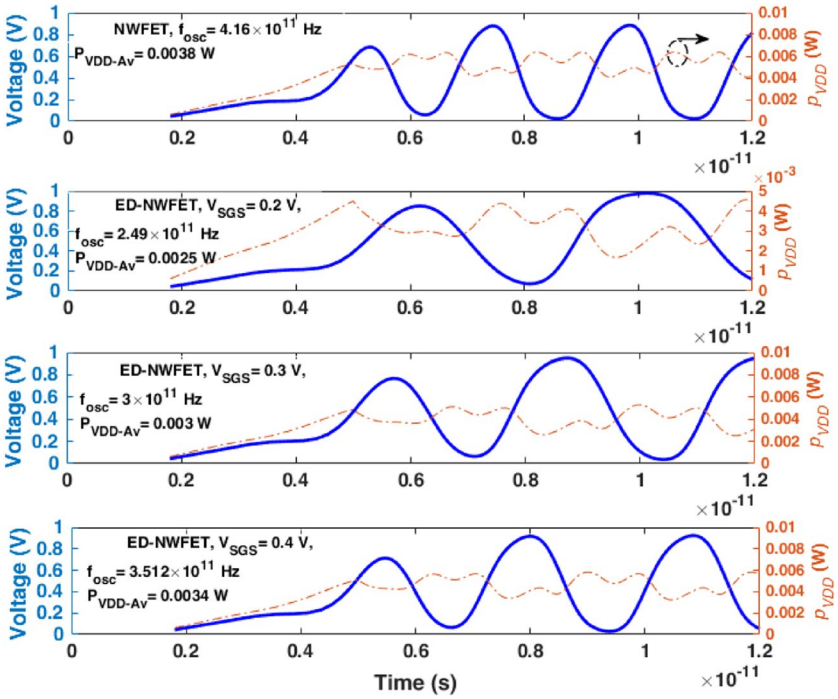

Fig. 13 The output signal of ring oscillator (a) and VCRO with V_{SGS}=0.2, 0.3 and 0.4 V (b, c, and d) and p_{VDD} (t) for the four cases

$$FTR(\%) = \frac{f_{max} - f_{min}}{(f_{max} + f_{min})/2} \times 100 \tag{3}$$

Using (3), the value of *FTR* is found to be 135.61%. The *phase noise* at f_0=351.25 GHz, V_{SGS}=0.4 V and *offset frequency* (Δf) of 10 MHz is -145.51 dBc/Hz. The standard *figure of merit* (*FoM*) and the *figure of merit* with tuning range (FoM_T) are defined as [27, 28]

$$FoM = L(\Delta f) - 20log(\frac{f_0}{\Delta f}) + 10log(\frac{P_{DC}}{1mW}) \tag{4}$$

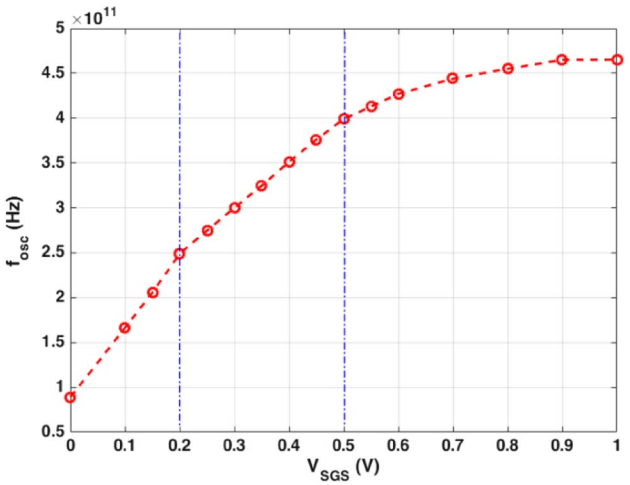

Fig. 14 f_{osc} versus V_{SGS} from 0 to 1 V

$$FoMT = L(\Delta f) - 20log(\frac{f_0}{\Delta f}) - 20log(\frac{FTR}{10}) + 10log(\frac{P_{DC}}{1mW}) \tag{5}$$

Here, $L(\Delta f)$ is the *phase noise* at a specific frequency (f_0) and *frequency offset* (Δf), P_{DC} is the DC power consumption and FTR is frequency tuning range which is represented by (3).

Table 1 provides a comparison of performance of the VCRO presented in this paper and other VCOs reported in the literature. Clearly, the proposed VCRO has the highest frequency range, highest frequency tuning range (FTR) and the lowest average DC power consumption compared all the literature summarized in Table 1. The magnitudes of the *figures of merit*, *FoM* and FoM_T, are higher than those of the other VCOs shown in Table 1. The *phase noise* at the *offset frequency* (Δf) of 10 MHz is -145.5 dBc/Hz, which is the lowest in comparison with those of the other works. Therefore, overall, our proposed VCRO has much superior performance.

6 Performance of the Proposed VCRO in Linear Region

As shown in Fig. 14, the f_{osc}-V_{SGS} characteristic is approximately linear in two V_{SGS} regions, i.e., from 0 V to 0.2 V and 0.2 V to 0.5 V. There is negligible increase of f_{osc} after V_{SGS}=0.9 V, because of the saturation of the decrease in propagation delay which was explained in Section IV.B.

Table 1 Comparison of performance of the proposed VCRO with other VCOs

References	[36]	[13]	[37]	[38]	[39]	[40]	[15]	[27]	[28]	This Work
CMOS Node (nm)	40	28	65	130	130	180	90	90	28	10
Frequency Range (GHz)	13–19	524.7–555.8	22.8–27.3	91–91.45	294.9–304.8	1.61–3.71	290–314.16	13–25	29–49	89.2–465
FTR (%)	37.5	5.9	17.8	0.5	3.3	78.52	8	63.13	68.96	135.6
Phase Noise (dBc/Hz)	-110 @ 1 MHz	-	-105 @1 MHz	-87 @ 1 MHz	-86.6 @10 MHz	-89 @1 MHz	-80.28 @1 MHz	-96.11 @1 MHz	-129.2 @ 1 MHz	-145.51 @10 MHz
V_{DD} (V)	0.8	0.9	1	1.8	3.6	1.8	1.8	1.4	1	1
Power Consumption (mW)	24	19	9.2	46	75.6	10.54	105.6	257	3.75	3.4
FoM	-	-	-186.2	-169.6	-	−150.1	-	-161.8	-217.26	-231.1
FoM_T	-193.76	-	-191.1	-	-	-167.99	-153.4	-177.8	-234.03	-253.75

In order to investigate this aspect, an enlarged view of the f_{osc}-V_{SGS} relationship for the V_{SGS} range of 0.2 V to 0.5 V is illustrated in Fig. 15(a). This figure shows that the value of f_{osc} for $V_{SGS}=0.2$ V is 2.49×10^{11} Hz and is named f_{minL}; and the value of f_{osc} for $V_{SGS}=0.5$ V is 3.99×10^{11} Hz and is named f_{maxL}. Therefore, the tuning range is 249 – 399 GHz. The percentage change in frequency (*PCF*) is 60.24%, which is calculated using (6) [29].

$$PCF(\%)=\frac{f_{maxL}-f_{minL}}{f_{minL}}\times100 \tag{6}$$

The f_{osc}-V_{SGS} relationship given in Fig. 15(a) confirms that it has a linear characteristic in the V_{SGS} range of 0.2 V to 0.5 V and can be fitted with the linear equation $f_{osc}=5.029\times10^{11}V_{SGS}+1.4881\times10.^{11}$. The Non-linearity Error (*NE*) is calculated using (7)

$$NE(\%)=\frac{f_{nonlinear}-f_{linear}}{f_{maxL}-f_{minL}}\times100 \tag{7}$$

A plot of the *NE* calculations for this linear VCRO is illustrated in Fig. 15(b) as a function of V_{SGS}. The maximum amount of *NE* is 0.84%. In order to evaluate the characteristics of the proposed VCRO in the linear region of operation, we use the figure of merit (FoM_L) [29] expressed as

$$FoM\mathrm{L}(\%)=\frac{Maximum\ NE\ (\%)}{PCF(\%)}\times100 \tag{8}$$

A smaller FoM_L value indicates better performance. Table 2 provides a comparison of performance of the linear VCRO presented in this work with other linear VCOs reported in the literature. Our proposed linear VCRO has $FOM_L=1.39\times10^{-2}$, which is less than those of [30] and [31]. The proposed circuit has considerably higher oscillating frequencies and significantly higher frequency range. Our proposed linear VCRO has $NE=0.84\%$, which is less than that of the design 1 of [30] and is equal to that of [29]. In addition, our proposed circuit has $PCF=60.24\%$, which is higher than those of the designs presented in [30] and [31]. While the linear VCO presented in [29] has a much higher PCF value, its frequency range is considerably lower than our proposed VCRO. In fact, the proposed linear VCRO has significantly higher frequency range compared to all the designs summarized in Table 2.

Figure 16 illustrates the output signal waveform of this VCRO in the linear region for a special V_{SGS} signal applied to the side-gate (SG) terminal. It can be seen that as V_{SGS} changes, the frequency of the output signal (V_o) changes, providing flexibility to control the frequency of the VCRO output signal in the linear region. This reinforces the results of Fig. 14.

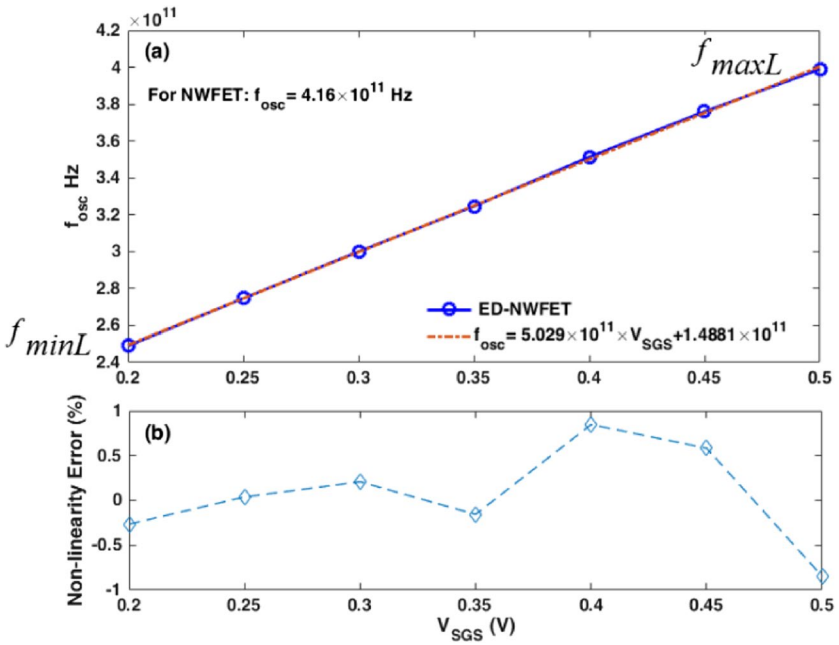

Fig. 15 **a** f_{osc}-V_{SGS} from 0.2 to 0.5 V and its linear approximation with the relationship $f_{osc} = 5.029 \times 10^{11} V_{SGS} + 1.4881 \times 10^{11}$, **b** Non-linearity Error

Table 2 Comparison of performance of the proposed linear VCRO with other linear VCOs

References	[29]	[30] Design 1	[30] Design 2	[31]	This work
CMOS Node (nm)	350	180	180	65	10
Frequency Range (GHz)	4–97 MHz	573– 852.8 MHz	569–717 MHz	4–5 GHz	249–399 GHz
NE (%)	0.84	0.9	0.66	0.5	0.84
PCF (%)	2325	48.8	26	25	60.24
FoM_L	3.6×10^{-4}	1.84×10^{-2}	2.53×10^{-2}	2×10^{-2}	1.39×10^{-2}

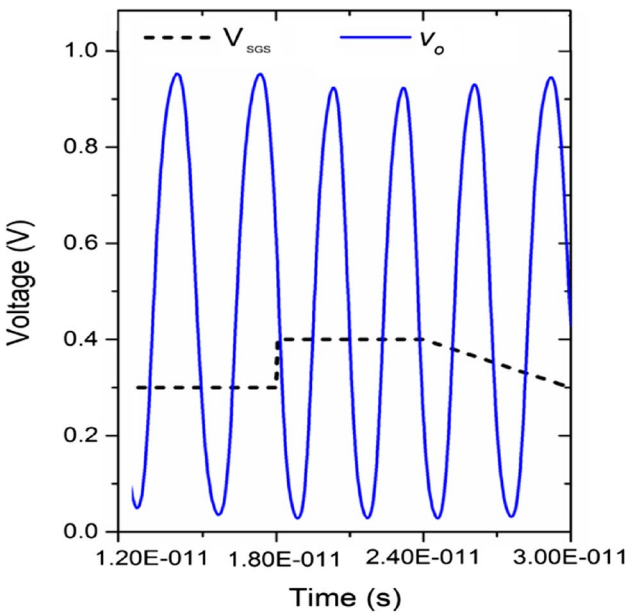

Fig. 16 The output waveform of the VCRO versus a special V_{SGS} signal applied to side-gate (SG) terminal

7 Evaluation of the Effects of Gate Resistance on f_{osc}

The gate width of *n*-type nanowire FET is 5 nm and the gate width of *p*-type Nanowire FET is 10 nm. The gate length and the gate metal thickness (t_g) are assumed 10 nm and 1 nm [32, 33] respectively. The gate metal is TiN with the resistivity of 10.9 μOmh.cm [34, 35]. Therefore, the gate resistances of *n*-type and *p*-type NWFETs (R_{GN} and R_{GP}) are calculated as follows:

$$R_{GN} = (10.9 \times 10^{-6} \times (\frac{5 \times 10^{-7}}{10 \times 10^{-7} \times 10^{-7}})) \times \frac{1}{3} = 18.16\Omega \quad (9)$$

$$R_{GP} = (10.9 \times 10^{-6} \times (\frac{10 \times 10^{-7}}{10 \times 10^{-7} \times 10^{-7}})) \times \frac{1}{3} = 36.3\Omega \quad (10)$$

To assess the effects of R_G on the VCRO oscillation frequency, we have simulated the VCRO with R_{GN} and R_{GP} as shown in Fig. 17. In this figure, the values of R_{GN} and

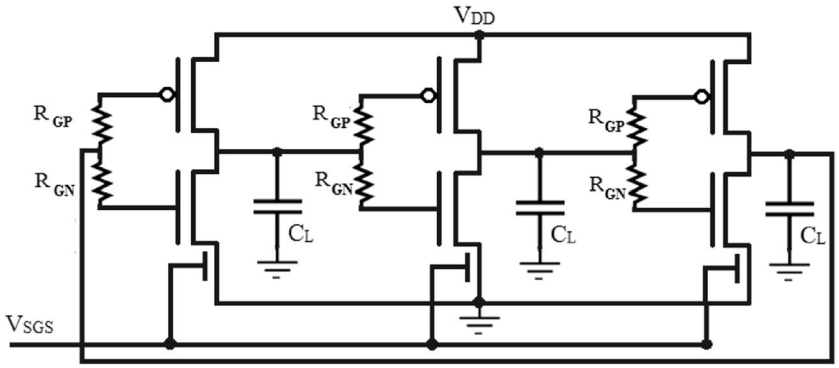

Fig. 17 The CMOS voltage controlled ring oscillator (VCRO) with R_{GP} *and* R_{GN} considered for each transistor

R_{GP} are 18.16 Ω and 36.3 Ω, respectively. The oscillation frequency (f_{osc}) for $V_{SGS}=0.5$ V is found to be 355.8 GHz. Whereas, the oscillation frequency without considering R_{GN} and R_{GP} for $V_{SGS}=0.5$ V is 377 GHz. Hence there is a 5.6% reduction in oscillation frequency when gate resistance is considered.

8 Conclusion

An *n*-type electrically doped (ED) NWFET with an additional gate named the side-gate (SG) has been proposed. A conventional *p*-type NWFET and the proposed *n*-type ED-NWFET have been used to design a CMOS inverter, achieving substantial dependency of the inverter characteristics on the voltage of the SG terminal. The CMOS voltage-controlled ring oscillator (VCRO) designed using three stages of this inverter has a significantly high frequency range of 89.2 to 465 GHz for the control voltage (V_{SGS}) range of 0 to 1 V. This is the highest frequency range among all the VCROs it has been compared against. The proposed VCRO has very small average DC power consumption, which is dependent on V_{SGS} and consequently on f_{osc}. Its *phase noise* at 10 MHz is -145.51 dBc/Hz, which is the lowest value in comparison with those of other VCOs. The figure of merit (*FoM*) and the figure of merit with tuning range (FoM_T) are 231.1 and -253.75 respectively, which are higher than the values for other structures. These parameters indicate superior performance of the proposed VCRO in comparison with other VCROs reported in the literature. In addition, the proposed VCRO has an approximately linear behavior in the V_{SGS} range of 0.2 V to 0.5 V based on its f_{osc}-V_{SGS} characteristics. It has the widest frequency range (249–399 GHz) among all the linear VCROs it has been compared against. The Non-linearity Error (*NE*) and the figure of merit (FoM_L) of this linear VCRO are 0.84% and 1.39×10^{-2} respectively. Considering the wide frequency range, the Non-linearity Error (*NE*) and the figure of merit of the proposed linear VCRO are quite acceptable. The proposed circuit design approach based on device engineering can provide considerable flexibility to design different types of communication circuits over a wide frequency range.

Authors Contribution Seyed Ali Sedigh Ziabari: Design and simulation; analysis and interpretation of curves; writing the first draft of this manuscript.

Syed Mahfuzul Aziz: Study supervision; technical support; revision of the manuscript to improve it.

Dimitri Lederer: Technical support; revision of the manuscript to improve it.

Data Availability Not Applicable.

Declarations

Ethics Approval and Consent to Participate Not Applicable.

Consent for Publication Not Applicable.

Research involving Human Participants and/or Animals Not Applicable.

Informed consent Not Applicable.

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Competing Interests The authors declare no competing interests.

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