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Ultra-low-power SOI CMOS pressure sensor based on orthogonal PMOS gauges

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***Abstract* – In this work, an ultra-low-power SOI CMOS pressure sensor is presented, using P-type MOSFET strain gauges to embed an active transducer in a 1 mm^2 1.5 µm-thick membrane. The system demonstrates: (i) a maximum sensitivity of 700 ppm/mbar, (ii) a precision down to 2 mbars, (iii) a power consumption less than 10 µW for the PMOS transducer.**

Keywords – Pressure sensor, membrane, MOSFET, ultra-low-power.

I. INTRODUCTION

Miniaturized pressure sensors are of great interest in many industry sectors such as automotive, environmental and biomedical. They are exploited to monitor industrial processing productions, weather conditions, physiological functions and treatments efficiency.

Silicon occupies an important place in the manufacture of such sensors, providing reliable micromachining and good performances in terms of sensitivity and precision. Piezoresistive and capacitive-based silicon devices constitute the two major pressure sensors families. The piezoresistive sensors classically consist of doped Si resistances mounted in a Wheatstone bridge configuration on a membrane [1-2]. They present a straightforward integration with a circuit interface, but typically consume mW's of power at several V's supply voltage. The capacitive sensors – i.e. planar capacitors with a mobile membrane electrode – offer good power consumption and sensitivity performances at the expense of large membranes or very small gaps [3-4].

In this paper, we target a highly-sensitive pressure sensors with a resolution of a few mbar around atmospheric pressure and present a less explored way to measure pressure with ultra-low power consumption, using active devices, i.e. MOS transistors as reported in [5-6]. Excellent sensitivity, higher than 200 and up to 700 ppm/mbar, is demonstrated with simple read-out circuit and ultra-low-power consumption (down to 10 µW for the transducer + ring oscillator (RO)).

II. SENSOR WORKING PRINCIPLE

Piezoresistivity is commonly used in strain gauges and pressure sensors. The piezoresistive coefficients, π, determine the variation of the electrical resistivity ρ, as a function of the directions of electrical currents and mechanical stresses (Fig. 1.b), according to the equation $\Delta\rho_{ij}/\rho_0 = \pi_{ijkl}\ \sigma_{kl} + O(\sigma^2)$, where ρ_0 is the stress-free resistivity, σ is the second rank tensor of mechanical stress. The suffices ijkl denote for i the direction of electrical potential measurement, for j the direction of current flow, for k the direction of the vector normal to the surface that the stress is applied to, and for l the stress direction. $O(\sigma^2)$ is the nonlinear contribution to the piezoresistance [7]. The nonlinear effects in silicon are negligible below 100 MPa stresses [8], and smaller than 5% below 200 MPa [9]. The π coefficients form a fourth-rank tensor, which can be reduced to three components thanks to the cubic symmetry of silicon: π_{11} (resp. π_{12}) for stresses applied longitudinally (resp. transversally) to the current direction and π_{44} for stresses applied in shear with the current direction. Their typical values in standard conditions are given in Table 1 and depend on the doping type. The largest coefficient is π_{44} for p-doped silicon.

Table 1. *First-order piezoresistance coefficients [10]*

	π_{11} [10^{-11}/Pa]	π_{12} [10^{-11}/Pa]	π_{44} [10^{-11}/Pa]	ρ [Ω.cm]
n-Si	-102.2	53.4	-13.6	7.8
p-Si	6.6	-1.1	138.1	11.7

The crystalline orientations for standard (100) silicon wafers are shown in Fig. 1.a. Directions [100] and [010] are 45°-tilted compared to the substrate flat orientation. Consequently, a 45° rotation of the π coefficients simplifies the piezoresistance modelling for the typical alignment of resistors and transistors, i.e. orthogonal to the flat. New π coefficients are defined as $\pi_{//} = (\pi_{11}+\pi_{12}+\pi_{44})/2$ and $\pi_{\perp} = (\pi_{11}+\pi_{12}-\pi_{44})/2$ [11].

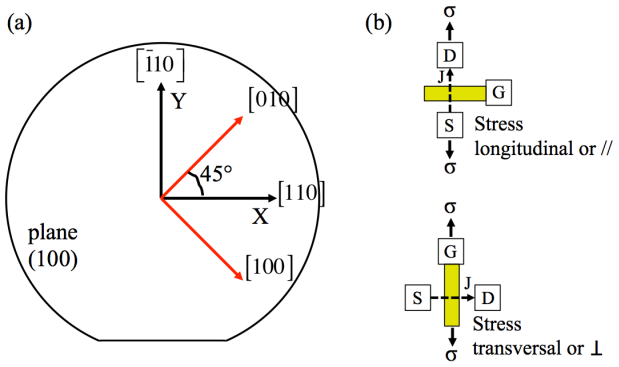

Fig. 1. *(a) Crystalline orientations in a (100) silicon wafer [12], (b) longitudinal or transversal stresses in transistor with D, S and G denoting MOSFET drain, source and gate contacts and indicating the current flow direction [13]*

They correspond respectively to resistivity variations occurring for stresses applied in parallel or in perpendicular to the current direction.
The previous relationship between ρ, π and σ can then be redeveloped for piezoresistive elements aligned orthogonally with the wafer flat as:

$$\begin{bmatrix}\Delta\rho_x/\rho_{0x}\\ \Delta\rho_y/\rho_{0y}\end{bmatrix} = \begin{bmatrix}\pi_{//} & \pi_{\perp}\\ \pi_{\perp} & \pi_{//}\end{bmatrix}\begin{bmatrix}\sigma_x\\ \sigma_y\end{bmatrix} \quad (1)$$

All the σ-components in the z direction are considered equal to 0, i.e. $\sigma_{zz}, \sigma_{xz}, \sigma_{yz} = 0$. The π-shear components for p-type silicon (=$\pi_{11}+\pi_{12}$) are also considered equal to 0. Notations for $\rho_{xx}, \rho_{yy}, \sigma_{xx}$ and σ_{yy} are simplified into ρ_x, ρ_y, σ_x and σ_y. To know the resistivity variation along the x-axis, the first line of the matrix is used while the second line is used for the resistivity variation along y-axis.
The pressure sensor detection principle is based on the aforementioned piezoresistive effect, exerted into on-membrane PMOS transistors. The current delivered by a MOS transistor in saturation regime can be simplified to:

$$I_{Dsat} = K(V_{GS} - V_{th})^2 \quad (2)$$

where $K = C_{ox}$ μW/L, with V_{GS} the gate-source voltage, V_{th} the threshold voltage, C_{ox} the gate oxide capacitance, μ the mobility, W and L the gate width and length of the transistor.
The stress applied to the transistor when the membrane deflects with pressure causes a mobility variation, which itself causes a current variation. The mobility μ is inversely proportional to ρ and σ, with $\Delta I_D/I_D = \Delta\mu/\mu = -\Delta\rho/\rho = -\boldsymbol{\pi}\,\boldsymbol{\sigma}$. The stress only affecting the mobility, the current in stressed transistors can be written, from Eq. 2, where $\boldsymbol{\pi}$ and $\boldsymbol{\sigma}$ are matrices:

$$I_D = (V_{GS} - V_{th})^2\, C_{ox}\mathrm{W/L}.\,\mu\,(1 - \boldsymbol{\pi\sigma}) \quad (3)$$

For two orthogonal PMOSFETs [14] forming a current mirror and having same V_{GS} and V_{th} (Fig. 2), the ratio between currents becomes:

$$\frac{I_{D2}}{I_{D1}} = \frac{K_2}{K_1} = \frac{(1-\boldsymbol{\pi\sigma_2})}{(1-\boldsymbol{\pi\sigma_1})} \quad (4)$$

with σ_1, I_{D1} and σ_2, I_{D2} being the stresses and the currents in transistors M1 and M2 respectively. The following development is applied to I_{D2}, in order to obtain the ΔI_{D2}:

$$I_{D2}(\sigma_1, \sigma_2) = I_{D2}(0,0) + \frac{dI_{D2}(0,0)}{d\sigma_1}\sigma_1 + \frac{dI_{D2}(0,0)}{d\sigma_2}\sigma_2,$$

and gives when applied to Eq. 4:

$$I_{D2}(\sigma_1, \sigma_2) - I_{D2}(0,0) = I_{D2}(0,0)(\boldsymbol{\pi\sigma_1} - \boldsymbol{\pi\sigma_2}) \quad (5)$$

This equation can be rewritten, by using the matrix (1):

$$\frac{\Delta I_{D2}}{I_2} = -\boldsymbol{\pi\sigma_2} + \boldsymbol{\pi\sigma_1} = -(\boldsymbol{\pi\sigma_2} - \boldsymbol{\pi\sigma_1})$$
$$= -((\pi_{//}\sigma_x + \pi_{\perp}\sigma_y) - (\pi_{\perp}\sigma_x + \pi_{//}\sigma_y))$$
$$= (\pi_{\perp} - \pi_{//})(\sigma_x - \sigma_y)$$

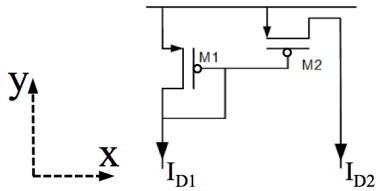

Fig. 2. *Current mirror with PMOS oriented orthogonally.*

And finally, the PMOS mirror delivers a current depending on the subtraction of stresses in x-direction, $\sigma_{//}$ and y-direction, $\sigma_{\perp}$:

$$I_{D2} = I_{D1}(1 + \pi_{\perp} - \pi_{//})(\sigma_x - \sigma_y)) \quad (5)$$

I_{D1} is the initial current generated by an NMOS current source (Fig. 3), and the transversal and longitudinal π_{PMOS} coefficients are fixed by circuit orientation. With this configuration, when $\pi_{\perp}$ and $\pi_{//}$ are expressed in function of π_{11}, π_{12} and π_{44}, Eq. 5 simplifies into:

$$I_{D2} = I_{D1}(1 + \pi_{44}(\sigma_y - \sigma_x)) \quad (6)$$

This configuration allows exploiting the highest π coefficient for p-type silicon, π_{44}. Cascading several PMOS mirrors will enhance the current amplification.

III. CIRCUIT DESCRIPTION

based on SOI CMOS technology and includes three functions, in a single chip (Fig. 3): (i) an active highly-sensitive mechanical stress transducer composed of a NMOS current source along with the two cascaded PMOS current mirrors, (ii) a 3-stage current-controlled ring oscillator (RO) read-out circuit for direct interfacing of the PMOS mirrors with the SPI port of a microcontroller and (iii) a large output buffer for driving large external loads. Piezoresistive CMOS transistors, called PIFETs, assembled as a differential pair or current mirror with PMOS oriented orthogonally, were previously proposed by [15].

Figure 3 also shows that the MOSFET-based piezoresistive pressure transducer consists of 4 PMOS transistors oriented orthogonally to maximize the stress sensitivity and that only the PMOS mirrors are embedded in a thin membrane for the pressure sensing, while the rest of the circuit lies on the standard SOI substrate for robustness reasons. The pressure-induced variations of the cascaded mirrors output current determines the oscillation frequency of the RO and the buffer finally generates a pressure-dependent square output signal.

The sensor is designed to minimize power consumption with a simple read-out interface, requiring no amplifier or ADC as for classical piezoresistive gauges and capacitive sensors. According to simulations, 90% of the 70 µW total power consumption is related to the buffer required to drive a large 100 pF-output capacitance in this set-up, meaning than less than 10 µW is needed for the transducer and RO when connected to an on-chip microcontroller.

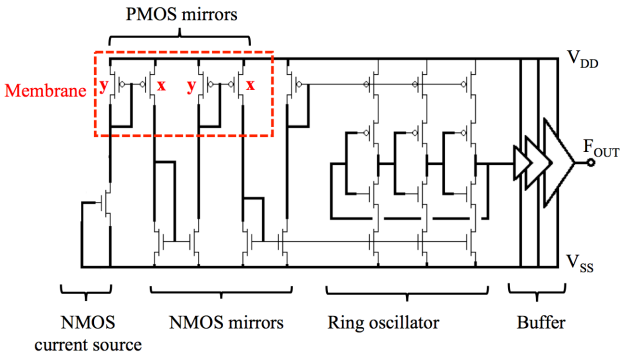

Fig. 3. *Pressure sensor MOSFET circuit with the SOI NMOS source, PMOS mirrors, ring oscillator and buffer.*

IV. SENSOR FABRICATION

The chip has been fabricated in UCL FDSOI 2µm technology. SOI technology offers a single-chip solution, i.e. monolithic integration on a high performance substrate with low voltage operation, low leakage, low crosstalk and high temperature working range.

The ultra-low-power (ULP) pressure sensor design is

The 1x1 mm^2 membrane, designed for pressure variation detection around the atmospheric pressure, is made of a 1.5 µm-thick silicon oxide-nitride-oxide stack [16], as represented on Fig. 4. For the transistors, the active Si film thickness is 80 nm and the gate oxide is 30 nm thick.

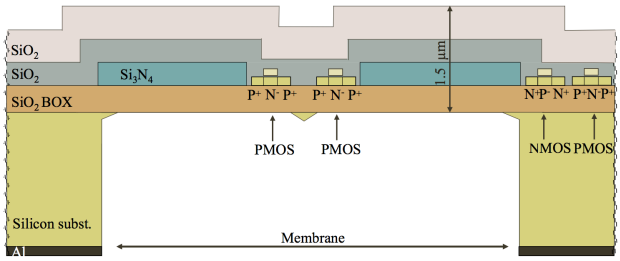

Fig. 4. *Schematic chip cross-section with embedded PMOS adjacent to a central silicon island.*

The Si_3N_4 layer, deposited by the low-pressure chemical vapor deposition technique (LPCVD) at 800°C, is highly tensile. The membrane stack ensures a slightly tensile membrane, with no buckling, once Si_3N_4 combined with compressive SiO_2 layer. The membrane release is obtained by patterning the silicon substrate with backside deep reactive-ion etching (DRIE) under Bosch process conditions, ended by a highly selective XeF_2 etching. The final isotropic etching leaves a silicon triangular island at the membrane centre. Figure 5 shows an optical view of the complete pressure sensor.

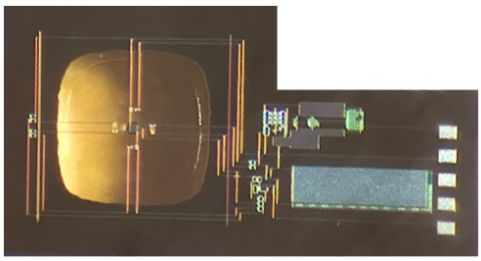

Fig. 5. *Pressure sensor and its 1x1 mm^2 membrane (left) and read-out CMOS circuits (right).*

V. SENSOR SIMULATIONS

To target the best resolution imposes a thin and large area membrane. Figure 6 shows two results obtained with finite element method (FEM) COMSOL Multiphysics® simulations showing stresses, taken at the bottom surface of the 1.5 µm-thick membrane. In these quick indicative simulations, the membrane is emulated by a single material having an effective Young's modulus calculated the arithmetic average of all four constitutive dielectrics SiO_2 and Si_3N_4 layers. No residual stresses are considered.

The values plotted are the distributions of the last Eq. 5

part, i.e. $(\sigma_x - \sigma_y)$, under 100 Pa applied pressure. To maximize the difference, sweet spots for the orthogonal PMOS mirror lie at the middles of each edge, as well as at the middles of the central island borders. The island, a 50 µm-side 5 µm-thick silicon square, creates a stress concentration in the centre. Placing the transistors adjacent to the island edges slightly decreases the pressure sensitivity but provides a more robust membrane compared to the typical solution using outer edges transistors, i.e. yielding higher burst pressure with less influence of membrane-to-transistors misalignment and enlargement of the process window according to our experiments.

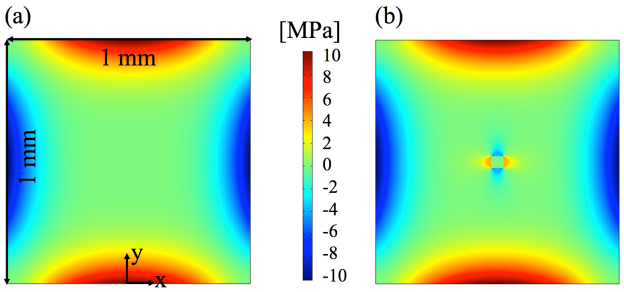

Fig. 6. *$\sigma_x - \sigma_y$ stress distributions under 100 Pa pressure for (a) bare and (b) with central island membranes.*

VI. SENSOR MEASUREMENT RESULTS

The membrane backside is sealed in a dual in-line ceramic package (DIL16) by a Norland Adhesive 68 photoresist at atmospheric pressure with the OmniCure® LX500 and its UV LED spot curing system.

The pressure sensor is first measured in a climatic chamber at constant atmospheric pressure, in order to experimentally assess the output sensor response versus the relative humidity (RH), the temperature, the supply voltage V_{dd} and the SOI wafer backside voltage V_{back} (Fig. 7). The sensitivity $\Delta f/\Delta$measurand varies according to the stimulus: (i) 0.1%/RH linearly for RH, (ii) 1.6%/°C linearly for temperature, (iii) quadratically for V_{dd}, with a minimum variation (almost zero) from 1.2 to 1.3 V, and (iv) cubically for V_{back}, with a minimum variation (almost zero) from -2 to -1 V. Each frequency point is an average of 4 period measurements obtained by an MSO8104 oscilloscope.

From these results, the output frequency signal can be de-noised, both mathematically and by biasing the sensor in the best voltage conditions to make the pressure measurements less sensitive to the variations of other parameters. More extensive work is currently under way to find the best trade-off between high sensitivity to pressure and small cross-sensitivities to other stimuli.

The pressure measurement set-up is presented in Fig. 8. The pressure is adjusted by controlling the nitrogen inlet and outlet ratio (RH = 0%), and can vary from 1 to 1.3 bar. The internal conditions are monitored by the pressure and temperature MPL115 gauges, embedded on Freescale KL25Z board and supplied at 5 V.

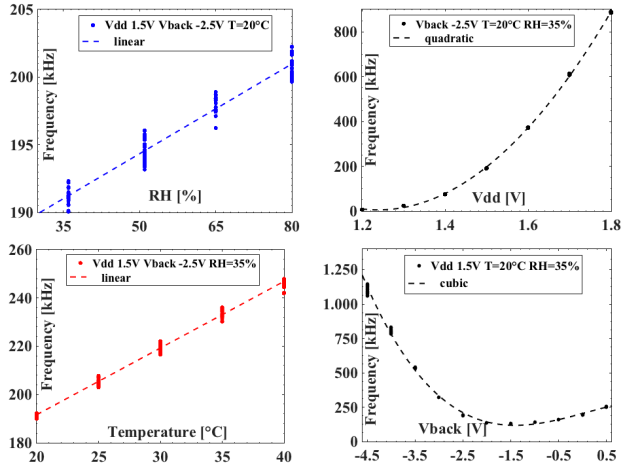

Fig. 7. *Influence of %RH, V_{dd}, the temperature and V_{back} on the frequency output at atmospheric pressure.*

The tested pressure sensor is powered on battery, regulated by a 1.2V low dropout regulator (LDO) and decoupling capacitance to minimize the noise on V_{dd}. The K2400 power supply controls the backgate voltage and the DSO91604 oscilloscope measures the output frequency. A LabWindows™ program allows GPIB control and datalogging.

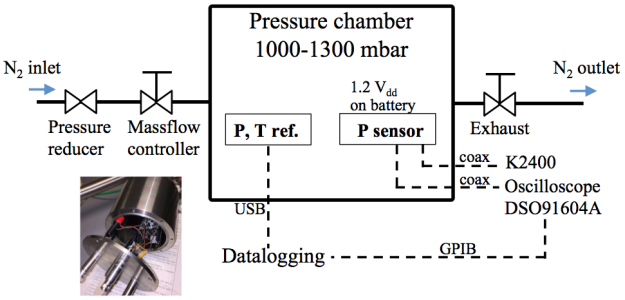

Fig. 8. *Pressure measurement set-up, picture in inset*

Figure 9 gives the frequency versus pressure variations, measured for the sensor presented in Fig. 5 with -4.5 V V_{back}. Each point is an average of 64 period measurements. Fluctuations are related to all the parameters varying during the measurement time as temperature, humidity, pressure, V_{dd}, V_{back}, floating backside voltage for on-membrane PMOS, etc. The linear correlation coefficient with the reference pressure sensor is 0.97, from 1050 to 1300 mbar. A maximum sensitivity equal to 100 Hz/mbar is found around 1250 mbar. Setting the sensor in this pressure range, where linearity and sensitivity are optimal, is achievable by controlling the initial deflection with a membrane prestressed by residual stresses and/or with an offset backside pressure when sealing the cavity. Different sensors measurements have shown pressure sensitivities from 200 up to 700 ppm/mbar.

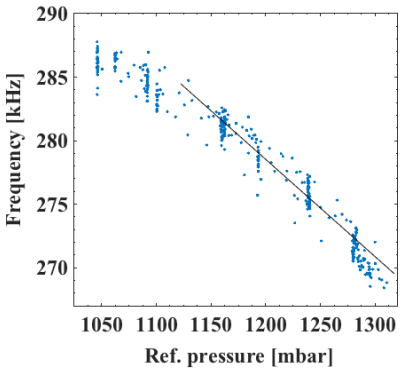

Fig. 9. *Frequency versus pressure response*

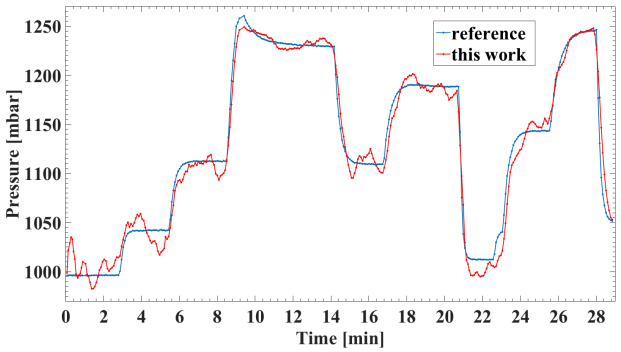

Fig. 10. *Comparison of the pressure measured by the reference sensor and the estimation obtained for our pressure membrane sensor using the correlation curve from Fig. 9.*

Figure 10 compares measurements of chamber pressure as a function of time from the reference sensor and our ULP sensor. For the latter, the pressure estimation is obtained from the frequency measurements taking the results of Fig. 9 into account and adding a subsequent treatment to the dataset: i.e. a quadratic regression to include results from 1000 to 1100 mbar after a 5 points moving averaging to de-noise local fluctuations. Reference and estimated pressure values are in good agreement. A precision down to 1-2 mbars can be reached with an oversampling of 400 measurements points (i.e. over 1 ms), based on an Allan deviation study.

Table 2 finally proposes a comparison between previous representative piezoresistive and capacitive pressure sensors with selected figures of merit. The three different working principles rely on mature CMOS-compatible technologies, which allow high miniaturization in monolithic designs.

All the sensors are based on a pressure-sensitive membrane, released by bulk or surface micromachining. Bulk micromachining is commonly combined with SOI substrate to obtain membranes, as in [3-5] and this work. Surface micromachining offers vacuum sealing during layer deposition. The considered range is around atmospheric pressure, which is the main target for biomedical and environmental sensors. Power consumptions are given for real-time measurements. However, the read-out can be turned off most of the time to spare energy for common applications. The measurement time, even counting the needed averaging, can be reduced to ms with >100 kHz signals. The two first table entries have a read-out consisting in four piezoresistive resistances mounted in Wheatstone bridge. The values of the resistance have also to be high (> 10 kΩ) to reduce the power consumption. The piezoresistive as well as the capacitive variations for 1 mbar are small, few µV or fF, which require a supplementary and adjacent read-out that should be taken into account for power consumption analysis. [4] uses an ASIC capacitance/voltage (C/U) converter with a differential voltage output signal adjustable in offset and gain. [5] presents the performances for one MOSFET. The performances of the presented pressure sensor are in the same order than the others but with more than 10x lower power consumption for the transducer and its RO interface. Design and process improvements such as gauge position on membrane and denoising techniques are currently under investigation to further improve the sensor accuracy.

Table 2: *Pressure sensors performances comparison*

#	Principle	Range	Sensitivity		Read-out	Power cons.
		[mbar]	$\Delta y/\Delta x$ [-/mbar]	$\Delta y/y_0/\Delta x$ [-/mbar]		[µW]
[17]	piezores.	200-1000	3.4 µV/V	NA	bridge	500
[1]	piezores.	500-1500	20 µV/V	NA	bridge	900
[3]	capa.	200-1200	8.3 fF	250 ppm	no	-*
[4]	capa.	900-1400	16 LSB	-	ASIC	300
[18]	capa.	300-1200	5.5 fF	550 ppm	no	-
[5]	FET	1000-1180	15 nA	75 ppm	no	-
This work	FET	1000-1300	100 Hz	250-700 ppm	osc.	10❖

**read-out dependent,* ❖10 µW (transducer + RO) or 70 µW (transducer + RO + buffer)

VII. CONCLUSIONS

Orthogonal PMOS transistors, embedded in ultra-thin-membrane, provide an original and power-efficient way to measure pressure. Combined with compact ring oscillator read-out, the miniature CMOS pressure sensor demonstrated performances aligned with the biomedical needs, i.e. a precision down to 2 mbars with less than 10 µW power consumption.

VIII. ACKNOWLEDGMENT

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