# Millimeter-Wave Low Noise Amplifiers in SOI for 5G/6G Joint Communication and Sensing

Mehmet Parlak, Member, IEEE, Martin Rack, L. Nyssens, Théo Denis, Student Members, IEEE,
Jean-Pierre Raskin, Fellow, IEEE and Dimitri Lederer, Senior Member, IEEE
*Université catholique de Louvain, Belgium*
e-mail: (see https://sites.uclouvain.be/RF-SOI-group)

***Abstract*— Joint Communication and Sensing (JCAS) has garnered considerable interest, offering dynamic resource allocation and operational adjustments based on real-time inputs, optimizing energy efficiency and overall system performance. JCAS comes with its challenges. Despite sharing a common front-end in a JCAS transceiver, communication and radio sensing exhibit distinct specifications, primarily in bandwidth and linearity. For the RF front-end to effectively function in both radar and communication modes, it is essential to incorporate reconfigurability concerning parameters such as gain, linearity, frequency, and bandwidth. Illustrating the operation of two LNAs in the 5G and 6G bands, this paper investigates the fully depleted (FD) silicon-on-insulator (SOI) technology as a candidate for JCAS systems integration while highlighting the utilization of the back-gate bias feature to enhance reconfigurability in communication and radar systems.**

***Index Terms* — Low noise amplifier, millimeter-wave circuits, silicon-on-insulator (SOI), fully depleted (FD) SOI, Joint Communication and Sensing (JCAS).**

## I. Introduction

In the realm of radar systems, Haykin's concept of "Cognitive Radar", as described in his own words, refers to an intelligent system that possesses an awareness of its surrounding environment. It utilizes prior knowledge and learns through interactions with the environment, adapting both its receiver and transmitter in real time to meet specific sensing objectives efficiently, reliably, and robustly [1].

Concurrently, as the demand for high-speed, low-latency communication systems intensifies due to the proliferation of augmented and virtual reality, and Internet of Things (IoT) technologies in everyday life, innovative approaches like Joint Communication and Sensing (JCAS) are poised to revolutionize multi-functional systems. JCAS, unlike traditional models, seamlessly integrates communication and sensing functionalities, forging a unified cognitive network. By synergistically leveraging data from both realms, JCAS enables a comprehensive understanding of the environment. This fusion empowers dynamic resource allocation and operational adjustments based on real-time inputs, optimizing energy efficiency and overall system performance.

The allure of high-frequency spectrums exceeding 100 GHz, which significantly enhances radar integration and performance, heightens consumer market interest, while the integration of radar sensors into IoT applications, known for their efficiency and precision in tasks like driving assistance and vital sign monitoring, further emphasizes the transformative potential of advanced communication technologies.

Amidst this landscape, JCAS emerges as a promising solution, offering simultaneous communication and sensing functionalities to optimize target detection and communication efficiency in various domains such as smart homes and cities, autonomous and intelligent transportation, environmental monitoring, surveillance and threat recognition, search and rescue operations, precision agriculture, wireless sensor networks, and even healthcare, as illustrated in Figure 1 [2].

While significant research efforts have delved into waveform classification, design, processing, and optimization for joint and collaborative operations [2-4], a noticeable gap exists in exploring front-end design challenges within JCAS mm-wave radio. The remainder of this paper unfolds as follows: Section 2 furnishes background material on JCAS transceivers and FD-SOI technologies. In Section 3, we showcase LNA designs in FD-SOI technologies, emphasizing the utilization of the back-gate bias feature to enhance reconfigurability. Sections 4 and 5 offer a comprehensive survey of SOI LNAs, presenting key findings, and engaging in a discussion on future avenues of exploration, respectively.

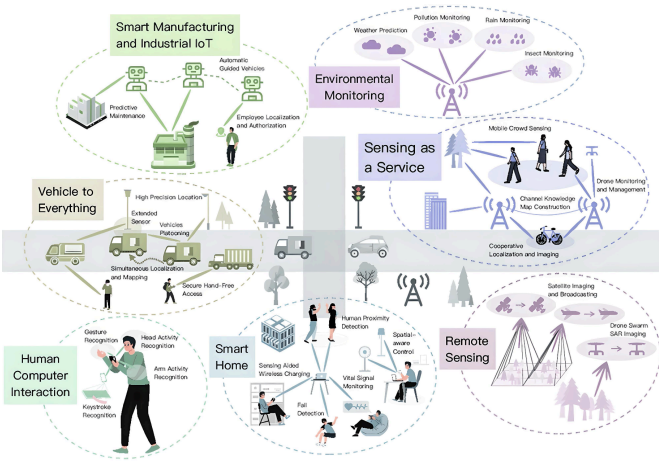


Figure 1. Use cases for JCAS sensors [2].

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## II. Background

### A. JCAS Transceivers

While communication and radar share a common RF front end, their specifications notably differ. Achieving seamless integration and operation of frequency-modulated continuous wave (FMCW) radar [5], pulsed radar [6-9], and communication within a single transceiver necessitates hardware reuse and reconfigurability in terms of gain, frequency bandwidth, and linearity [10]. Figure 2 illustrates the single channel of a JCAS beamformer, showcasing the utilization of the same front-end (comprising LNA and PA) across multiple communication and sensing functions, and various operational modes such as half- and full-duplex.

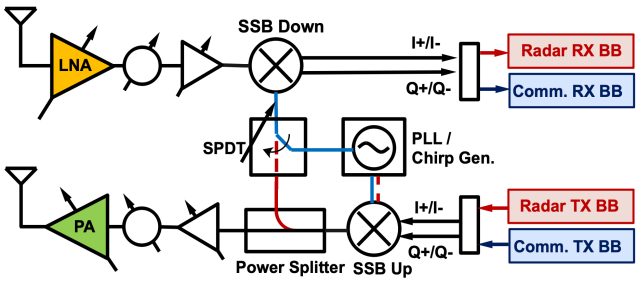


Figure 2. A transceiver for JCAS.

Noise poses a sensitivity challenge for both radar and communication transceivers as broad bandwidth is mandated for enhanced range resolution and data rates, respectively. The linearity expectations starkly contrast between radar and communication domains. The nature of pulsed radar signals, characterized by short durations and high-power transmissions occurring at regular intervals, exacerbates the demands on linearity. Furthermore, as the distance of sensing decreases (as in gesture recognition), the received power at the LNA increases significantly. Therefore, radar systems demand superior linearity to contend with scenarios where incoming signals can saturate LNAs, causing non-linearities and potentially compromising detection accuracy.

In the proposed pedestrian detection radar system [11], as the range to the target object varies from $R_{min}$ of 1m to $R_{max}$ of 48m, the input at the front-end beamforming unit spans from -111.53 dBm to -44.29 dBm, resulting in a dynamic range of 67.24 dB. The radar cross section (RCS) of the largest and smallest objects varies from $\sigma_{min}$ ($0.01m^2$) to $\sigma_{max}$ ($1m^2$), which results in an additional dynamic range of 20 dB. Designing circuits to achieve a dynamic range of 87.24 dB presents significant challenges, demanding variable gain amplification at the front end and baseband with minimal group delay imbalance [12]. Selecting reconfigurable and variable gain circuit architecture ensures high signal to noise ratio (SNR) and linearity in communication and radar operational modes, respectively.

### B. FD-SOI Technologies

Radio frequency (RF) applications have increasingly adopted partially depleted silicon-on-insulator (PD-SOI) technologies for circuit components such as RF switches due to their low off-capacitance ($C_{off}$) and inherent benefits in isolation and linearity attributed to the high-resistivity (HR) substrate.

However, at millimeter-wave (mmWave) frequencies, advanced nodes with shorter channel lengths are needed for high transition frequency ($f_t$) and maximum oscillation frequency ($f_{max}$). Fully depleted SOI (FD-SOI) addresses the challenges posed by short-channel effects in advanced nodes by improving gate control, reducing DIBL, lowering parasitic capacitances, and enhancing overall mmWave performance of circuit blocks. These advanced nodes, boasting reduced parasitics, achieve $f_t$ and $f_{max}$ values of approximately 300~400 GHz, rendering them ideal for circuits in Joint Communication and Sensing (JCAS) front-ends for 5G and 6G technology bands operating above 100 GHz. Therefore, FD-SOI technology, as exemplified by GlobalFoundries' 22FDX® at 22 nm and STMicroelectronics' 28 nm nodes, facilitates the cost-effective development of JCAS transceivers. Several other benefits and characteristics that have solidified FD-SOI's role in digital and mm-wave circuits are illustrated in Figure 3 [13] and [14].

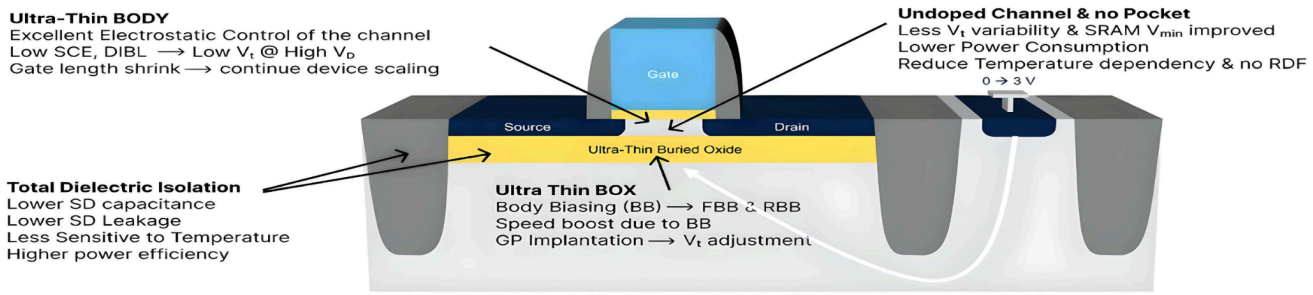


Figure 3: Benefits of FD-SOI Transistor and technology, where DIBL: Drain Induced Barrier Lowering, RDF: Random Dopant Fluctuation, FBB RBB: Forward Reverse Body Biasing, GP: Ground Plane [13].

With the ability to adjust the threshold voltage through back-gate control, FD-SOI technology introduces a unique tuning capability, enhancing configurability, crucial for JCAS transceivers. The Forward Body Biasing (FBB) feature/ability to dynamically adjust biasing during transistor operation [15-17] presents a dynamic avenue for integrating pulsed mm-wave radar circuits into the JCAS architecture, while optimizing both performance and power consumption of the front-end circuits .

## III. Low Noise Amplifiers in FD-SOI

Within the receiver, LNA stands out as the most critical component, exhibiting trade-offs between key performance parameters such as gain, linearity, power dissipation ($P_{dc}$), noise figure (NF). This section presents Q- and D-band LNAs implemented in 22nm FD-SOI CMOS process and showcases the trade-offs and the gain-tunability through the back-gate voltage.

### A. Q-Band LNA in 22-nm FD-SOI CMOS

As illustrated in Figure 4-a, a 36.7-43.3 GHz Q-band LNA is designed and implemented using 22FDX®, with a mm-wave back-end of line (BEOL), which includes 4 layers with thicknesses greater than 1 µm (JA to LB) [16]. The super-low threshold voltage nMOS with high $f_t$, high $f_{max}$ and low minimum noise figure ($NF_{min}$) performances is chosen in this design with the nominal gate length of 20 nm. Introducing a relaxed contact-poly-pitch (CPP) of 208 nm (2xCPP) serves to enhance $f_t$ and $f_{max}$ performance, albeit resulting in a slight increase in the active layout area, which remains inconsequential at the circuit level, as the overall area is predominantly governed by passive components. Optimal gate biasing of $M_1$ & $M_3$ ($V_{g1}$) at 0.4 V is identified to achieve the lowest $NF_{min}$ while ensuring sufficiently robust $f_t$ and $f_{max}$. Additionally, the voltage bias for $M_2$ & $M_4$ is meticulously adjusted to ensure equal voltage distribution across each device.

Utilizing back-gate bias modulation facilitates the adjustment of each stage's operational characteristics within defined voltage biases: $V_{g1,3}$ = 0.3 V, $V_{g2,4}$ = 1V, $V_{dd1,2}$ = 1.3V, and $V_{bgi}$ varying from -0.2 to 2V. This modulation corresponds to a range of drain currents ($I_d$) and power consumption levels spanning from 2.2-14 mA and 2.85-18.1 mW, respectively. To prevent detrimental effects such as forward biasing of the n-well/p-substrate diode and reverse breakdown, the back-gate bias range is carefully constrained. As illustrated in Figure 4-c, by adjusting the back-gate biases of stages 1 and 2, one can achieve trade-offs between DC power dissipation and metrics such as NF and gain primarily influenced by stage-1 bias, or between power consumption and metrics such as third-order intercept point (IIP3) and gain, that are primarily influenced by stage-2 bias.

Notably, the biasing of transistors closer to their threshold voltage results in a trade-off between noise and gain for power, leading to decreased $f_t$ and $f_{max}$, as well as increased $NF_{min}$ but reduced $I_d$. Simulation results, as depicted in Figure 4-b, illustrate the impact on $f_t$, $f_{max}$ and $NF_{min}$ of $M_1$, considering interconnects up to the JA layer. Furthermore, the optimal noise impedance is also modified, which further increases the NF for a constant input matching, mainly when biased close to threshold voltage where the FET characteristics have a sharp transition.

As discussed in [16], enhancing substrate RF performance using a high-resistivity substrate doesn't inherently boost mm-wave LNA performance with conventional designs. However, stacking multiple thick metal layers on a high-resistivity Si substrate can yield modest improvements in LNA performance. The use of a high-resistivity substrate coupled with a specialized inductor resulted in a 30% increase in quality factor (Q = 22.9). This improvement is attributed to the lower series resistance of the inductor due to metal stacking. Conversely, the quality factor of the input spiral inductor implemented on the QB layer is only 17.6 at 39 GHz, with simulations on a high-resistivity Si substrate. Consequently, no notable enhancements in small-signal performance (in gain or NF) are anticipated with a more resistive Si substrate unless multiple thick metal layers are stacked.

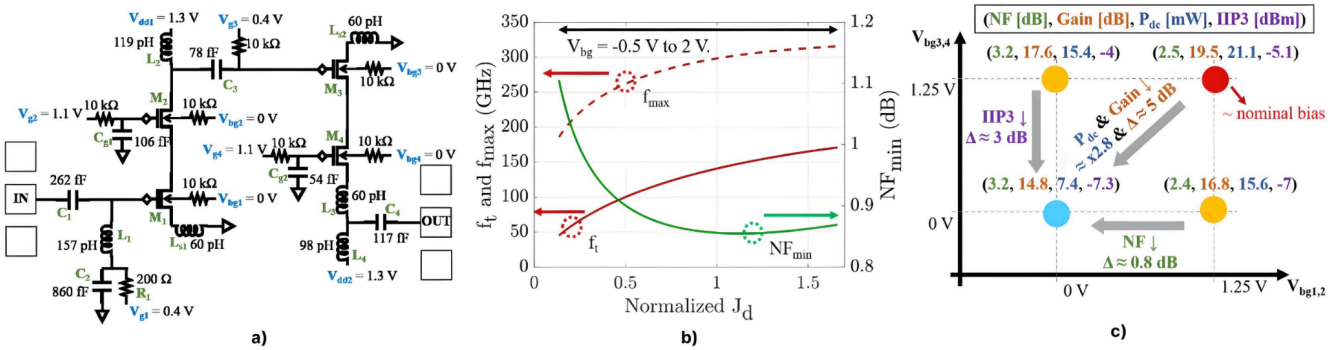


Figure 4. a) Schematic of the 2-stage LNA, b) Simulated $f_t$, $f_{max}$ , $NF_{min}$ of the common source with $V_{gs}$ = 0.3V, $V_{ds}$ = 0.65 V and $V_{bg}$ varying from -0.5 to 2 V (at 39 GHz). c) LNA measurements with back-gate bias $V_{bg\text{-}M1,2}$ and $V_{bg\text{-}M3,4}$ varying from 0 to 1.25 V.

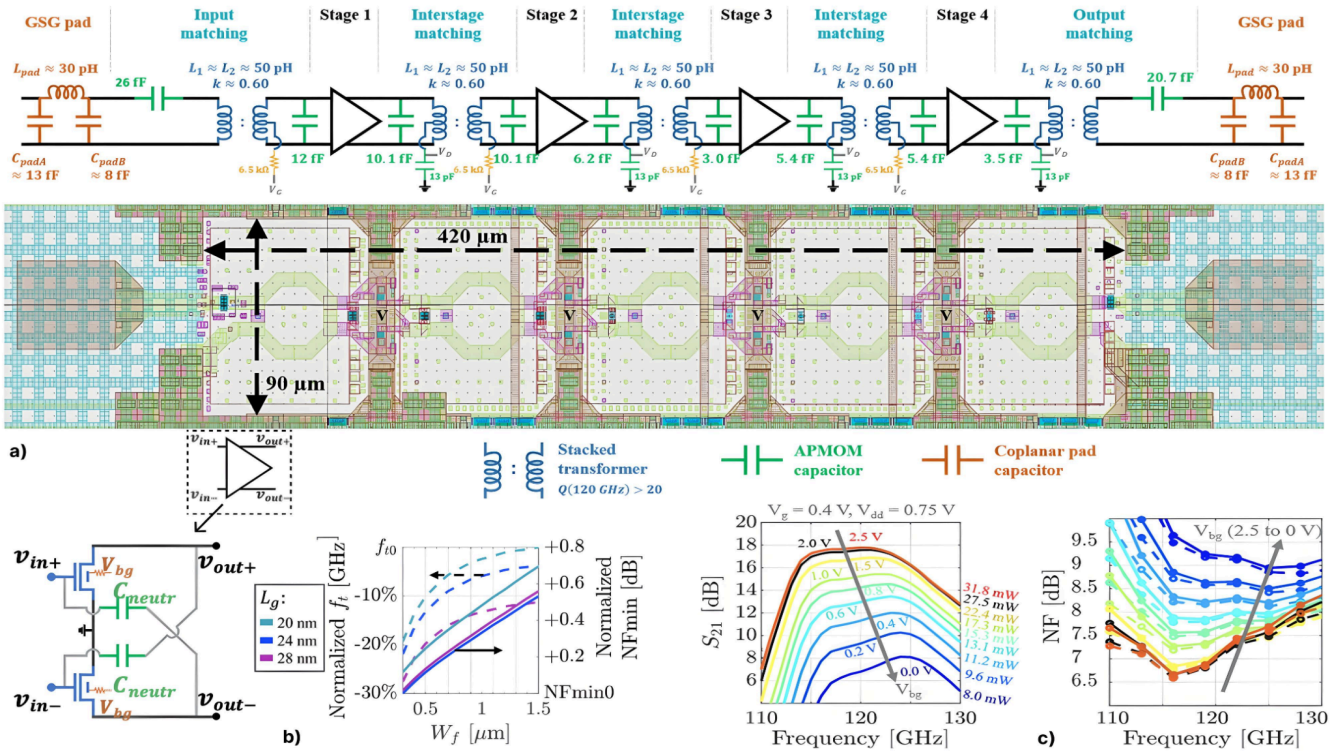


Figure 5. a) Schematic of the 4-stage LNA, b) Core amplification stage; CS differential pair with neutralization feedback capacitors and its simulated normalized $f_t$ and $NF_{min}$ as a function of transistor finger width, c) Gain and NF versus decreasing $V_{bg}$

### B. D-Band LNA in 22-nm FD-SOI

As illustrated in Figure 5-a, a D-band LNA operating within the frequency range of 113.5-127 GHz is constructed using 22FDX technology [17]. This LNA comprises four stages utilizing common-source differential-pair cores, incorporating cross-coupled neutralization capacitors for stability enhancement. The capacitors are sized to around 5.5 fF to counterbalance the $C_{gd}$ feedback capacitor of the device, ensuring unconditional stability across a broad frequency spectrum. The initial stages of the LNA are tailored to match the source closely to Γopt, aiming for near-optimal noise figure performance, while the latter stages approach conjugate matching at their sources to maximize gain. Interstage matching is facilitated by compact transformer cells featuring center-tap connections for amplifier core biasing. Input and output matching circuits utilize transformer components, functioning dually as baluns to drive the differential circuit in a balanced fashion.

As depicted in Figure 5-b, the selection of transistor finger width ($W_f$) plays a pivotal role in determining the gate resistance of the device and significantly impacts the $NF_{min}$ value. Opting for shorter $W_f$ values is favored in LNA designs, albeit at the expense of heightened fringing capacitances at the finger tips, consequently leading to a lower $f_t$. The length $L_g$ of each transistor has been extended from the standard 20 nm to 24 nm to mitigate noise contributions from the gate accesses. This compromise is illustrated in Figure 5-b. Extending $L_g$ to 24 nm entails a slight reduction in $f_t$ (and thereby available stage gain) but yields an enhanced NF. Additionally, it's observed that further extending $L_g$ to 28 nm only deteriorates $f_t$ without significantly altering NF. Thus, gate lengths were established at 24 nm for these reasons.

Achieving a minimal noise-figure of 6.6 dB within the in-band frequency range, the LNA exhibits a peak gain of 17.5 dB at its nominal bias, consuming 27.5 mW at a low supply voltage of 0.75 V. Furthermore, under high performance conditions with a supply voltage of 0.9 V, the LNA achieves a noise-figure as low as 6.1 dB and a gain of up to 19.1 dB with a power consumption of 34.8 mW.

As illustrated in Figure 5-c, the LNA features variable-gain functionality enabled by the unique back-gate bias node, allowing for a gain control range of 9.7 dB (from 17.8 to 8.1 dB) over a 2 V bias range while maintaining a favorable noise-figure value (6.6 to 8.9 dB).

## IV. A Survey and Conclusion

The survey [18] presents the performance results of LNA designs across various SOI processes, spanning from 2004 to 2023. Analysis of the survey data indicates that Q-band LNAs predominantly employ 45nm RF PD-SOI process, while D-band LNAs are primarily designed using 22nm FD-SOI processes.

As illustrated in Figure 6-a, the fractional bandwidth (FBW) of these designs typically hovers around or below 30% for Q-band and 20% for D-band. This underscores the impending challenges in JCAS design, aiming to achieve broader bandwidths at increasingly higher frequencies while upholding low noise figures and adequate gain, given the inherent constraints of semiconductor devices and circuit design. Implementing wideband matching networks with low insertion loss and effective impedance matching across a wide frequency spectrum poses considerable challenges, particularly in compact LNA configurations. Practical limitations related to parasitics, device characteristics, and interconnects impose restrictions on achievable bandwidth, particularly at elevated mm-wave frequencies.

Moreover, at elevated mm-wave frequencies, the deterioration in the noise factor occurs due to the diminished quality factor of passives and the low ratio of center frequency ($f_o$) to transition frequency ($f_t$). As illustrated in Figure 6-b , some designs, such as those by Landsberg [#35], Nyssens [#39], Tang [#41], and Rack [#49] specified in the survey [15], exhibit enhancements in NF as the process node scales down. Nevertheless, the relationship between NF and process nodes lacks a discernible pattern, owing to a multitude of factors beyond the technology node alone, including circuit topology and design considerations.

In parallel with the trend observed in noise figure (NF), a consistent pattern in the output 1 dB compression point (OP1dB) concerning scaling process nodes is not readily discernible across the dataset. Despite the reduction in supply voltage accompanying the scaling of process nodes, OP1dB and gain remains notably robust for the 22nm process, exhibiting values ranging from -2.5 dBm to 7.5 dBm and 16dB to 21dB across different frequency bands, respectively, as illustrated in Figure 6-c and 6-d. This underscores the nuanced influence of process node size on OP1dB, wherein variables such as transistor characteristics and circuit design intricacies play pivotal roles.

It's observed that several entries in the data with smaller process nodes do exhibit lower Pdc values compared to those with larger process nodes. This aligns with the expectation of reduced power consumption in smaller nodes due to smaller supply voltages.

Based on our investigation into Q- and D-band LNAs in 22nm FD-SOI CMOS technology presented in Section III, and the survey data provided, it becomes evident that the design of RF front-ends for JCAS systems is a complex endeavor, necessitating careful consideration of various performance metrics and design tradeoffs. Overall, while there are instances in the data that support the expected trends in Pdc, NF, and OP1dB when transitioning to smaller process nodes like 22nm, the relationship is not universal across all cases. This highlights the complex interplay between process technology, circuit design, and performance metrics, emphasizing the need for careful consideration and analysis on a case-by-case basis.

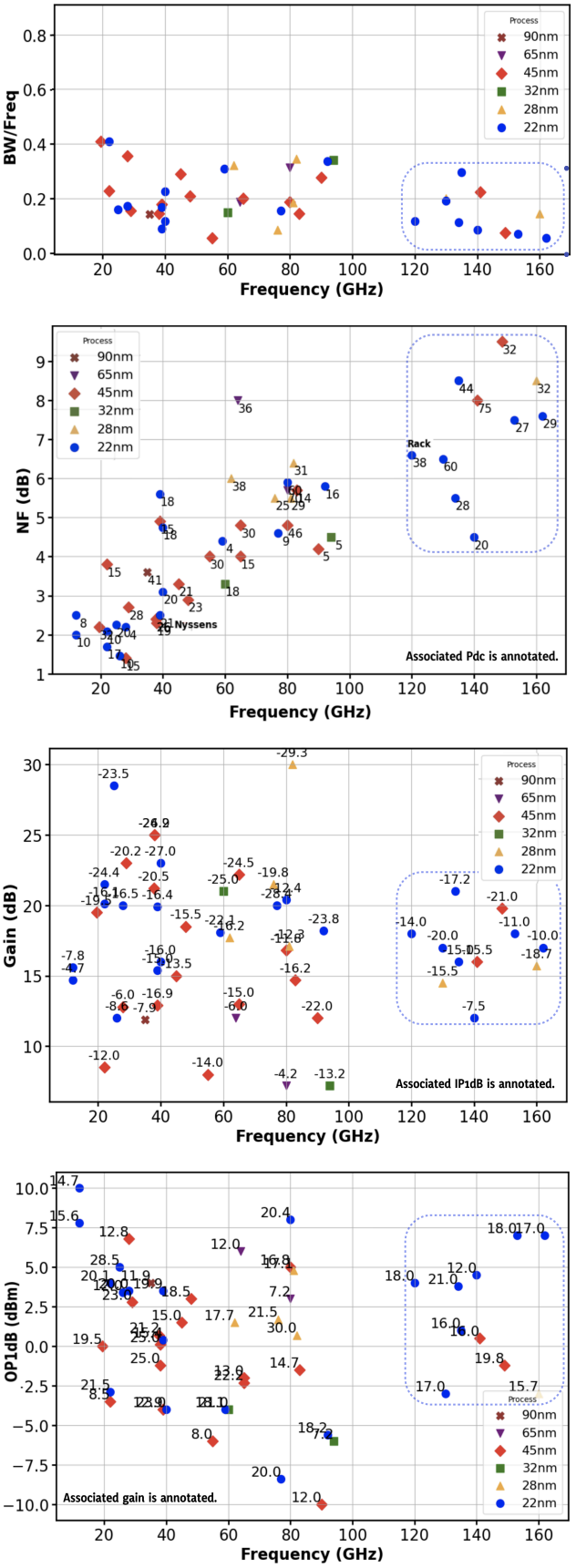


Figure 6. $BW_{fract.}$ , NF, OP1dB, Gain vs. frequency. in SOI tech.

## V. Future Work

Future work in the realm of JCAS transceiver development holds promise for further advancements in reconfigurability, performance optimization, and integration of advanced functionalities. One avenue for exploration involves extending the capabilities of the dynamic tuning mechanisms such as back-gate bias modulation in FD-SOI technology, which is also demonstrated through the Q- and D-Band LNAs illustrated in this paper.

Future work leveraging back-gate bias modulation in JCAS transceivers could focus on several fronts to enhance performance, adaptability, and energy efficiency. One potential direction is the refinement and optimization of biasing strategies to achieve finer control over transistor characteristics and circuit behavior. This could involve exploring advanced control algorithms or machine learning techniques to dynamically adjust back-gate biases in response to real-time operating conditions, environmental factors, or performance metrics.

Additionally, novel circuit architectures and design methodologies that exploit the full potential of back-gate bias to achieve reconfigurability and multifunctionality could be investigated. For example, integrating adaptive biasing schemes into RF front-end circuits could enable seamless switching between different operational modes, such as communication and radar sensing, without the need for external control signals or dedicated hardware to address the different input linearity and dynamic range requirements - for instance; enabling detection of closer targets.

Furthermore, future work could focus on extending the application of back-gate bias modulation to other functional blocks within JCAS transceivers, such as power amplifiers, frequency synthesizers or mixers [19]. Exploring how dynamic biasing techniques can improve the efficiency, linearity, and overall performance of these components could lead to significant advancements in JCAS system capabilities.

Moreover, researchers may investigate the potential of back-gate bias modulation for mitigating process variations and enhancing device reliability in FD-SOI technology. By dynamically adjusting bias voltages to compensate for manufacturing variations or aging effects, JCAS transceivers could maintain consistent performance over time and across different operating conditions.

Finally, exploring the integration of back-gate bias modulation with other emerging technologies, such as reconfigurable antennas could open up new possibilities for enhancing the functionality and versatility of JCAS transceivers. Overall, future work in this area has the potential to significantly impact the design, performance, and deployment of next-generation JCAS systems for various military, aerospace, and commercial applications.

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(Appendix) Table I. LNA designs across various SOI processes, spanning from 2004 to 2023

| # | Reference | Year | Process (SOI) | Frequency (GHz) | Bandwidth (GHz) | NF (dB) | Gain (dB) | OP1dB (dBm) | Pdc (mW) | Topology |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | Ellinger | 2004 | 90nm | 35 | 16 | 3.6 | 11.9 | 4 | 40.8 | 1-stage Cas. |
| 2 | Martineau | 2008 | 65nm | 80 | 25 | 5.7 | 7.2 | 3* | 70 | 3-stage CS. |
| 3 | Siligaris | 2010 | 65nm | 64 | 12 | 8 | 12 | 6 | 36 | 2-stage Cas. |
| 4 | Parlak | 2011 | 45nm RF | 48 | 10 | 2.9 | 18.5 | 3 | 22.8 | 2-stage Cas. |
| 5 | Inac | 2011 | 45nm RF | 45 | 13 | 3.3 | 15 | 1.5 | 20.8 | 2-stage Cas. |
| 6 | Inac | 2011 | 45nm RF | 65 | 13 | 4 | 13 | -2 | 15 | 2-stage Cas. |
| 7 | Inac | 2011 | 45nm RF | 83 | 12 | 5.7 | 14.7 | -1.5 | 13.5 | 3-stage CS |
| 8 | Kanar | 2013 | 45nm RF | 19.5 | 8 | 2.2 | 19.5 | 0 | 32.5 | 2-stage (CS + Cas.) |
| 9 | Plouchart | 2015 | 32nm | 60 | 9 | 3.3 | 21 | -4 | 18 | 3-stage Cas. |
| 10 | Karaca | 2017 | 28nm FD | 62 | 20 | 6 | 17.7 | 1.5 | 38.2 | 3-stage CS |
| 11 | Vigilante | 2017 | 28nm FD | 82 | 28.3 | 6.4 | 30 | 0.7 | 31.3 | 4-stage Diff. CS |
| 12 | Gao | 2018 | 45nm RF | 90 | 25 | 4.2 | 12 | -10 | 4.7 | 2-stage CS + 1-stage Cas. |
| 13 | Li | 2018 | 45nm RF | 28 | 10 | 1.4 | 12.8 | 6.8 | 15 | 1-stage Cas. |
| 14 | Parveg | 2018 | 28nm FD | 160 | 23 | 8.5 | 15.7 | -3 | 32 | 4-stage CS |
| 15 | Sayginer | 2018 | 32nm | 94 | 32 | 4.5 | 7.2 | -6 | 5.2 | 1-stage Cas. |
| 16 | Zhang | 2019 | 22nm FD | 26 | 15 | 1.46 | 12 | 3.4 | 9.8 | 1-stage Cas. with ind. degen. |
| 17 | Gao | 2019 | 22nm FD | 40 | 9 | 3.1 | 23 | -4 | 20.5 | 3-stage Cas. with 3-pole HPF |
| 18 | Lee | 2019 | 45nm RF | 65 | 31 | 4.8 | 22.2 | -2.3 | 30 | 4-stage Cas. |
| 19 | Paulin | 2019 | 28nm FD | 76 | 6.5 | 5.5 | 21.5 | 1.7 | 25 | Diff. CS with ind. degen. |
| 20 | Farid | 2019 | 22nm FD | 135 | 40 | 8.5 | 16 | 1 | 44 | 4-stage Diff. CS |
| 21 | Gao | 2020 | 22nm FD | 77 | 12 | 4.6 | 20 | -8.4 | 9 | 3-stage Cas. with Xformer |
| 22 | Gao | 2020 | 22nm FD | 92 | 31 | 5.8 | 18.2 | -5.6 | 16 | 3-stage Cas. with Xformer |
| 23 | Cui | 2020 | 22nm FD | 22 | 17 | 1.7 | 21.5 | -2.9 | 17.3 | 2-stage (CS + Cas.) |
| 24 | Aassar | 2020 | 22nm FD | 22 | 9 | 2.08 | 20.1 | 4 | 9.6 | 2-stage CS. (back bias) |
| 25 | Aassar | 2020 | 22nm FD | 25 | 4 | 2.25 | 28.5 | 5 | 20 | 2-stage Cas. (back bias) |
| 26 | Hamani | 2020 | 45nm RF | 141 | 31.5 | 8 | 16 | 0.5 | 75 | 4-stage Diff. |
| 27 | Li | 2020 | 45nm RF | 80 | 15 | 4.8 | 16.8 | 5 | 46 | 3-stage Diff. CS. |
| 28 | Morath | 2021 | 22nm FD | 59 | 18.3 | 4.4 | 18.1 | -4 | 3.6 | 2-stage Cas. |
| 29 | Shaheen | 2021 | 45nm RF | 22/39 | 5/7 | 3.8/4.9 | 8.5/12.9 | -3.5/-4 | 15 | 2-stage Cas. (multi-band) |
| 30 | Hu | 2021 | 45nm RF | 38 | 25 | 2.4 | 25 | -1.2 | 25.5 | 2-stage Cas. |
| 31 | Li | 2021 | 45nm RF | 29 | 4.5 | 2.7 | 23 | 2.8 | 28 | 1-stage CS + 2-stage Cas. |
| 32 | Li | 2021 | 45nm RF | 38 | 5.5 | 2.3 | 25 | 0.1 | 18.6 | 1-stage CS + 2-stage Cas. |
| 33 | Ghanevati | 2021 | 45nm RF | 55 | 20 | 3 | 6 | 4 | 30 | 1-stage CS |
| 34 | Zandieh | 2021 | 45nm RF | 149 | 11 | 9.5 | 19.8 | -1.2 | 32 | 3-stage Cas. with Xformer |
| 35 | Landsberg | 2021 | 22nm FD | 134 | 15 | 5.5 | 21 | 3.8 | 28 | 3-stage CS |
| 36 | Li | 2022 | 22nm FD | 80 | N/A | 5.9 | 20.4 | 8 | 60 | 2-stage Cas. |
| 37 | Ravellec | 2022 | 28nm FD | 81 | 15 | 5.5 | 17.1 | 4.8 | 29.4 | 2-stage Diff. CS |
| 38 | Mangraviti | 2022 | 22nm FD | 39 | 3.5 | 15.4 | 5.6 | 0.4 | 18.5 | 2-stage Diff. CS |
| 39 | Nyssens | 2022 | 22nm FD | 39 | 6.6 | 2.5 | 19.9 | 3.5 | 20.8 | 2-stage Cas. |
| 40 | Hetterle | 2022 | 22nm FD | 130 | 24.8 | 6.5 | 17 | -3 | 60 | 4-stage differential CS. |
| 41 | Tang | 2022 | 22nm FD | 138 | 20 | 4.5 | N/A | N/A | 20 | 4-stage differential CS. |
| 42 | Kim | 2022 | 28nm FD | 130 | 26 | N/A | 14.5 | N/A | 21.6 | 3-stage CS (Gain-boosting) |
| 43 | Fu | 2022 | 22nm FD | 40 | 4.7 | 4.75 | 16 | 7.8 | 18 | 3-stage Cas. |
| 44 | Kobal | 2022 | 22nm FD | 28 | 4.8 | 2.2 | 20 | 3.5 | 4.4 | 2-stage Cas. |
| 45 | Hu | 2023 | 45nm RF | 37.8 | 19 | 2.4 | 21.2 | 0.7 | 25.5 | Dual-resonant input matching |
| 46 | Artz | 2023 | 22nm FD | 153 | 10.8 | 7.5 | 18 | 7 | 27 | 4-Stage Diff. CS (back-gate) |
| 47 | Radpour | 2023 | 22nm FD | 15 | 15.7 | 2.8 | 15.6 | 0 | 7.8 | 2-stage CS. |
| 48 | Mustapha | 2023 | 22nm FD | 162 | 9 | 7.6 | 17 | N/A | 28.8 | 1-stg CS. + 6-stg Casc. + 1-stg CS. |
| 49 | Rack | 2023 | 22nm FD | 120 | 14 | 6.6 | 18 | 4* | 38 | 4-Stage Diff. CS (back-gate) |

* simulated