Subthreshold Operation of Self-Cascode Structure Using UTBB FD SOI Planar MOSFETs

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***Abstract*— This paper presents an experimental analysis of the analog characteristics of self-cascode structures composed by 28 nm technological node ultra-thin body and BOX fully-depleted silicon-on-insulator planar MOSFETs, focusing on the subthreshold operation regime. Apart from the increased gain promoted by the reduction of front gate voltage, there is further improvement when the back-gate bias is used to reduce the threshold voltage of transistor close to the drain of the composite device, making this structure a promising option for low-power low-voltage (LPLV) analog applications.**

Keywords— UTBB, self-cascode, subthreshold, low-power, SOI MOSFET, asymmetric structure, composite transistor

I. Introduction

Ultra-thin body and buried oxide (UTBB) technology is a promising evolution of conventional planar FD SOI technology, where enhanced electrostatic control of the channel charges by the gate bias is obtained thanks to the very thin active layer and BOX thicknesses. As a result, further downscaling of channel length can be achieved [1]. Amongst the reported advantages of UTBB, one can mention improved short-channel effects [2], variability [3], parasitic resistances and capacitances and analog figures of merit [4]. The use of self-cascode (SC) structure is a common way to improve analog performance of MOS transistors [5]. In this structure, schematically shown in Fig. 1, two transistors are associated in series, with gates connected and V_G, V_D and V_S are the gate, drain and source biases, respectively, and MS and MD are the transistors close to the source and close to the drain, respectively, with length L_S and L_D.

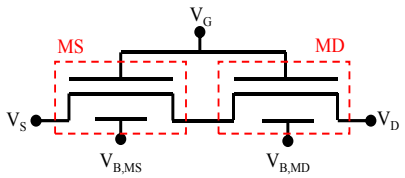

Fig. 1. Schematic representation of a self-cascode structure.

Usually, both transistors feature the same threshold voltage (V_T) forming a structure called symmetric SC (S-SC). It is reported to reduce the output conductance, without compromising the transconductance. By playing with the doping concentration in the channel in order to reduce the V_T of MD, the asymmetric self-cascode (A-SC) has been proposed [5]. For this case, the benefits of SC are further enhanced due to the reduction of the electric field peak close to the drain-channel junction and the generation of carriers by impact ionization [6].

However, for more recent technologies, where MOSFETs channel are usually undoped, reaching different V_T by changing the doping concentration is not always a possibility. Therefore, the A-SC structure can take advantage of the V_T control by the back-gate bias (V_{BS}=V_B-V_S) offered by the UTBB technologies [3, 7]. SPICE simulation results reported in [8] have shown that the V_B tuning combined with the SC structure can provide a promising alternative for analog circuit design. In this context, this paper presents, for the first time, experimental results of analog parameters of SC structures composed by UTBB SOI transistors, operation at low front gate voltages, aiming at low-power low-voltage applications.

II. Device Characteristics and Methodology

This work was based on experimental measurements on individual transistors of 28 nm technological node fabricated by ST-Microelectronics and measured at UCLouvain. These transistors showcase a BOX thickness of 25 nm, active layer thickness of 7 nm and front gate EOT of 1.3 nm [3]. The devices used in this work are 1 µm wide, with length (L) of 30 and 80 nm and display the threshold voltages and subthreshold slopes (SS) shown in Table I for two different V_{BS}. The I-V characteristics of Symmetric and Asymmetric SC structures have been obtained by using a coding method described in [8] using the DC experimental measurements of the single transistors. In S-SC structures, both transistors feature V_{BS} = 0 V. For the A-SC devices, MS transistor present $V_{BS,MS}$ = 0 V

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and MD has reduced threshold voltage, by applying $V_{BS,MD}$ = 1.6 V.

TABLE 1.THRESHOLD VOLTAGE AND SUBTHRESHOLD SLOPE OF SINGLE TRANSISTORS USED TO FORM SELF-CASCODE STRUCTURES.

Length [nm]	V_{BS} = 0 V		V_{BS} =1.6 V	
	V_T [V]	*SS [mV/dec]*	*V_T [V]*	*SS [mV/dec]*
30	0.49	73.7	0.41	69.6
80	0.47	66.1	0.39	61.8

III. EXPERIMENTAL RESULTS

Fig. 2 shows the subthreshold drain current (I_{DS}) as a function of gate overdrive voltage ($V_{GT} = V_{GS} - V_T$) biased in saturation (V_{DS} = 1 V) for SC and a single transistor with L=80 nm. It is worthwhile to mention that the overall V_T of A-SC transistors is given by MS. Also, from the presented curves one can note that SC with the same length of MS (L_S) present the same SS as the one obtained for the single transistor used as MS. Aiming at correlating inversion level to bias current, the curves of the transconductance-to-current ratio (g_m/I_{DS}) as a function of I_{DS} and V_{GT} are shown in Fig. 3. In this study, focus is given on devices operating in weak-moderate inversion, i.e. $V_{GT} \leq 0V$, which corresponds to $g_m/I_{DS} > \sim 15V^{-1}$. As shown by these results, the single transistor and SC structures with L_S=80 nm present slightly larger values of g_m/I_{DS} for low I_{DS}, which is related to the reduced SS observed in Fig. 2.

The transconductance (g_m) and output conductance (g_D) curves, extracted from the derivative of I_{DS} as a function of V_{GS} and V_{DS}, respectively, are shown in Fig. 4 and 5, for V_{DS}=1V and V_{GT}=-200mV, -100mV and 0V. Both g_m and g_D values are reduced as the structures are biased deeper in subthreshold region. It can be seen that SC (both A- and S-) with the same L_S present similar g_m. On the other hand, g_D is highly influenced by the asymmetry of V_T. In the structures where $L_S = L_D$, g_D has shown a reduction of up to 6 times by reducing V_T of MD. This reduction can reach almost 20 times when increasing L_D, which is in accordance to the results presented in the literature [5]. Also, any A-SC has shown reduced g_D in comparison to the single transistor.

The values of Early voltages V_{EA} (defined as I_{DS}/g_D) are shown as a function of g_m/I_{DS} ratio for V_D = 1V in Fig. 6. In general, the increase of g_m/I_{DS} promoted a slight reduction of V_{EA}. However, the use of A-SC increased V_{EA} independent on the association. For the shortest SCs, an increase of at least 3.8 times has been obtained for V_{EA} @ V_{GT}=-200mV. Nevertheless,

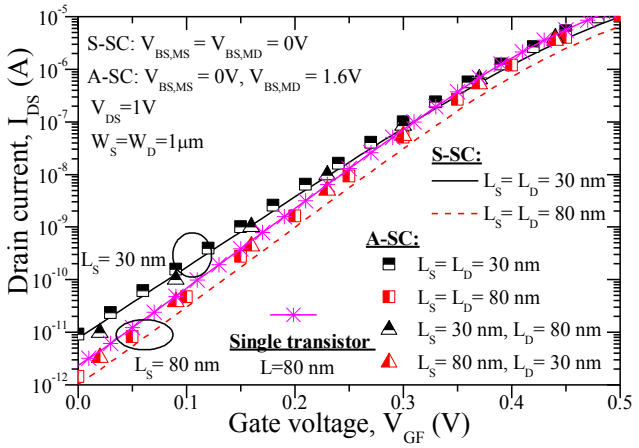

Fig. 2. Drain current vs gate voltage for S-SC and A-SC devices with various L_S and L_D combinations.

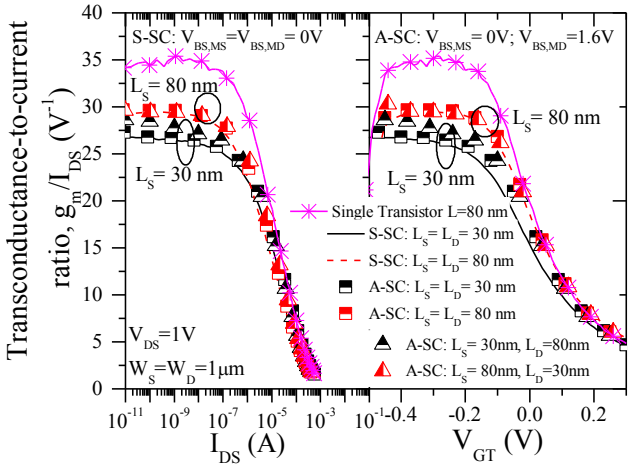

Fig. 3. Transconductance-to-current ratio vs I_{DS} and V_{GT} for different S-SC and A-SC devices at V_D=1V.

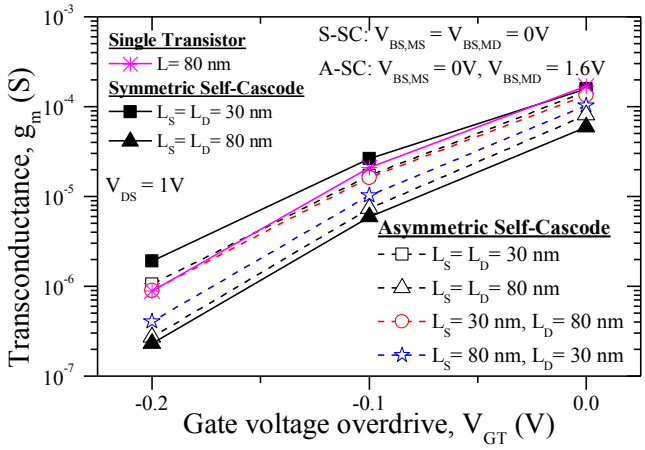

Fig. 4. Transconductance as a function of the gate voltage overdrive for a single transistor (L=80 nm), S-SC and A-SC devices with various L_S and L_D combinations.

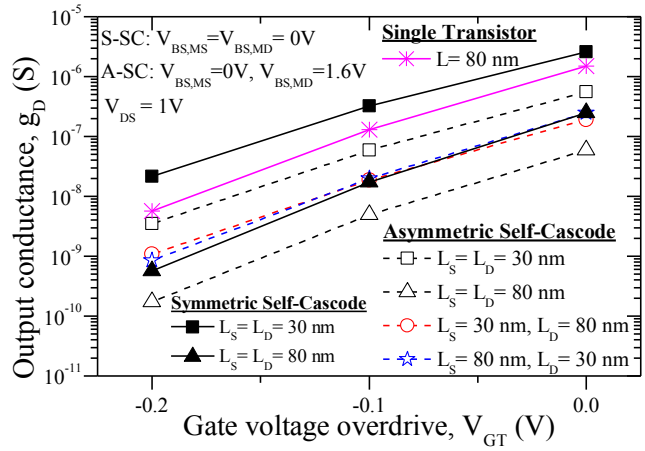

Fig. 5. Output conductance as a function of the gate voltage overdrive for a single transistor (L=80 nm), S-SC and A-SC devices with various L_S and L_D combinations.

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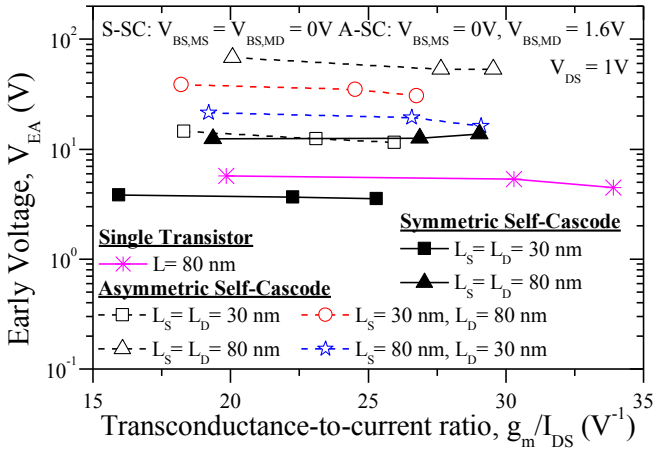

Fig. 6. Early voltage as a function of g_m/I_{DS} for a single transistor (L=80 nm), S-SC and A-SC devices with various L_S and L_D combinations.

the small increase of g_m/I_{DS} in A-SC is responsible for a larger intrinsic voltage gain (A_V) as V_{GT} reduces (larger g_m/I_{DS}), as shown in Fig. 7. As for V_{EA}, its increase provided by A-SC reflects on an improvement on the gain. As expected, longer devices present larger A_V. Among the S-SC structures, the one with L_S=L_D=80 nm has shown A_V around 50 dB. It is interesting to note that similar A_V can be obtained with L_S=L_D=30 nm if A-SC is used. In addition, any A-SC, even with L_S=L_D=30 nm, presented larger gain than the single transistor with L=80 nm.

Fig. 8 displays g_m and a function of A_V. Although the use of A-SC allows for larger A_V in comparison to S-SC, when biasing these devices at sub-V_T, there is a reduction of g_m, which can compromise frequency. Therefore, a compromise must be established between gain and frequency when using SC at low voltage. Finally, the intrinsic voltage gain is shown as a function of power. The presented results show that at 1µW, for SCs with L_S=30nm, A_V of A-SC devices is 10 to 20 dB larger than the gain of S-SC counterpart.

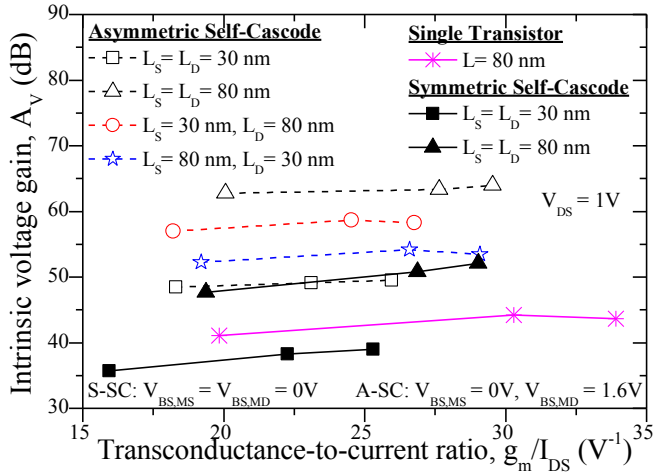

Fig. 7. Intrinsic voltage gain as a function of g_m/I_{DS} for a single transistor (L=80 nm), S-SC and A-SC devices with various L_S and L_D combinations.

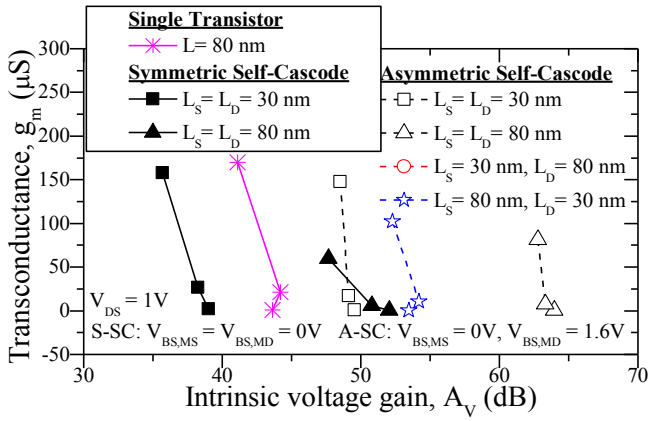

Fig. 8. Transconductance as a function of the intrinsic voltage gain for a single transistor (L=80 nm), S-SC and A-SC devices with various L_S and L_D combinations

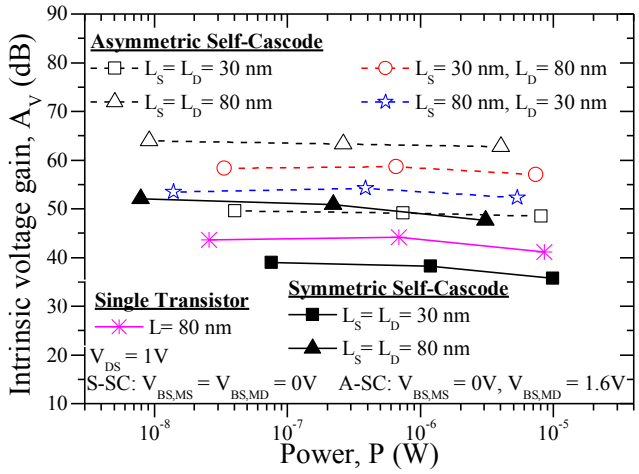

Fig. 9 Intrinsic voltage gain as a function of the power for a single transistor (L=80 nm), S-SC and A-SC devices with various L_S and L_D combinations.

REFERENCES

[1] Y.-K. Choi *et al.*, "Ultrathin-body SOI MOSFET for deep-sub-tenth micron era," *IEEE Electron Device Letters*, vol. 21, no. 5, pp. 254–255, May 2000.

[2] S. Burignat *et al.*, "Drain / substrate coupling impact on DIBL of Ultra Thin Body and BOX SOI MOSFETs with undoped channel," in *ESSDERC '09. Proceedings of the European*, 2009, pp. 141–144.

[3] N. Planes *et al.*, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *2012 VLSIT*, 2012, pp. 133–134.

[4] M. K. Md Arshad *et al.*, "UTBB SOI MOSFETs analog figures of merit: Effects of ground plane and asymmetric double-gate regime," *Solid-State Electronics*, vol. 90, pp. 56–64, Dec. 2013.

[5] M. Gao, J.-P. Colinge, L. Lauwers, S. Wu, and C. Clayes, "Twin-MOSFET structure for suppression of kink and parasitic bipolar effects in SOI MOSFETs at room and liquid helium temperatures," *Solid-State Electronics*, vol. 35, no. 4, pp. 505–512, Apr. 1992.

[6] M. de Souza, D. Flandre, R. T. Doria, R. Trevisoli, and M. A. Pavanello, "On the improvement of DC analog characteristics of FD SOI transistors by using asymmetric self-cascode configuration," *Solid-State Electronics*, vol. 117, pp. 152–160, Mar. 2016.

[7] L. Martins d'Oliveira, V. Kilchytska, D. Flandre, and M. de Souza, "Design benefits of self-cascode configuration for analog applications in 28 FDSOI - IEEE Conference Publication," in *EUROSOI-ULIS 2018*, Spain, 2018.

[8] L. Martins d'Oliveira, V. Kilchytska, D. Flandre, and M. de Souza, "Self-Cascode Current-Voltage Curve-Construction Algorithm from Single MOSFET Measurements for Analog Figures-of-Merit Extraction," *JICS*, vol. 14, no. 1, 2019.

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